A NOVEL TRENCH LATERAL POWER MOSFET WITH HIGH BREAKDOWN VOLTAGE AND LOW ON-RESISTANCE

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Department of Electrical and Computer Engineering
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ABSTRACT

This thesis deals with lateral power MOSFETs which are used in disc drives, power supplies, and automotive applications. Power MOSFETs are popular because of their high switching speed, high input impedance and wide safe operating area. However, reduction in device specific on-resistance is limited in conventional lateral DMOS transistors due to the long drift region associated with the drain. The objective of this thesis is to propose a novel power MOSFET to solve the problem.

A novel Trench Lateral Power MOSFET (TLPM) and its fabrication process are proposed in this thesis. The TLPM is implemented along the sidewall of trenches in order to increase packing density of the MOSFET. The process utilizes self-aligned method to form the gate electrode and the trench bottom contact holes to the drain to achieve minimum pitch and very low on-resistance.

Simulation results show that the proposed TLPM with a device pitch of 4 μm has a similar current handling capability to a Conventional LPM (CLPM) with a device pitch of 8 μm for devices with breakdown voltage of 80 V, indicating drastic improvement of specific on-resistance for the TLPM. Experimental verification proves that the unique self-aligned method to open trench bottom contact holes to the drain leads to reduced device pitch. The results show that the specific on-resistances for the TLPM and CLPM are 0.8 $m\Omega\text{-}cm^2$ and 1.6 $m\Omega\text{-}cm^2$ respectively for a 80 V breakdown device.

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CHAPTER 1

Introduction

The idea of combining power devices and integrated circuits on a single chip is quite attractive because integration of multiple functions into one chip reduces system costs and increases reliability by reducing packaging count, saving area of implementation and eliminating interconnections. A simple block diagram of a Power Integrated Circuit (PIC) is shown in Figure 1.1. The power devices which drive actuators can be protected from overvoltage, overcurrent and overtemperature by circuitry with sensing devices. The integrated microprocessor unit provides control functions by responding to the state of the actuator. As indicated in Figure 1.2 [1], PICs cover a number of applications such as computer peripherals, consumer electronics, and automotive applications.

PIC technology, using junction isolated bipolar transistors, emerged in the late

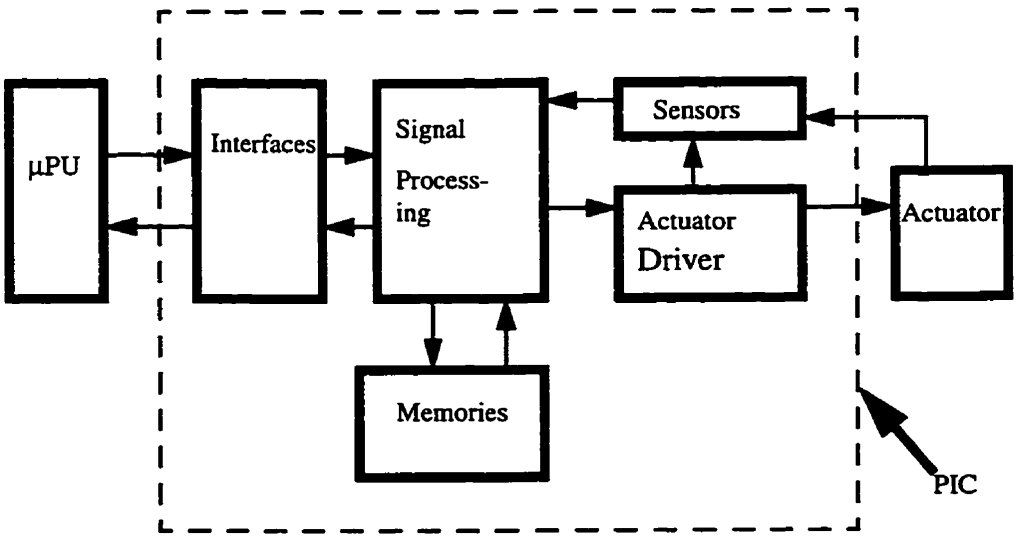

Figure 1.1 A simple block diagram of a PIC

1960's [2], however, it did not become a success because of the limitations of bipolar power technology. One of them is slow switching speed associated with the storage of minority carriers in the base. Another is the occurrence of second breakdown which limits the voltage handling capability of the device. In addition driving power caused by the base current is far from negligible and cannot be reduced, thus limiting efficiency. Furthermore, bipolar processes gain little from lithography advances because the current carrying capability of bipolar transistors depends on the emitter area.

In comparison with power bipolar transistors, MOSFETs have shown advantages

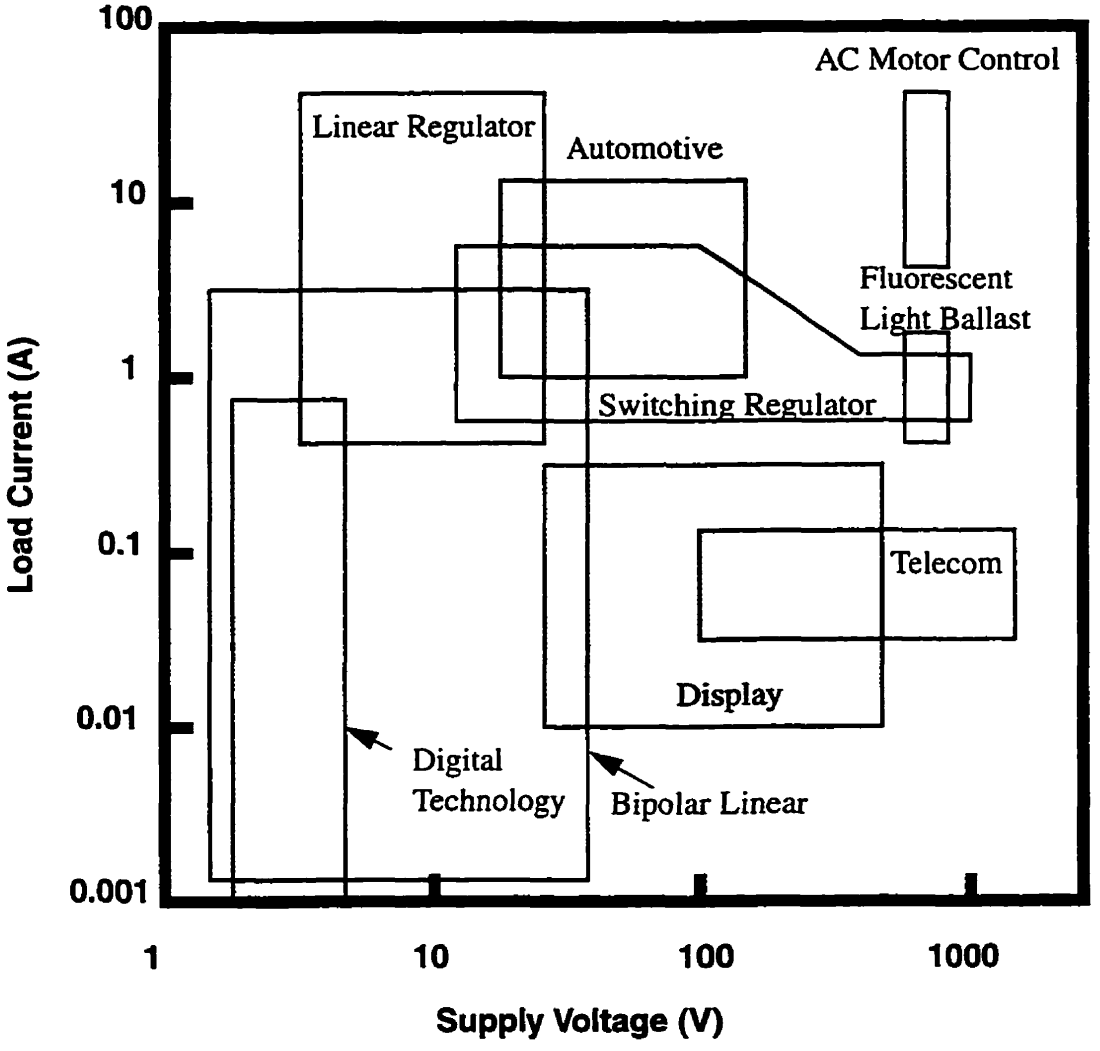

Figure 1.2 Major applications and requirements of PICs

such as higher input impedance and higher switching speed and immunity from second breakdown. However, the conventional MOSFETs suffer from increased on-resistance as the breakdown voltage is increased. As an alternative, the lateral double diffused MOS transistor (LDMOST) has become popular because the device achieves very short channel length due to the double diffused channel and offers an extended drain structure which can be used to increase the breakdown voltage [3].

In recent years, DMOS transistors were further enhanced by the introduction of sub-micron processing to improve current density per unit area.

This thesis deals with DMOS devices which are used in such applications as disc drives, power supplies, and automobiles because of their high switching speed, high input impedance, controllable breakdown voltage and wide safe operating area. Reduction in device specific on-resistance of LDMOST results in huge area savings, which leads to higher die yield and lower cost. In addition, reduced on-resistance reduces power dissipation and increases battery life in portable applications.

A brief discussion of alternative means of designing low on-resistance lateral power MOSFETs with high breakdown voltages is given in the following section.

1.1 Low On-resistance High Breakdown MOSFETs

Efland et al. [4] proposed a low on-resistance lateral power MOSFET which is fabricated using advanced CMOS and BiCMOS process as shown in Figure 1.3. The MOSFET is built on the epitaxial layer which is grown on the p^- substrate. Advances in process technology have improved transistor's packing density by reducing the contact area of the source (L_1) and drain (L_4). The advanced process allows to scale down the gate oxide thickness, successfully reducing the threshold voltage of the device. This not only reduces the channel resistance but also saves power dissipation in driving circuits as

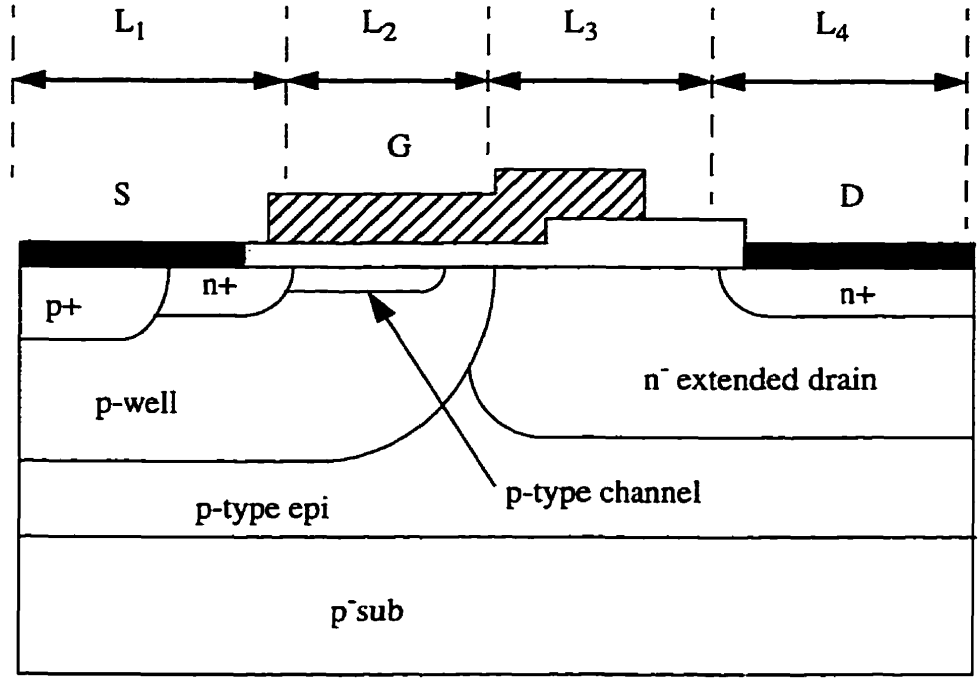

Figure 1.3 Optimized RESURF LDMOST [4]

a result of a reduced gate driving voltage. In addition, RESURFing the devices has resulted in increased charge density in the n^- extended drain. This reduces on-resistance while keeping the breakdown voltage high. A blocking voltage of 97 V and a specific on-resistance of 2.0 $m\Omega\text{-}cm^2$ were achieved.

The device consists of the following four regions shown in Figure 1.3: (1) a source region with a length L_1, (2) a channel region with a length L_2, (3) an extended drain region with a length of L_3 and (4) a drain region with a length of L_4. The pitch of the device is the sum of $L_1+L_2+L_3+L_4$ and that pitch determines the packing density of the device and its specific on-resistance. The smaller the pitch the higher the packing density and the lower the on-resistance per unit area. Present state of the art MOSFETs with a breakdown voltage of 80 V require L_3 to be 3 μm to reduce the electric field near the drain and prevent premature breakdown. The remaining parameters (L_1, L_2, and L_4) do not influence the breakdown voltage significantly and are required to be 1.5 μm, 2 μm, and 1.5 μm respectively for L_1, L_2 and L_4 respectively (for 1 μm minimum design

rules). The length of the n^- extended drain is the largest among all of the regions and must be increased as the breakdown voltage of the MOSFET increases. As a result, the packing density of the MOSFET is sacrificed and on-resistance increases.

Figure 1.4 illustrates another advanced lateral power MOSFET compatible with advanced VLSI processes [5]. A sidewall spacer is effectively introduced in the power MOSFET. First, boron ions are implanted using the polysilicon gate as a mask. Following sidewall spacer formation, arsenic ions are implanted using the sidewall spacer edge as a mask. Resulting in an extremely short channel (0.4 μm). This structure yields a device with a very low channel resistance and a very high transconductance.

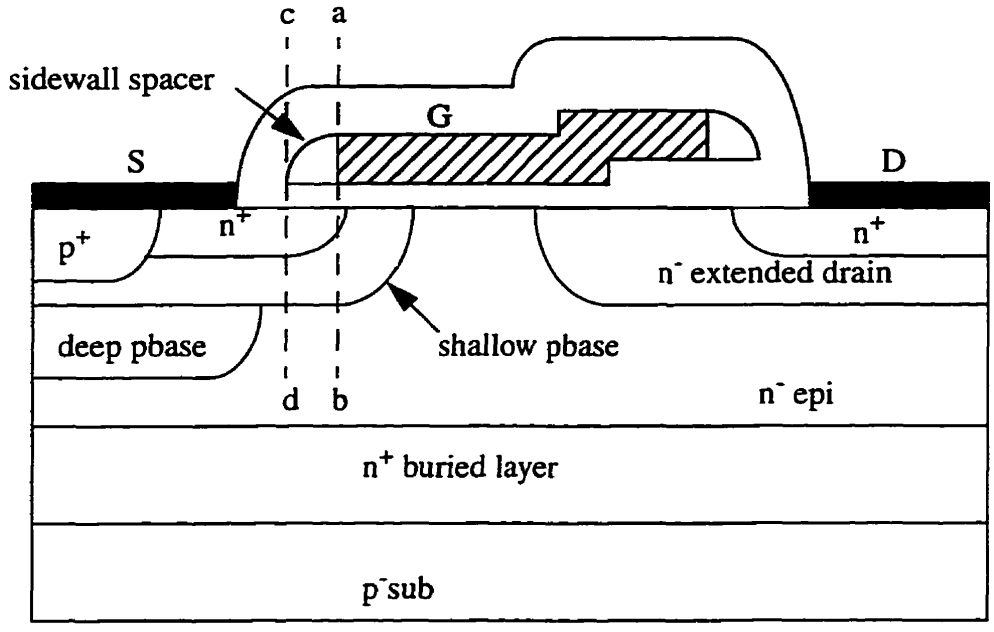

Figure 1.4 LDMOST with oxide sidewall spacer [5]

Both of the previous examples use epitaxial layers which increase production cost. Instead of using an epitaxial layer, Kitamura et al. [6] proposed a lateral DMOST which is self-isolated in a p-type substrate as shown in Figure 1.5. The LDMOST is surrounded by a p well. Due to the charge sharing effect between the p well and the n^- drift region, the breakdown voltage is improved and at the same time a low threshold voltage is obtained to allow a low voltage gate drive. The device achieved a blocking

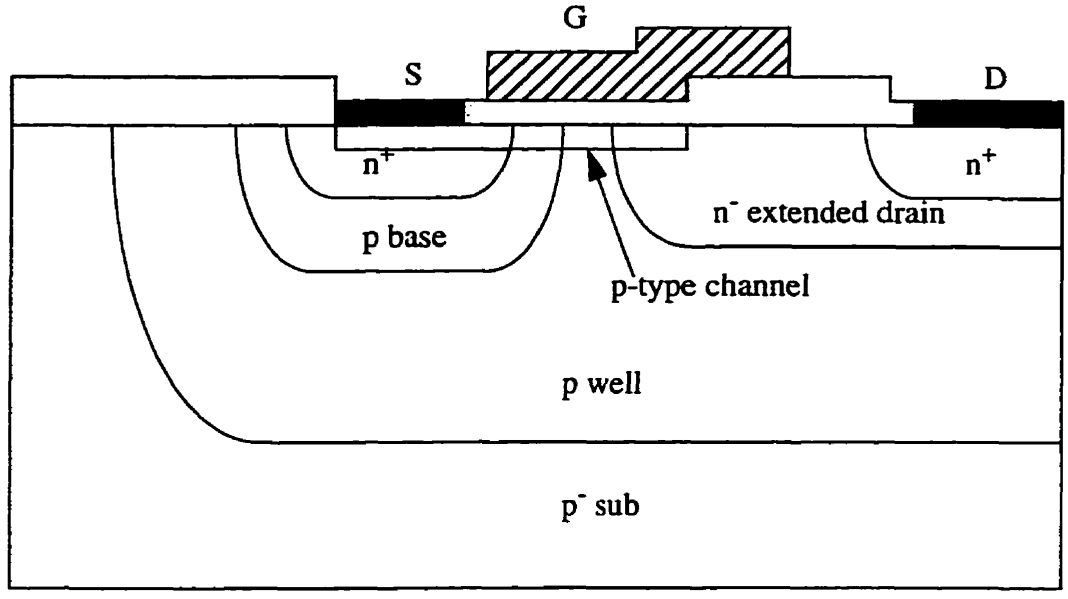

Figure 1.5 LDMOST with surrounding-body region [6]

voltage of 87 V and a specific on-resistance of 1.24 mΩ-cm^2. This technology makes it possible for power ICs to be more inexpensive and to be fabricated within a shorter time.

Improvements in on-resistance have been limited in conventional design geometries (such as the devices in Figures 1.4 and 1.5) because the long extended drain is located horizontally and sacrificing the packing density of the power MOSFETs. In order to avoid this long horizontal drift region, a vertical DMOS (VDMOS), shown in Figure 1.6 was proposed by Hoshi et al. [7]. The vertical thickness between p base and n^+ buried layer determines the breakdown voltage. The device achieved a specific on-resistance of 0.65 mΩ-cm^2 with a breakdown voltage of 36 V. However, a thicker epitaxial layer is needed for devices with higher breakdown voltage resulting in deeper n^+ sinker and causing a reduction of packing density. In addition, the p bases under the gate create JFETs which increase the on-resistance of the device.

Silicon trench technology is widely used for isolation and dynamic memories in VLSI to save silicon real estate. The technology can also be applied to power MOSFETs

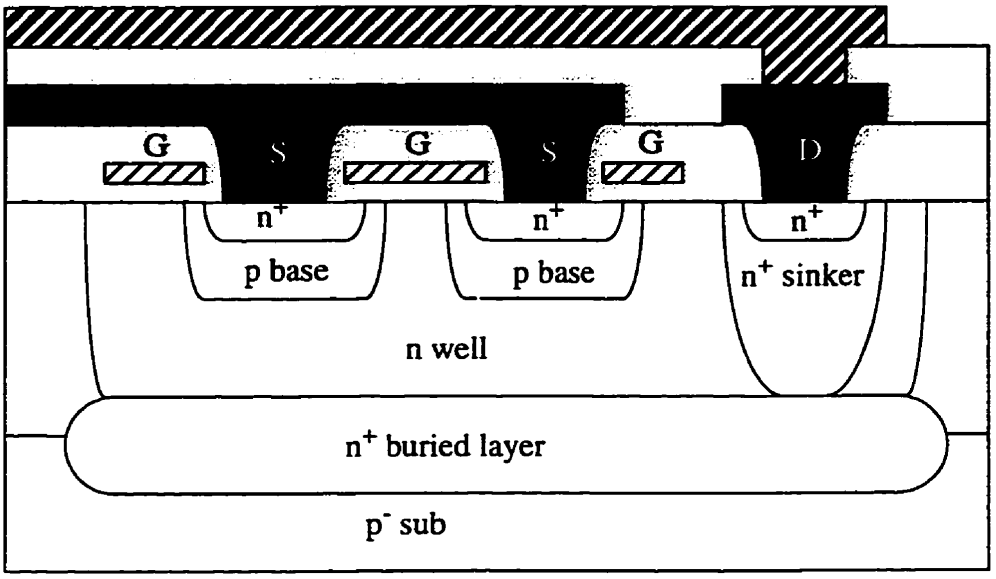

Figure 1.6 Vertical LDMOST with a deep sinker [7]

as proposed (RMOS: Rectangular-grooved MOSFET) by Ueda et al. [8] and shown in Figure 1.7. The gate electrodes in the device are buried inside the trench and the channels are created along the sidewall of the trench. The RMOS reduces the unit cell size and increases channel density and is suitable as a discrete device.

S. Mukherjee, et al. [9] proposed a high current power IC technology that combines

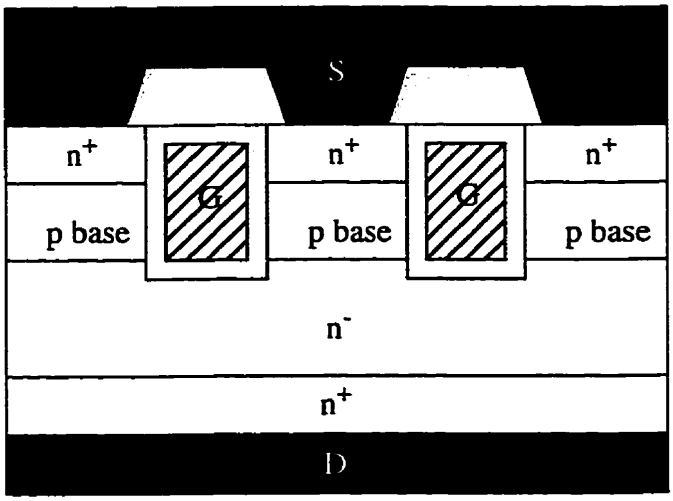

Figure 1.7 Rectangular-grooved MOSFET (RMOS) [8]

trench power DMOST with CMOS control as shown in Figure 1.8. The trench DMOS power device has a breakdown voltage of over 60 V and specific on-resistance of 0.8 $m\Omega\text{-}cm^2$. Although this technology integrates a high performance trench DMOST with low voltage CMOS, the drain of the trench device is located at the back side of the silicon substrate, making it difficult to implement more than one power device on a single chip.

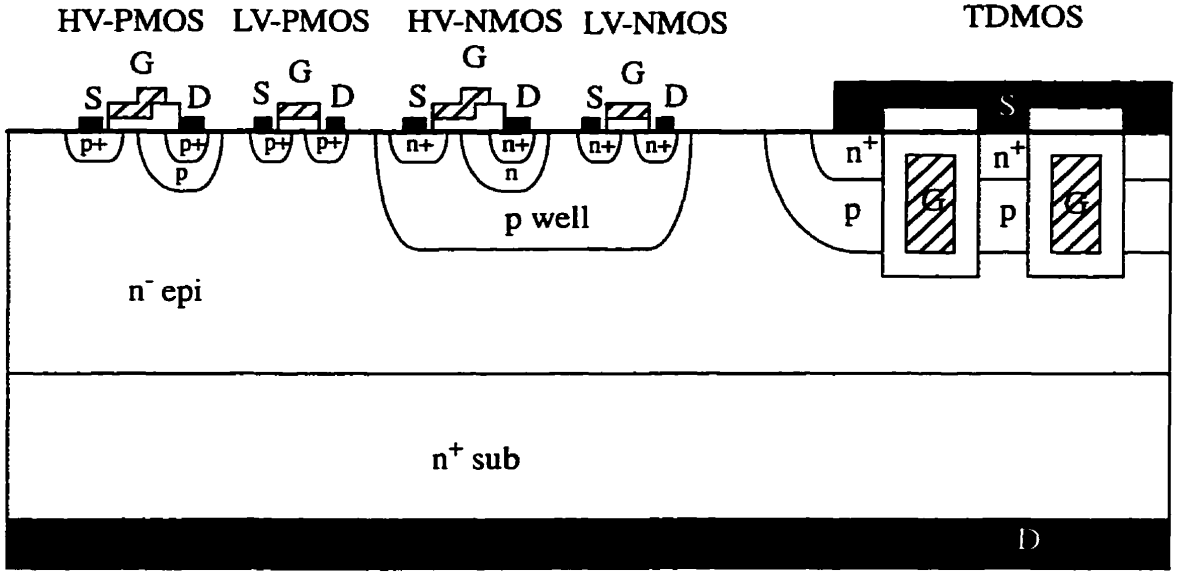

Figure 1.8 Integrated PIC process combining high and low voltage CMOS with trench-DMOST [9]

To overcome the packing density limitation and at the same time to implement multiple power devices in one chip, MOSFETs using trench structures have been proposed by N. Fujishima, et al. [10]. As illustrated in Figure 1.9, a channel and n^- extended drain are located vertically along the sidewall of a trench formed in a substrate. Since the trench MOSFET has n^- extended drain between a source contact and a drain region, and a thick oxide between gate electrode and the drain region, it is possible to optimize the structure to get almost the same current handling capability per unit cell as in the conventional MOSFET without reducing the breakdown voltage. The pitch in this case is determined by the sum of L_1, L_5, and L_6 which have typical values of 1.5 μm, 2

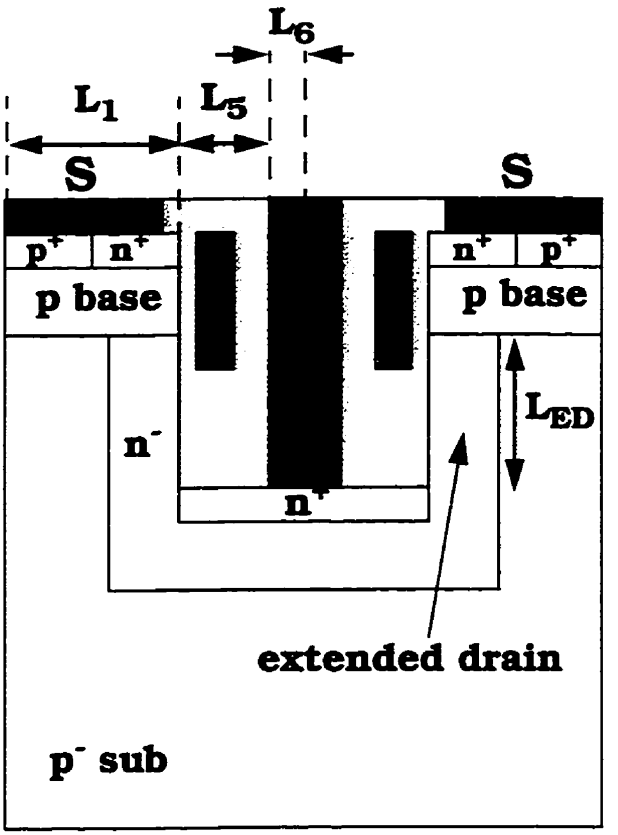

Figure 1.9 Conventional Trench Lateral DMOST [10]

μm and 0.5 μm respectively (for minimum 1 μm design rules) resulting in half the pitch of the conventional structure in Figure 1.3. Therefore, the packing density per unit area of the MOSFET can be increased and a reduction in on-resistance per unit area is achieved. However, two additional masks are needed to define the silicon trench and the drain contact holes in the illustrated structure. The resulting process also requires strict alignment tolerance between the two masks. In addition, two deep directional etching steps are needed to define the gate and the drain contact hole inside the initial silicon trench.

1.2 Thesis Objective and Organization

In view of the above, it is an objective of this thesis to propose a lateral DMOST incorporating a high packing density trench structure and offering high breakdown

voltage with low on-resistance and to describe a method of manufacturing and realizing that device. [11-13].

In Chapter 2, the device structure and the fabrication process are described and the device layout is discussed.

In Chapter 3, two dimensional process and device simulations to predict the electrical performance of the proposed device are presented and experimental results are reported.

Chapter 4 concludes the thesis and presents suggestions for future work.

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CHAPTER 2

Device Structure and Fabrication Process

2.1 Introduction

The objectives of this thesis were presented in Chapter 1 together with a discussion of previous approaches to the lateral power MOSFETs. In order to achieve further reduction of on-resistance, a trench structure is introduced to increase the cell density in the MOSFET thus increasing the current handling capability. In this work, an 80 V class MOSFET is designed. Such devices are widely used in a large number of applications, such as automotive and power management systems, where demand for improvement in the performance of the power MOSFETs is quite high.

In this chapter, the device structure of the proposed Trench Lateral Power MOSFET (TLPM) is described. Then, operation of the device and specific requirements for the device structure are presented. Following this, the fabrication process is demonstrated. Since it is quite important to simplify the fabrication procedure, self-aligned methods are chosen for the gate formation and the bottom trench contact hole opening. The specific values for the detailed condition for the process steps and geometrical parameters are selected as a result of process and device simulation calculations. Finally, the layout design to optimize the TLPM is discussed at the end of this chapter.

2.2 Device Structure

A top view and cross-sectional view of the proposed Trench Lateral Power MOSFET are shown in Figure 2.1 and 2.2. In order to realize a wider channel and increase the

current handling capability of the device, a source and a drain having an interdigitated geometry are provided as shown in Figure 2.1 The cross-section of the active area (along the line A-B in Figure 2.1) is shown in Figure 2.2 (a). The MOSFET has its channel region

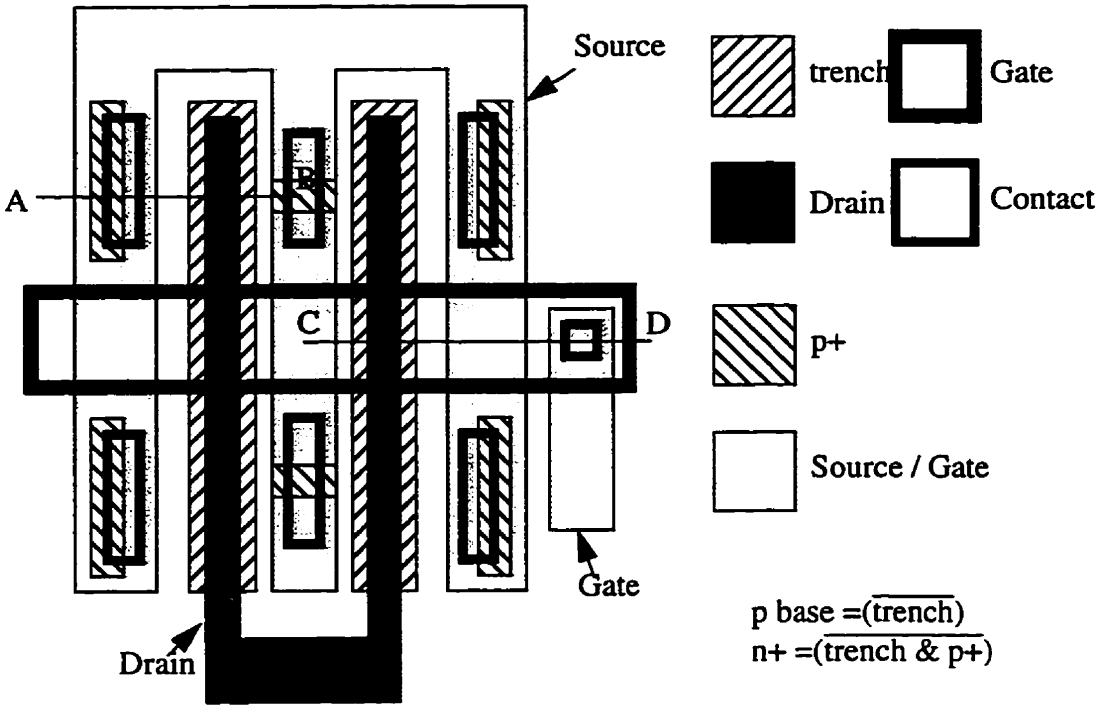


Figure 2.1 Top view of the TLPM

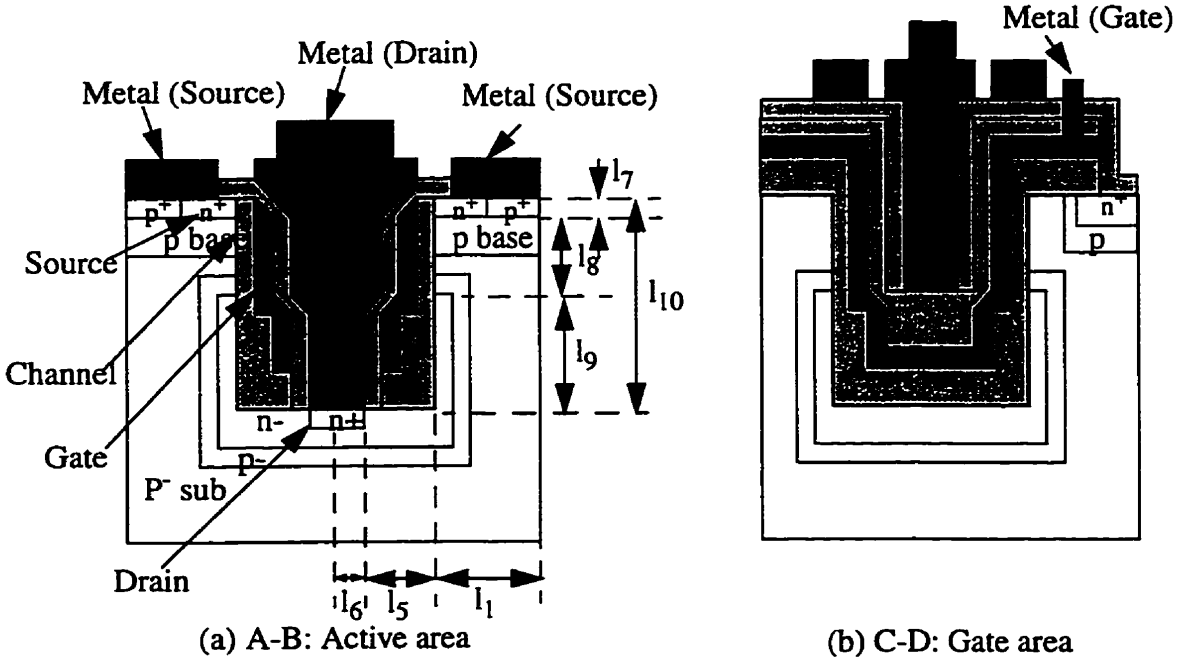


Figure 2.2 Cross-section of the TLPM

along the sidewall of the trench, with the source at the top of the trench and the drain at the bottom of the trench. The trench itself extends from the top surface of the substrate to a defined depth. The gate oxide is formed at the upper side of the sidewall. A thicker oxide is provided on the lower part of the sidewall and at the bottom of the trench. The n^- extended drain region is surrounded by a p body diffused region and both are implemented through a window defined by the sidewalls and the bottom of the trench as will be described in greater detail in the following paragraph. When the impurity profile between the p body diffusion region and n^- extended drain are optimized, the MOSFET exhibits a low on-resistance and a high breakdown voltage. The drain contact hole is completely filled with polysilicon to access the drain contact from the surface of the wafer.

When a positive potential higher than the threshold voltage is applied to the gate electrode, an inversion layer is created along the sidewall of the trench in the p base region, the created channel allows electron current to flow vertically from the source to the drain at the bottom of the trench. The current in the drain is collected through the drain at the bottom of the trench. The current in the drain is collected through the drain electrode and the polysilicon plug connecting the n^+ drain to the electrode.

The (100) silicon plane is used to implement the device by orienting the main side-wall plane in the trench 45 ° away from the <110> axis of the (100) orientation wafer resulting in very high electron mobility in the channel [1]. In addition, the current in the n^- extended drain flows mainly in the bulk, instead of at the surface, thus avoiding mobility degradation due to damage associated with trench formation.

In this structure, the gate oxide thickness is chosen to be 0.1 μm which is suitable for realizing a stable gate oxide with a breakdown voltage of more than 30 V, as well as for obtaining a threshold voltage of approximately 1 - 2 V. The thick oxide at the bottom of the trench is provided to reduce the electric field under the gate near the drain. For a blocking capability of 80 V, a thickness of no less than 0.5 μm is required for the thick

oxide. In addition, the channel region and the n^- extended drain need to be long enough to achieve the required breakdown voltage.

The vertical length of the source l_7 needs to be 1 μm to guarantee overlap between the source and the gate. For an 80 V MOSFET, the channel length l_8 needs to be 2 μm and the length of the extended drain l_9 needs to be 3 μm. Hence l_{10} is 6 μm. However, since the structure is vertical, these dimensions do not affect the device pitch which is determined by half the contact opening at the drain l_6, the lateral distance l_5 between the edge of the drain and the edge of the source and the length l_1 of the source region. For a 1 μm minimum design rule, $l_6 = 0.5$ μm, $l_5 = 2$μm, $l_1 = 1.5$ μm resulting in a device pitch of 4 μm which is half the value of the pitch in the conventional MOSFET of Figure 1.3 [2].

Figure 2.2 (b) shows a cross-section of the gate area coupled to a gate electrode at the surface (along the line C-D in Figure 2.1). The polysilicon gate is expanded from inside the trench. Drain contact holes are not created in this area.

2.3 Fabrication Process

The process flow of the Trench Lateral Power MOSFET (TLPM) will be described with reference to Figure 2.3, which includes the cross sections of each step for the active area and the gate area. The detailed description of the process condition is summarized in Table 2.1. First, a 1.8 μm thermal oxide film is grown on the p^- substrate and then selectively etched using photolithography (first mask). The oxide film is then etched by RIE using photoresist as a mask. In this RIE step, etching must be carefully performed so as to prevent photoresist from burning out. The silicon substrate is then etched by RIE [3] to form a trench then the etched surface is wet etched removing a 0.1 μm surface layer to eliminate the damage caused by RIE, resulting in the structure as illustrated in Figure 2.3 (a). Following this step, the growth of a 0.1 μm pad oxide is carried out. Throughout the whole process, thermal oxide is grown at a temperature of 1100 °C so as to minimize

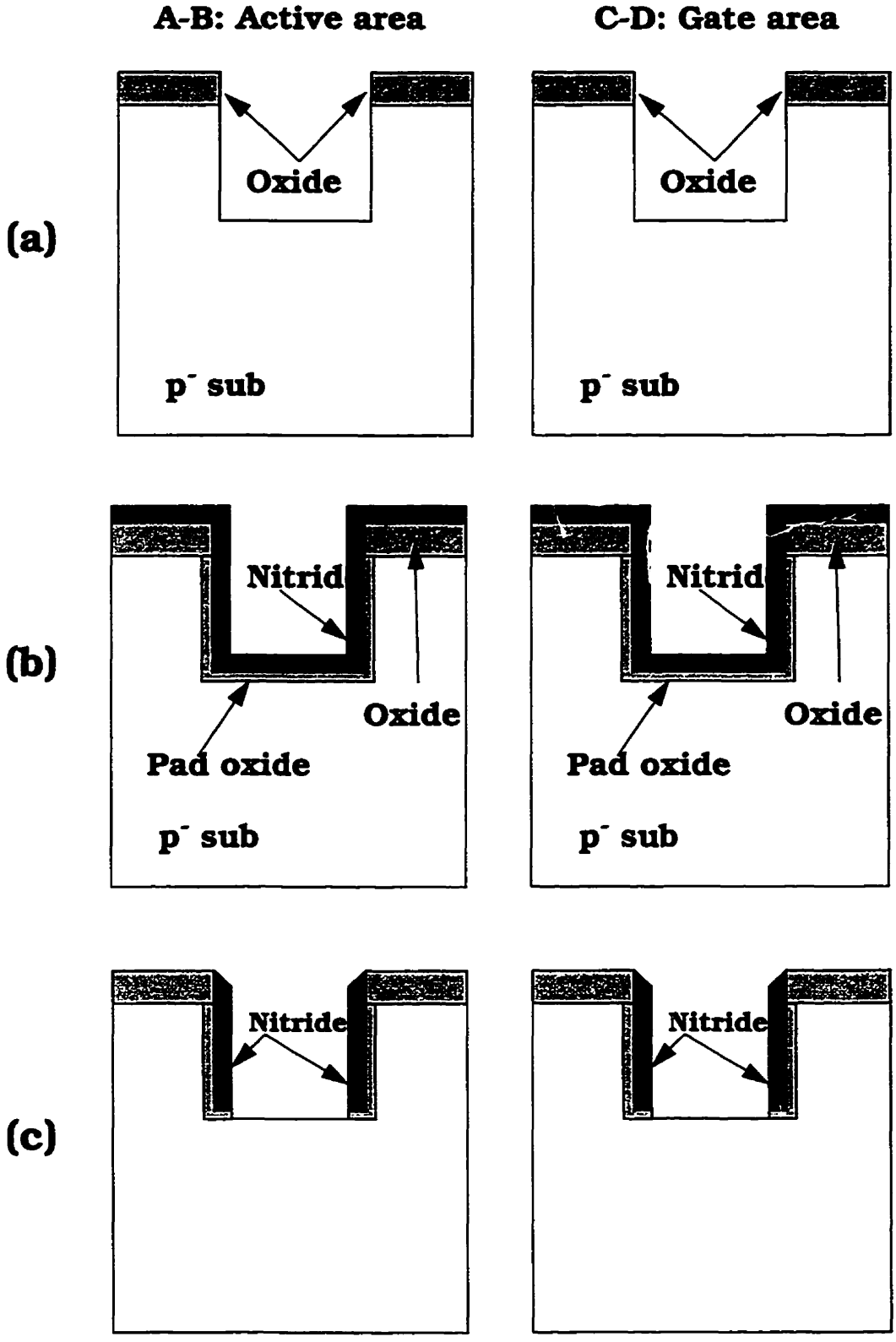


Figure 2.3 TLPM processing steps

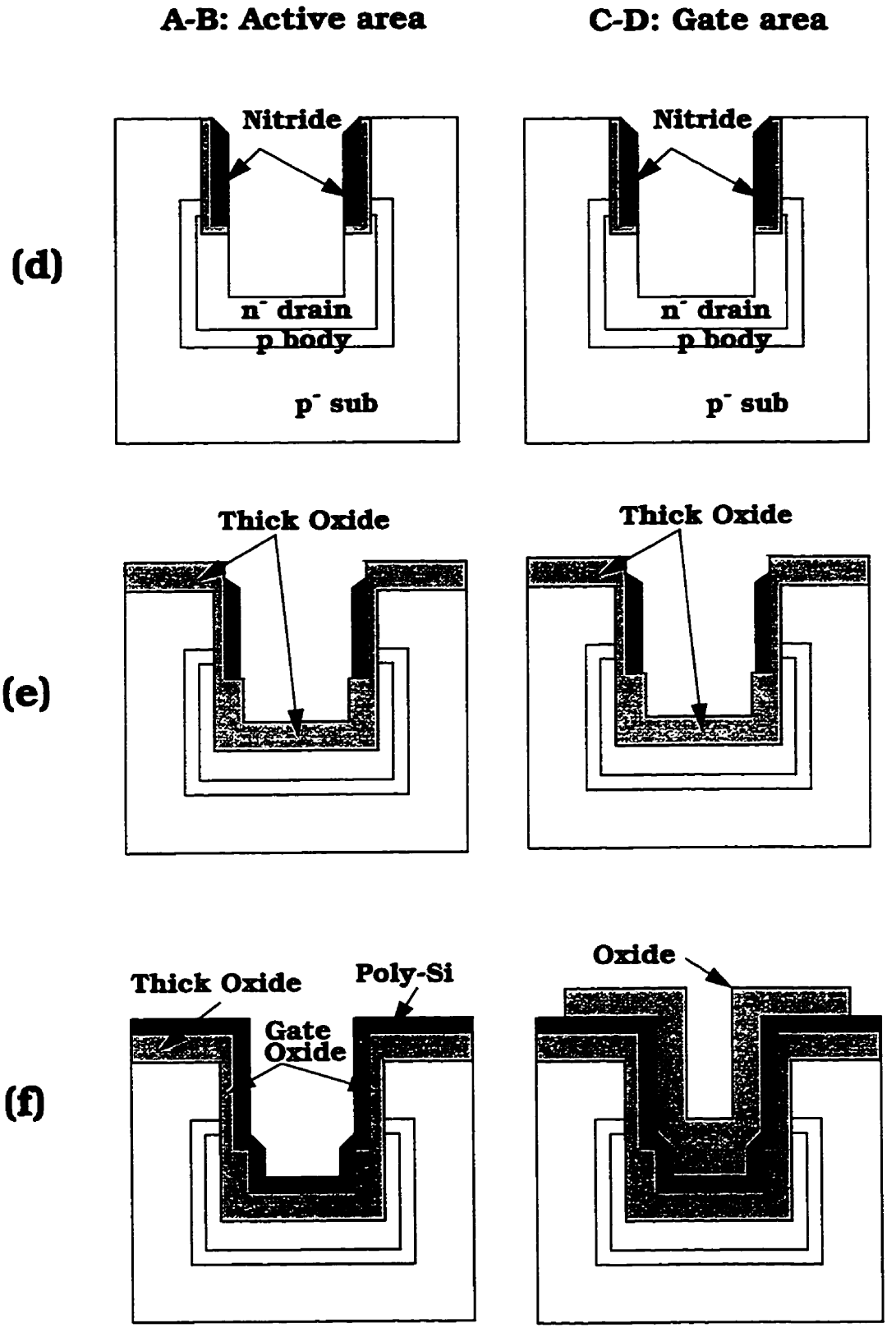
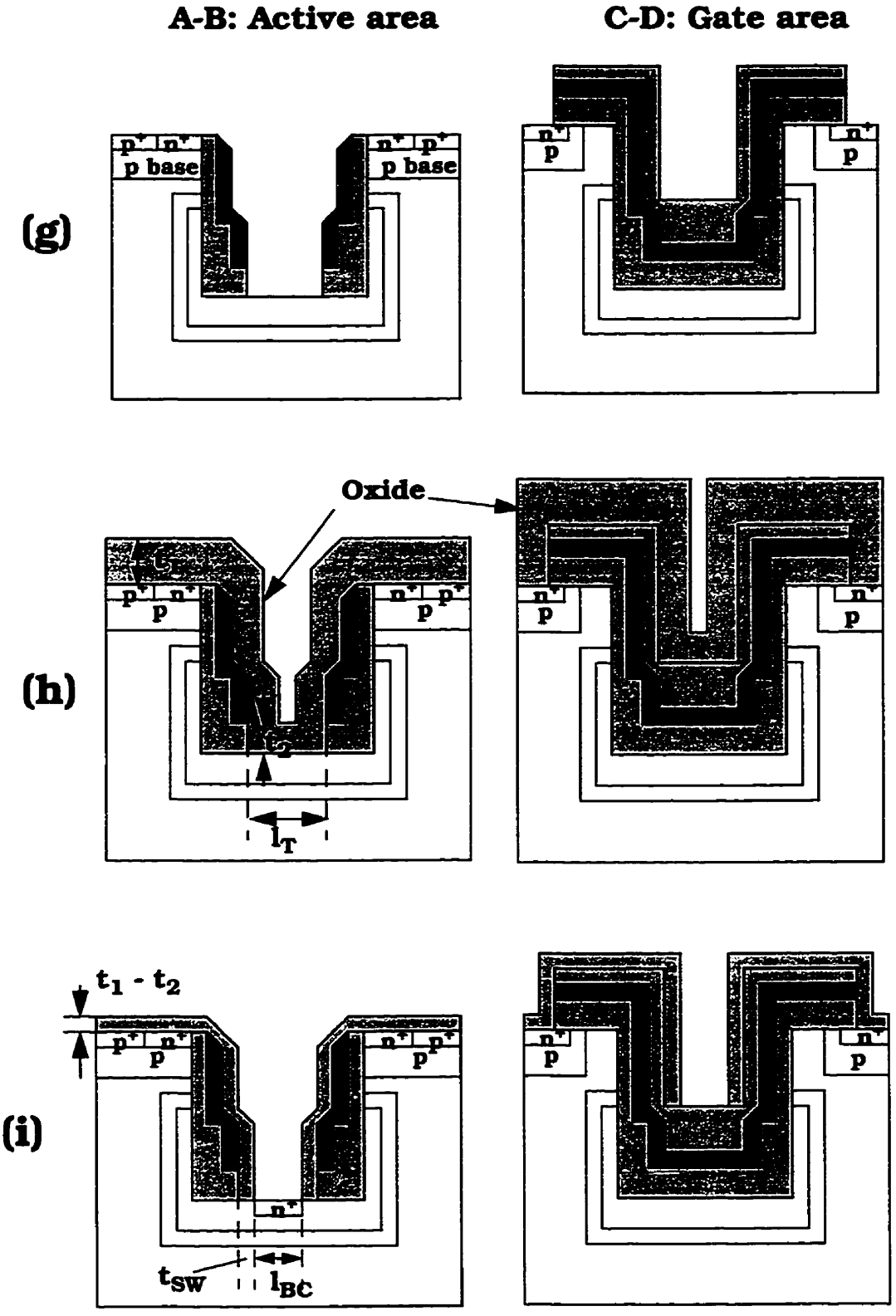


Figure 2.3 TLPM processing steps (continued)



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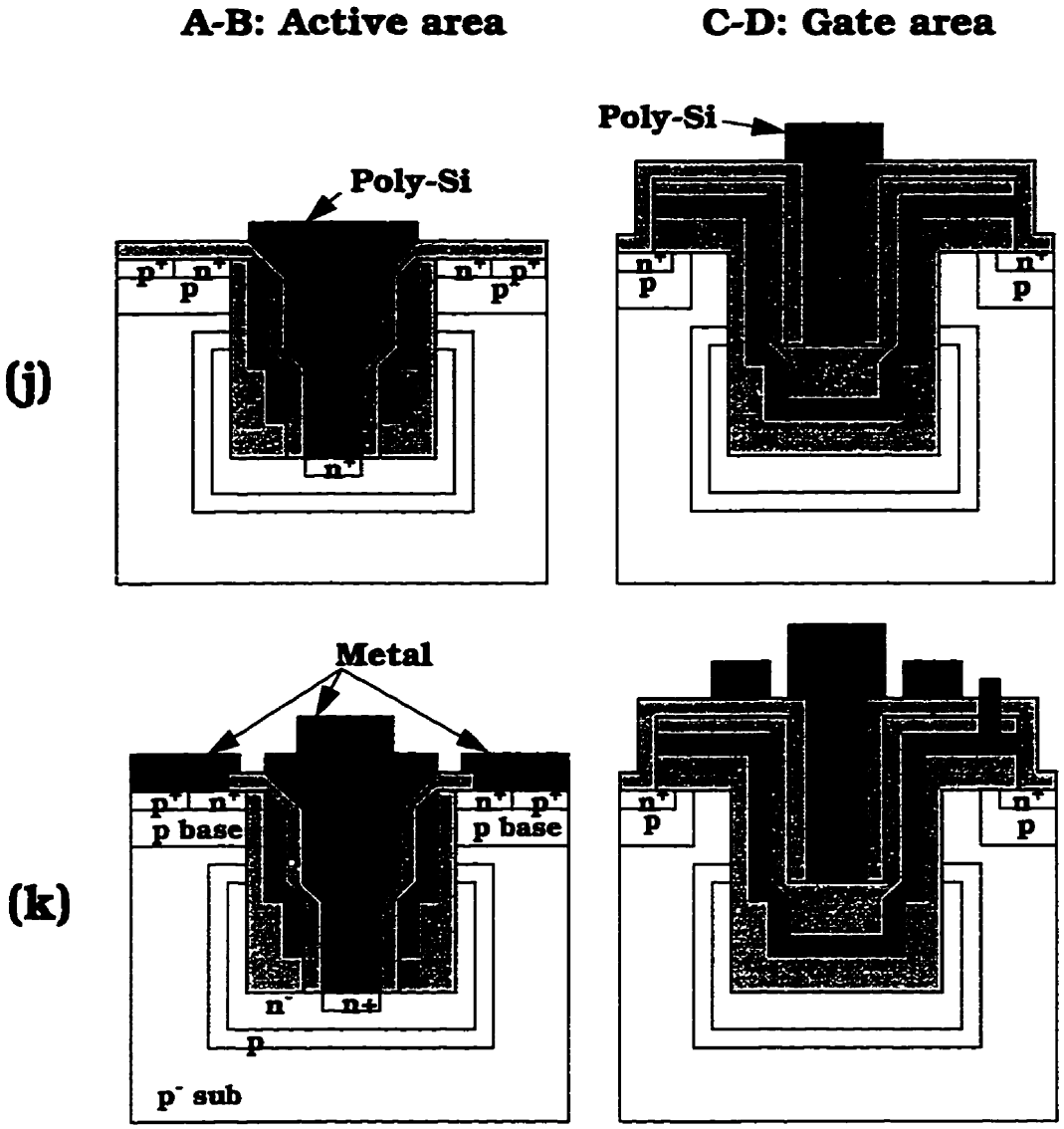

Figure 2.3 TLPM processing steps (continued)

stress which induces dislocation in the silicon substrate [4]. Then, a silicon nitride layer with a thickness of 0.4 μm is deposited on the pad oxide as shown in Figure 2.3 (b), and etched by RIE to leave residual portions of the nitride layer on the sidewall of the trench as shown in Figure 2.3 (c). Thereafter, the silicon substrate is etched by RIE once again to extend the depth of the trench past the residual nitride layer. In order to remove the damage caused by RIE and make a recessed silicon on the sidewall, silicon wet etching is performed and approximately 0.3 μm of silicon layer is removed. After 0.03 μm of oxide is grown to prevent channeling, tilted ion-implantation of boron is performed on the sidewalls of the trench. Each implantation injects a dose of 8×10^{12} cm^{-2} at a tilted angle of 15 ° with the substrate rotated at 0°, 90°, 180° and 270 ° to provide ions into the four individual sidewalls. Then the boron is driven into substrate to create the p body. Next, tilted (15 °) ion-implantation of phosphorus is performed. Each implantation injects a dose of 2×10^{13} cm^{-2} with the substrate rotated at 0°, 90°, 180° and 270 ° to provide ions into the four individual sidewalls. Then the phosphorus is annealed to create the n^- extended drain. This step is followed by wet etching removal of the oxide as shown in Figure 2.3 (d). Wet oxidation is carried out for 100 minutes to grow a thick oxide layer of 0.8 μm at the surface of the substrate, at the lower part of the sidewall and at the bottom of the trench, where nitride is not present, as shown in Figure 2.3 (e). Thereafter, the residual nitride and the pad oxide are removed by using wet etching. Further wet oxide etching is performed and another 0.3 μm of oxide is removed to level the sidewall. Then a sacrificial oxide is thermally grown at 1100 °C and the oxide is removed by wet etching (0.1 μm thick) in order to clean the sidewall for the following gate oxidation. A gate oxide is then thermally grown in a O_2 + 2% HCl atmosphere and doped polysilicon with a thickness of 0.6 μm is deposited by LPCVD. This step is followed by the deposition of a 1.6 μm oxide layer by LPCVD. The oxide layer at the top is selectively etched using the second mask to define the actual gate region as shown in Figure 2.3 (f). The photolithography in this step is used to define the gate running across the silicon trench which has a depth of approxi-

mately 6 μm. First, photoresist* (6 μm) is deposited to completely fill the trench. Then a first exposure using the second mask is performed with an exposure time of 10 minutes. Additional mask alignment is carried out using the second mask again. Here, the exposure time is chosen to be 3 minutes. Following this step, combination of wet and dry etching is performed to remove the oxide selectively and the photoresist is removed.

Next, the polysilicon layer is etched by RIE using the oxide as a mask. The thick oxide under the polysilicon is then etched using RIE and the silicon is bare at the surface and at the bottom of the trench. On the other hand, residual portions of the polysilicon and the thick oxide are left on the sidewall. During this etching step, the oxide mask on the polysilicon is also etched at the same etching rate as the oxide under the polysilicon.

After 0.03 μm layer of oxide is then deposited by LPCVD, boron is selectively implanted using the third mask and the boron is annealed at 1100 °C for 100 minutes to form the p base. This step is followed by formation of the n^+ and p^+ regions on the surface using the fourth and fifth masks, respectively, as shown in Figure 2.3 (g). Phosphorus is used for the ion-implantation of the n^+ region, where the dose and the energy are 5×10^{15} cm^{-2} and 130 KeV, respectively. Boron is used for the ion-implantation of the p^+ region where the dose and the energy are 5×10^{15} cm^{-2} and 50 KeV, respectively. The implants are driven in at 1100 °C for 15 minutes.

An oxide layer with a thickness of 2 μm is then deposited by LPCVD as shown in Figure 2.3 (h). Because the reactants do not migrate rapidly along the surface at the temperature used for the LPCVD, the thickness t_2 of the oxide inside the trench is thinner than the thickness of the oxide t_1 at the surface of the substrate ($t_2 < t_1$) [5].

A 1.3 μm thickness of oxide is etched by using RIE so as to create a contact hole at the bottom of the trench as shown in Figure 2.3 (i). Since RIE has strong directional etch-

* Shipley Microposit 1350J positive photoresist

ing properties, the oxide film at the bottom of the trench is completely removed and the surface of the silicon substrate is exposed. On the other hand, the oxide on the sidewalls and the top surface is retained and is thick enough to provide good electrical isolation between the gate and the drain.

An n^+ region is then formed at the bottom of the trench by ion-implantations as shown in Figure 2.3 (i). Here, two arsenic ion-implantations with a dose of 5×10^{15} cm^{-2}, energy of 50 KeV and a tilted angle of 7 ° are carried out by rotating the substrate at 0° and 180 °.

Thereafter, a doped polysilicon layer is deposited to fill the trench and patterned so as to obtain a drain electrode using the sixth mask as shown in Figure 2.3 (j). Then, the doped polysilicon and n^+ region at the bottom of the drain are annealed using RTA at 1100 °C for 1 minute. One purpose of the RTA in this step is to break up of the native oxide layer into small oxide islands to achieve a good contact between the drain polysilicon and the n^+ drain underneath [6]. Another purpose is to reduce the resistivity of the polysilicon by annealing [6].

Thereafter, RIE etching is used to open contact windows at the surface of the source region and the gate electrode using the seventh mask. The surface metal is deposited and finally the source, the drain and the gate electrodes are defined by using the eighth mask as illustrated in Figure 2.3 (k)

Table 2.1 TLPM process summary

Step	Process
Starting material	(100) p-type, 18 Ω-cm, boron doped primary flat (100)
Oxidation for trench mask	1100 °C, 600 min., wet O_2
Trench photolithography (Mask #1)	Oxide RIE etch, time = 19 min. Oxide wet etch, time = 1 min.
Photo resist removal	
Silicon trench formation	Silicon RIE etch, time = 23 min. Silicon wet etch, time = 20 min.
Pad oxidation	1100 °C, 60 min., dry O_2
Nitride deposition	0.3 μm CVD nitride
Nitride formation on the sidewall	Nitride RIE etch, time = 4 min. Pad oxide RIE etch, time = 2 min.
2nd silicon trench formation	Silicon RIE etch, time = 13 min. Silicon wet etch, time = 30 min.
P body implant	1100 °C, 7 min., dry O_2 (0.03 μm oxide) Boron dose = 8×10^{12} cm^{-2} each Energy = 50 KeV Tilt = 15°, rotation = 0°, 90°, 180°, 270° (Total boron dose = 3.2×10^{13} cm^{-2})
P body drive	1100 °C, 70 min., N_2
N^- drain implant	Phosphorus dose = 2×10^{13} cm^{-2} each Energy = 130 KeV Tilt = 15°, rotation = 0°, 90°, 180°, 270° (Total phosphorus dose = 8×10^{13} cm^{-2})
N^- drain drive	1100 °C, 30 min., N_2
Oxide mask removal	Oxide wet etch, time = 1 min.
Field oxidation	1100 °C, 100 min., wet O_2
Nitride removal	Oxide wet etch, time = 1 min. Nitride wet etch, time = 250 min. Oxide wet etch, time = 2.5 min.
Sacrificial oxidation	1100 °C, 7 min., dry O_2
Sacrificial oxide removal	Oxide wet etch, time = 50 sec.

Table 2.1 TLPM process summary

Step	Process
Gate oxidation	1100 °C, 40 min., dry O_2 2% HCl
Doped polysilicon deposition	0.6 μm CVD doped polysilicon
CVD oxide deposition	1.6 μm CVD undoped oxide
Gate photolithography (Mask #2)	Oxide wet etch, time = 7.5 min. Oxide RIE etch, time = 15 min. Oxide wet etch, time = 15 sec.
Photo resist removal	
Polysilicon formation on the sidewall	Polysilicon RIE etch, time = 6 min.
Oxide formation on the sidewall	Oxide RIE etch, time = 14 min. Oxide wet etch, time = 10 sec. Polysilicon wet etch, time = 1 min.
Oxidation for implant	1100 °C, 7 min., dry O_2 (0.03 μm oxide)
P base photolithography (Mask #3)	
P base implant	Boron dose = 4×10^{14} cm^{-2} Energy = 50 KeV
Photo resist removal	
P base drive	1100 °C, 50 min., N_2
N^+ source photolithography (Mask #4)	
N^+ source implant	Phosphorus dose = 5×10^{15} cm^{-2} Energy = 130 KeV
Photo resist removal	
P^+ photolithography (Mask #5)	
P^+ implant	Boron dose = 5×10^{15} cm^{-2} Energy = 50 KeV
Photo resist removal	
N^+ source drive	1100 °C, 15 min., N_2
CVD oxide deposition	2 μm CVD undoped oxide
Drain contact hole opening	Oxide RIE etch, time = 18 min.
CVD oxide deposition	0.03 μm CVD undoped oxide

Table 2.1 TLPM process summary

Step	Process
N^+ drain implant	Arsenic dose = 5×10^{15} cm^{-2} each Energy = 80 KeV Tilt = 7° rotation = 0°, 180 ° (Total arsenic dose = 1×10^{16} cm^{-2})
Oxide removal	Oxide wet etch, time = 40 sec.
Doped polysilicon deposition for plugged drain	0.7 μm CVD doped polysilicon
Drain polysilicon implant	Arsenic dose = 5×10^{15} cm^{-2} Energy = 80 KeV
Polysilicon anneal	RTA anneal, 1100 °C, 1 min., N_2
CVD oxide deposition for implant	0.03 μm CVD undoped oxide
Drain polysilicon photolithography (Mask #6)	
Polysilicon drain formation	Oxide RIE etch, time = 1 min. Polysilicon RIE etch, time = 6 min.
Photo resist removal	
Contact photolithography (Mask #7)	
Contact hole opening	Oxide RIE etch, time = 16 min. Oxide wet etch, time = 30 sec.
Photo resist removal	
Oxide removal	Oxide wet etch, time = 80 sec.
Metallization	1.2 μm sputtering aluminum
Metal photolithography (Mask #8)	Etch in phosphoric/nitric acid mixture, time = 2.5 min.
Metal anneal	450 °C, 25 min. forming gas

2.4 Mask Layout

The process uses a 1-μm minimum line width photolithography. Two typical device layout patterns for the TLPMs are presented in Figures 2.4 and 2.5. A TLPM layout with a smaller channel width is shown in Figure 2.4. The device has an interdigitated surface geometry which consists of two trenches with a width of 3 μm are drawn. The channel width of the device is 116 μm and the active area is 1,856 μm^2. The gate is located across the trenches.

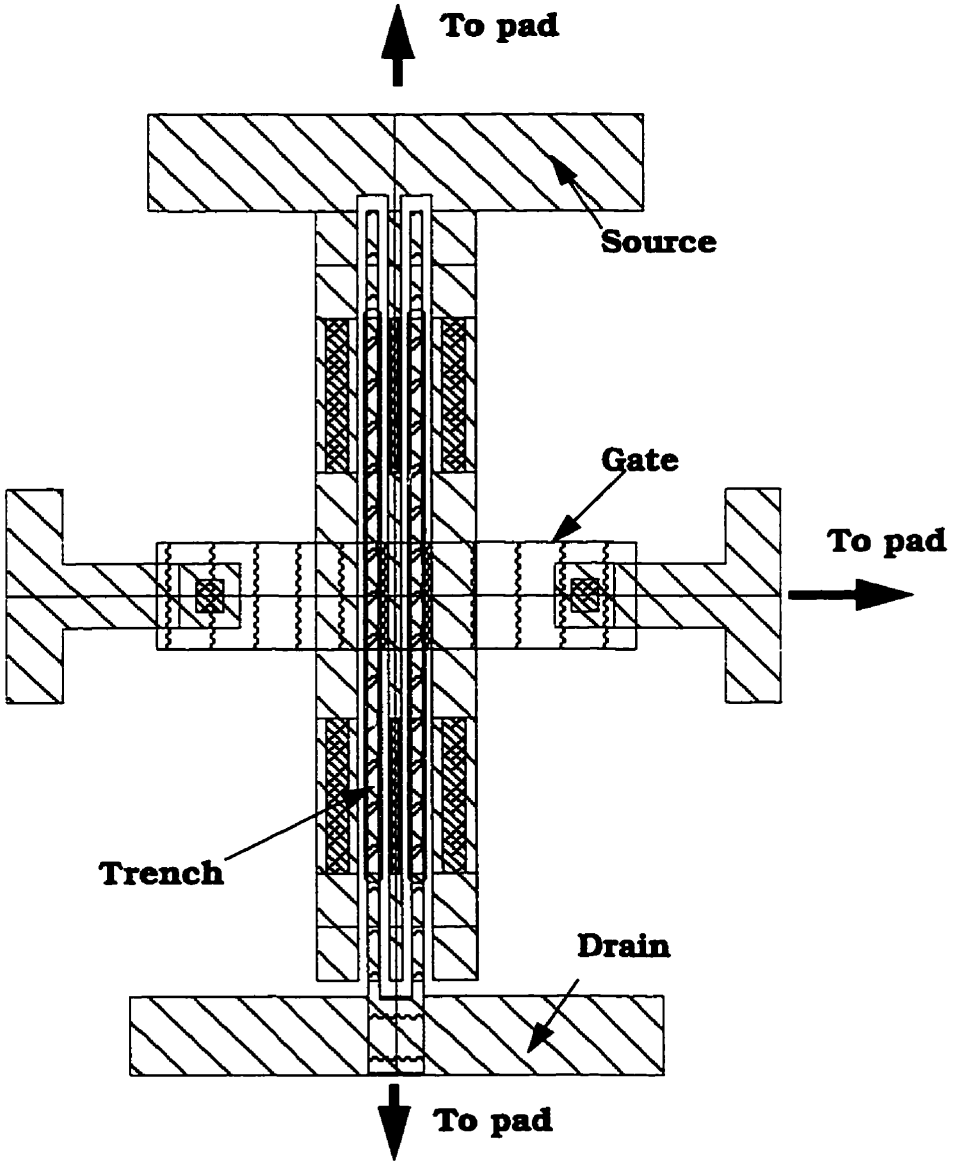

Figure 2.4 TLPM device layout (small channel width W=116 μm)

A TLPM layout with a larger channel width (and higher current handling capability) is illustrated in Figure 2.5. Thirty four stripes of trench are included. The channel width is 11,832 μm and the active area is 47,328 μm^2.

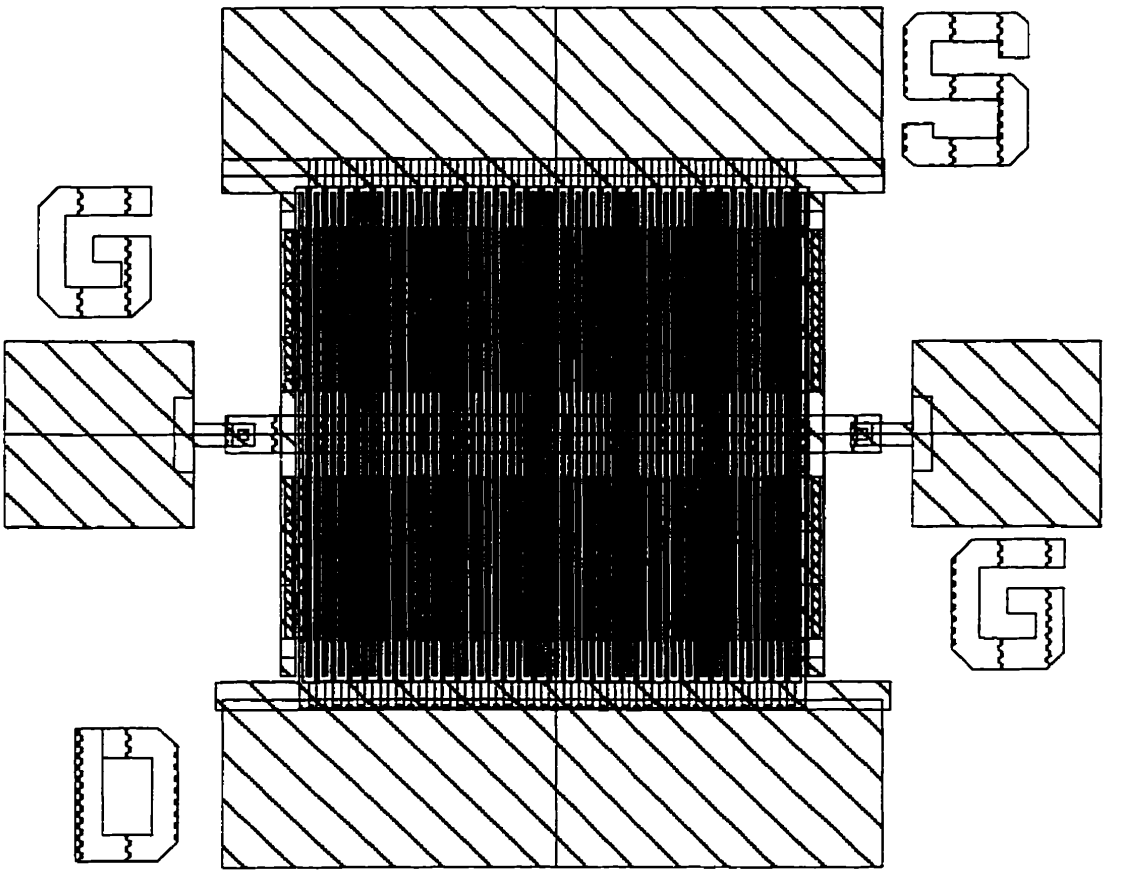

Figure 2.5 TLPM device layout (large channel width W=11,832 μm)

2.5 Summary

A novel Trench Lateral Power MOSFET (TLPM) was proposed. This device is formed along the sidewalls of a trench defined in the silicon. The p body and n^- extended drain, which are formed on the lower side of the sidewall, are used to optimize the trade-off between the on-resistance and the breakdown voltage. The thick oxide on the lower side of the sidewall reduces the electric field in the n^- extended drain, increasing break-

down voltage. Since the channel and the n^- extended drain are located vertically along the sidewall, the packing density of the TLPM is maximized.

Fabrication process steps for the TLPM were proposed using an eight mask process. The process effectively combines LPCVD deposition and RIE etching to form residual films on the sidewall of the trench, creating a thick oxide on the lower side of the sidewall, and forming a gate electrode. In addition, the process utilizes a property of oxide deposition by LPCVD where the deposition rate of oxide inside the trench is approximately half of that on the surface. The process results in a very small spacing between the source and the drain and can be used to form the gate electrodes and the drain contact holes which are self-aligned to the silicon trench, minimizing cell pitch and hence reducing specific on-resistance while keeping the breakdown voltage high.

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CHAPTER 3

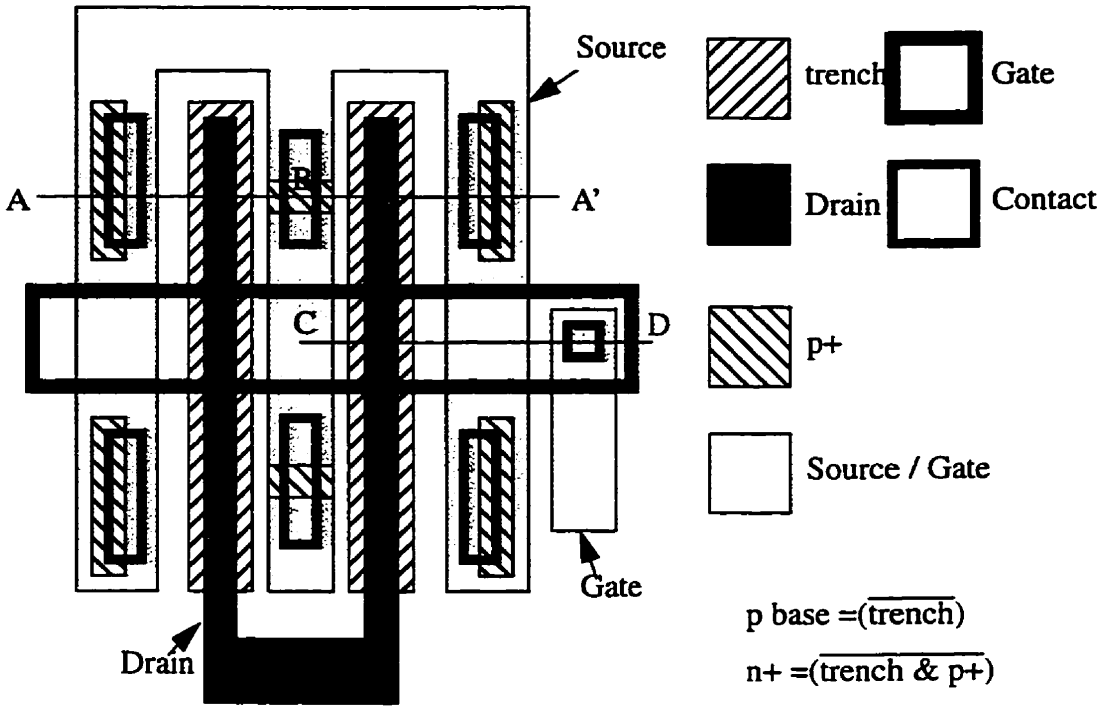
Simulation and Experimental Results

3.1 Introduction

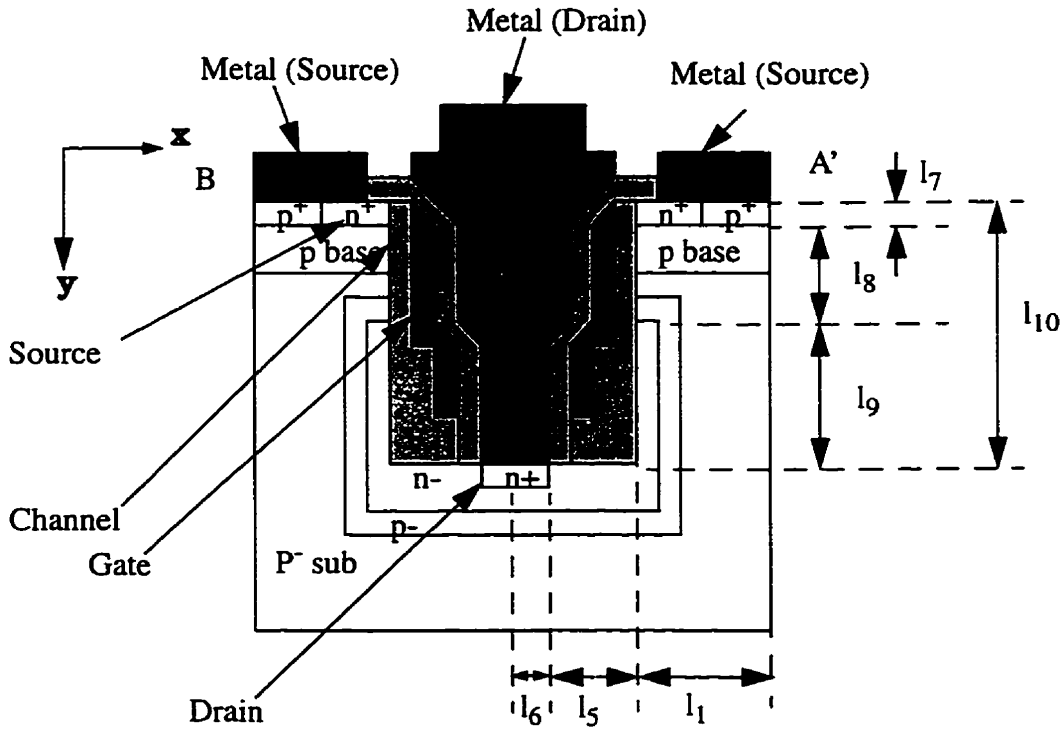
This chapter deals with the evaluation of the proposed Trench Lateral Power MOSFET (TLPM) using two-dimensional simulation and experimental results. Following process simulation to verify the processing steps for the TLPM, the electrical characteristics of the device are demonstrated to illustrate the trade-off between specific on-resistance and breakdown voltage. The TLPM is then compared to a Conventional Lateral Power MOSFET (CLPM) in terms of on-resistance and breakdown voltage using 2-D process and device simulations. Thereafter, experimental work to demonstrate the feasibility of the proposed TLPM process is presented. Finally, conclusions regarding the simulation and experimental results are presented.

3.2 Process Simulation

A 2-D process simulator TSUPREM4 [1] was used to simulate the processing steps for the TLPM. A top view along with a cross section of the device are shown in Figure 3.1. The simulations were carried out for the cross section along the line B-A'. A simulation across the active region is illustrated in Figure 3.2. The n^+ source is formed at the surface of the trench. The n^+ drain is located at the bottom of the trench. The gate oxide is formed at the upper side of the sidewall. The thick oxide is formed on the lower side of the



(a) Top view of TLPM



(b) B-A': Active area

Figure 3.1 Simulated structure for TLPM

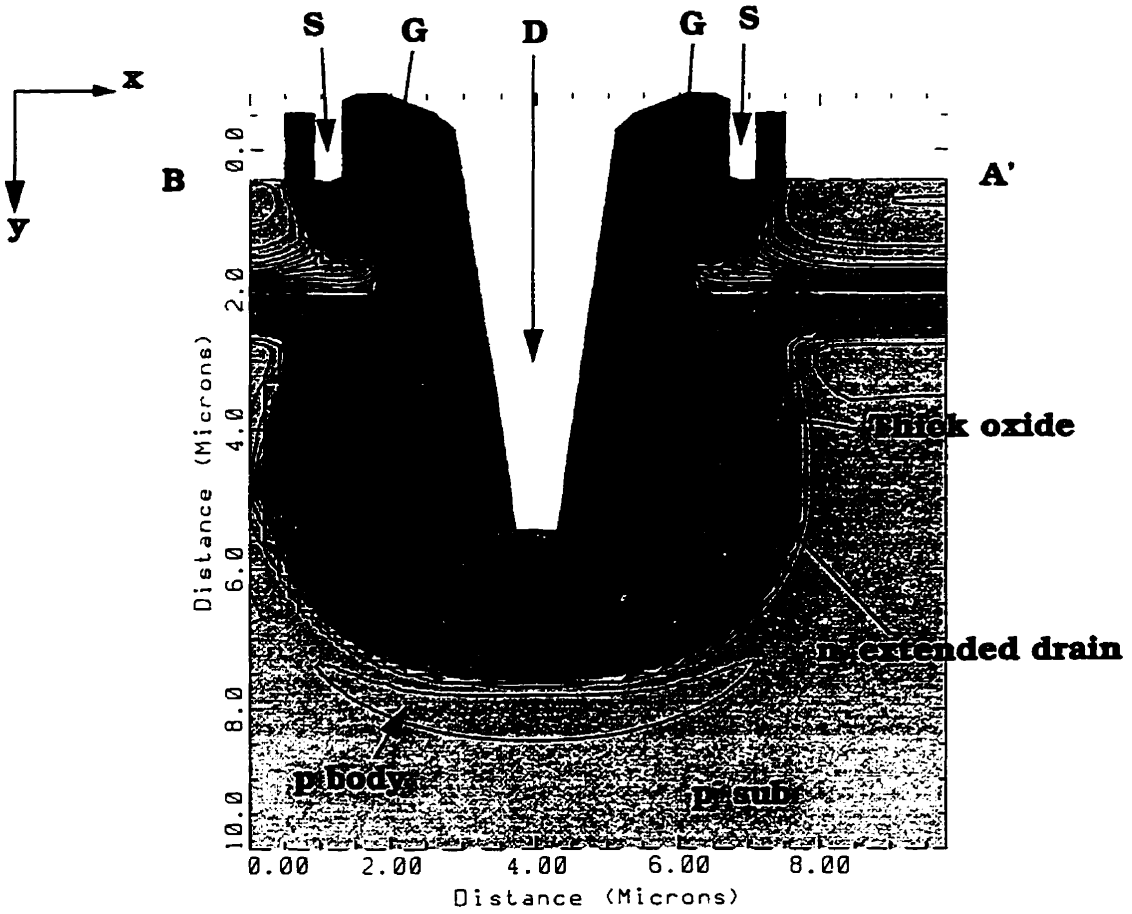


Figure 3.2 Result of process simulation for TLPM

sidewall and at the bottom of the trench. The n^- extended drain is implemented on the lower side of the sidewall and at the bottom of the trench. The polysilicon gate is formed along the sidewall.

The resultant doping profiles at different locations across the device are plotted in Figures 3.3 to 3.5. The net doping profile along the sidewall is shown in Figure 3.3. The n^+ source, p base, n^- extended drain, and p^- substrate extend from the surface to the bulk. The n^+ source has a surface concentration of 5×10^{19} cm^{-3} to create a good ohmic contact with the metal [2]. The junction depth is 0.7 μm which is deep enough to prevent penetration of any aluminum spike toward the p base [3]. The p base has the peak concentration

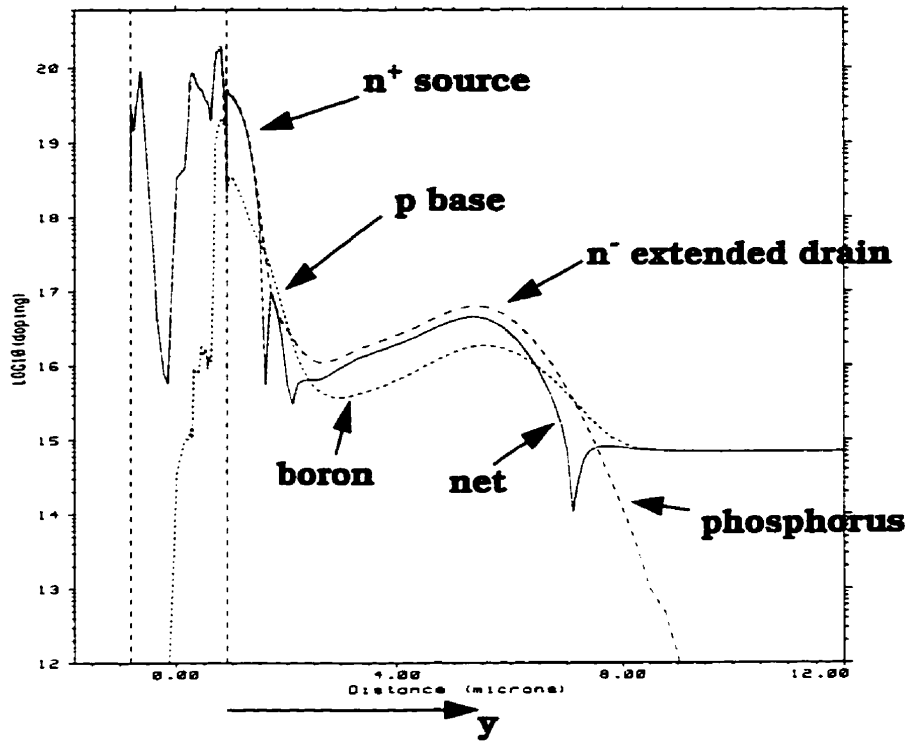


Figure 3.3 Doping profile along the sidewall (x = 1.6 μm)

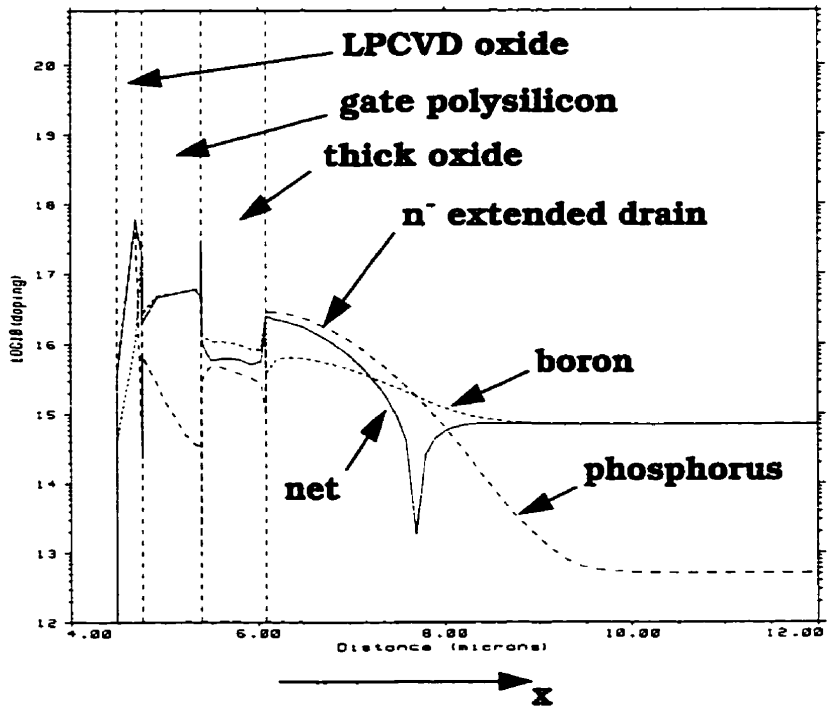


Figure 3.4 Doping profile at the n^- extended drain (y = 4 μm)

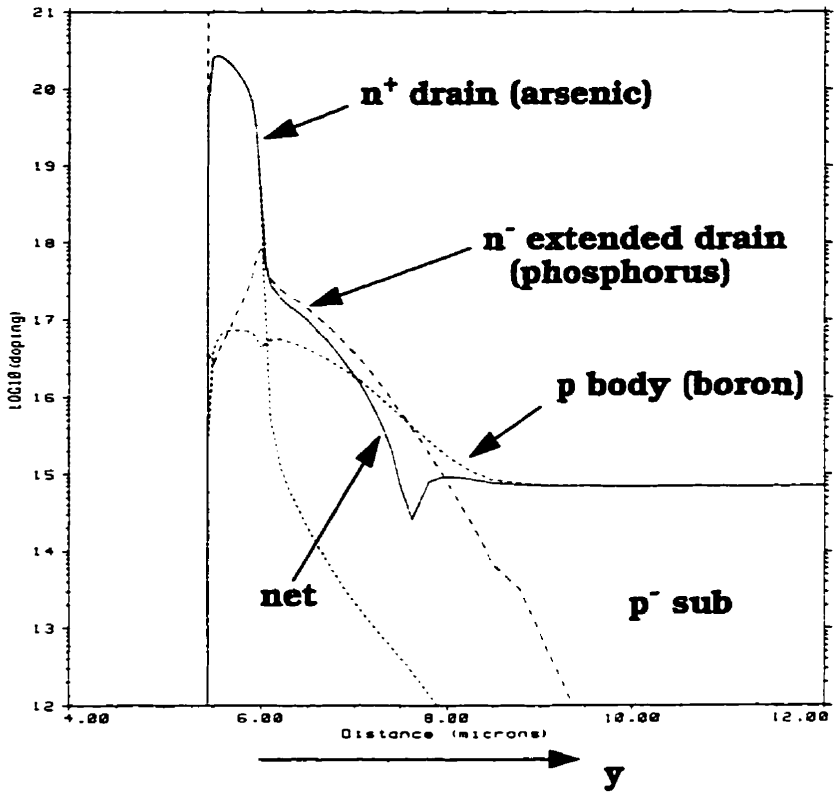


Figure 3.5 Doping profile at the n^+ drain (x = 4 μm)

of 1×10^{17} cm^{-3} and the base width is 0.7 μm. The p base concentration at the vicinity of the sidewall is 5×10^{16} cm^{-3}. The impurity concentration at this point and the thickness of the gate oxide are two of the major parameters which determine the threshold voltage of the device. The length of the n^- extended drain is approximately 4 μm to realize a breakdown voltage exceeding 80 V.

The horizontal net doping profile at the n^- extended drain is illustrated in Figure 3.4. Boron ions are added, compensating the phosphorous ions to optimize the breakdown voltage. The surface concentration and junction depth of the n^- extended drain are approximately 5×10^{16} cm^{-3} and 1.5 μm, respectively. The balanced charge between the n^-

extended drain and the sum of the p body and the p^- substrate expands the depletion region uniformly in the n^- extended drain and reduces the electric field in the region [4].

The vertical net doping profile at the bottom of the trench is shown in Figure 3.5. Arsenic is used instead of phosphorous at the bottom of the trench in order to provide a good contact between the silicon and the polysilicon by increasing the surface concentration on the silicon surface.

3.3 Device Simulation

3.3.1 Operation of the TLPM

A 2-D device simulator MEDICI [5] was used in the following device simulations with the doping profiles and the geometrical information from TSUPREM4 as input. The calculation was carried out on half of the structure because of the symmetrical nature of the device.

An on-state simulation was carried out and the result is illustrated in Fig.3.6 at operation conditions of V_{GS}=20 V and V_{DS}=1 V, I_{DS} flows from the source to the drain as is indicated by the current flow lines. Most of the current flows in the vicinity of the surface in the channel region, however, the current flows in the bulk silicon in the n^- extended drain.

I_D-V_{DS} drain characteristics are illustrated in Figure 3.7. When the gate voltage is smaller than 5 V, the channel resistance is predominant among the total on-resistance. Since most depletion region expands into the n^- extended drain because of the lower impu-

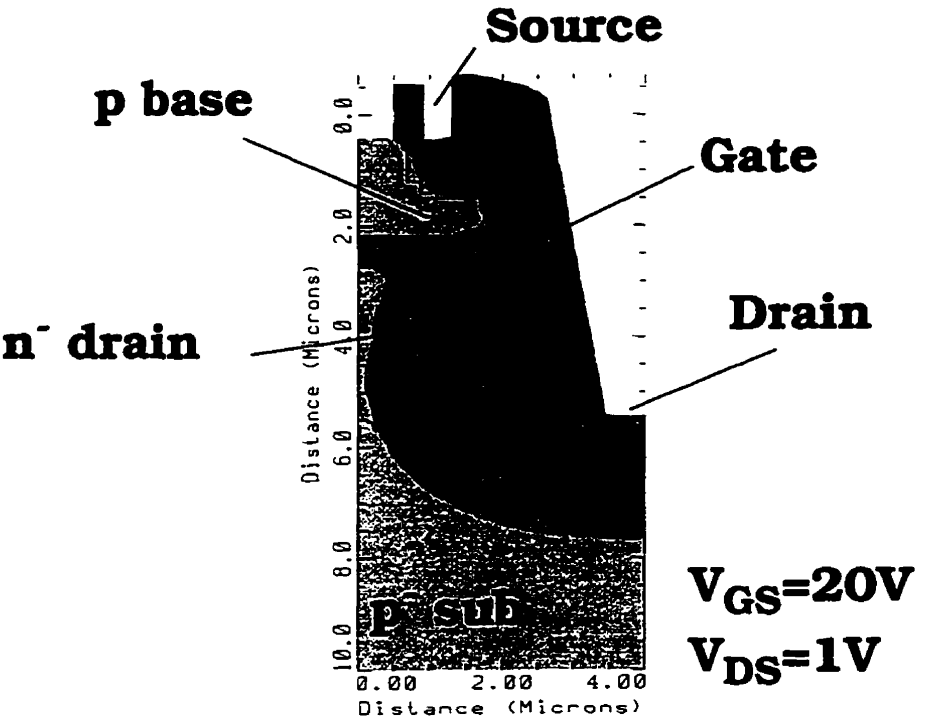


Figure 3.6 On-state simulation for TLPM

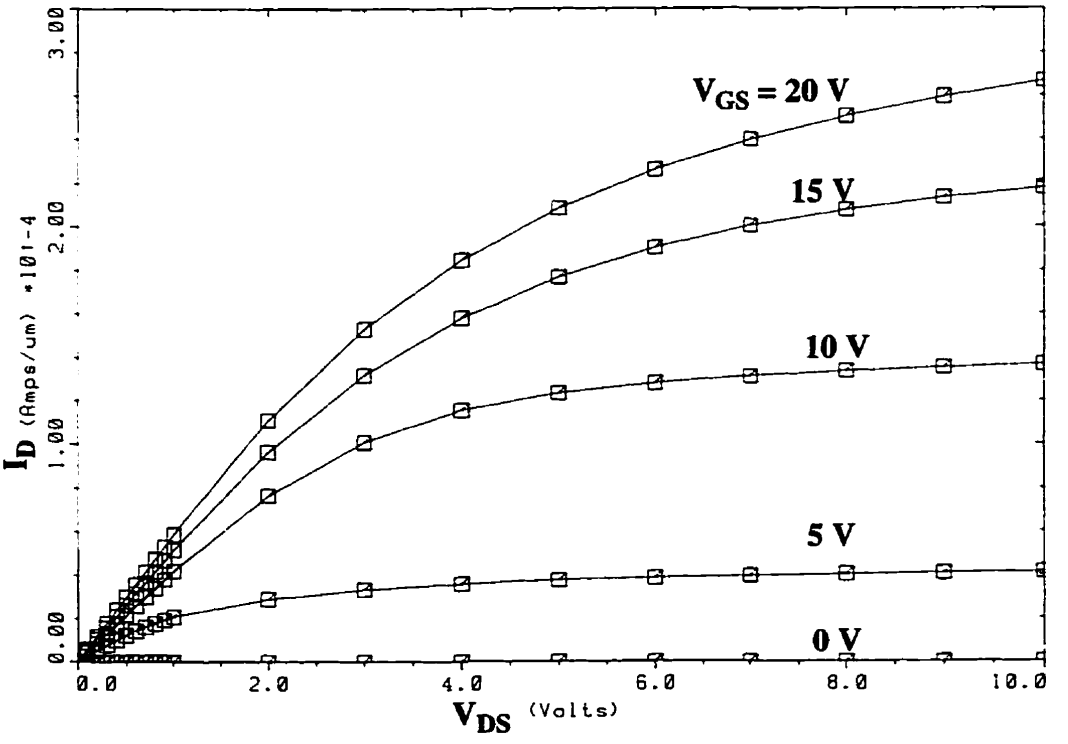


Figure 3.7 I_D-V_{DS} drain characteristics for TLPM

rity concentration in the region compared to that in the p base. As a result, although the TLPM has a short channel of 0.7 μm, constant drain current is observed in the saturation region. On the other hand, when the gate voltage is greater than 10 V, the channel resistance is not a major factor and now the resistance in the n^- extended drain become a predominant component of the total on-resistance of the TLPM, the increasing drain current in the saturation region due to the JFET type resistance in the n^- extended drain.

I_D-V_{GS} drain characteristics are illustrated in Figure 3.8. The threshold voltage is approximately 2 V and the drain current I_D is saturated for larger gate voltages because of a limited current in the n^- extended drain.

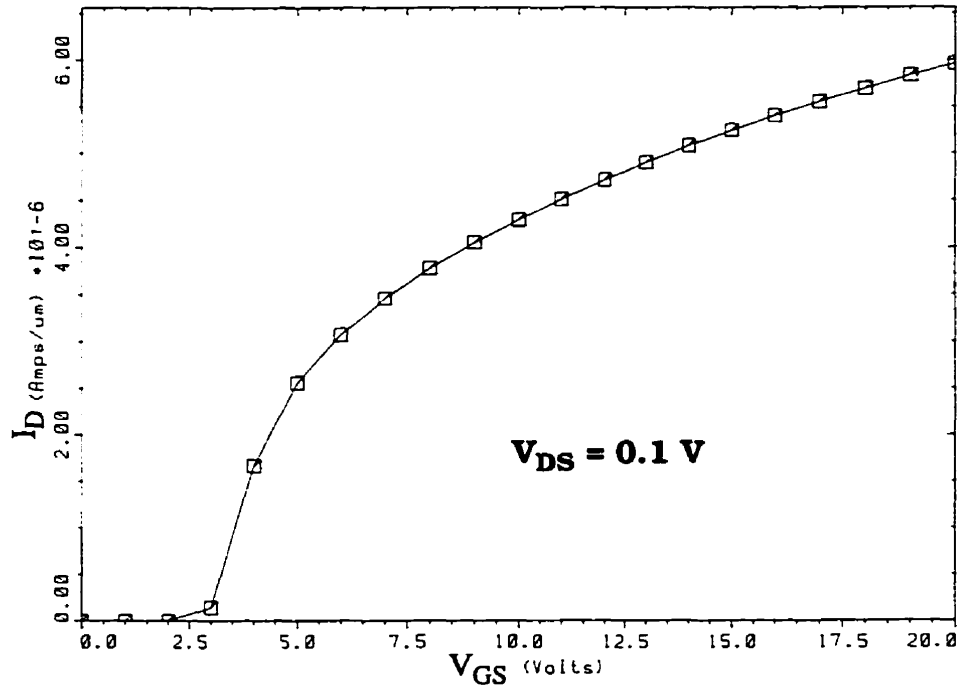


Figure 3.8 I_D-V_{GS} drain characteristics for TLPM

An off-state simulation is shown in Figure 3.9. At V_{GS}=0 V and V_{DS}=80 V, the electric field is uniformly distributed in the n^- extended drain as a result of balanced

charges in the n^- extended drain and the p-type substrate, showing a blocking capability exceeding 80 V. The breakdown occurs near the drain contact in the n^- extended drain.

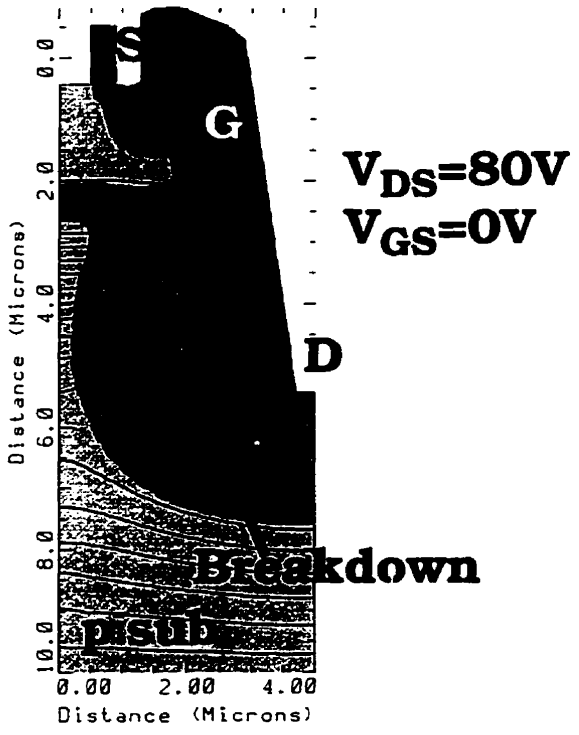


Figure 3.9 Off-state simulation for TLPM (each n^- drain dose is 1.8×10^{13} cm^{-2})

3.3.2 Off-state simulation at the device edge

Junction termination technology is important to obtain full breakdown capability. Off-state simulation at the device edge was carried out for the right half of the cross section in Figure 3.10. At V_{GS}=0 V and V_{DS}=80 V, the electric field is uniformly distributed in the n^- extended drain, showing a blocking capability of approximately 80 V. The breakdown occurs near the drain contact in the n^- extended drain.

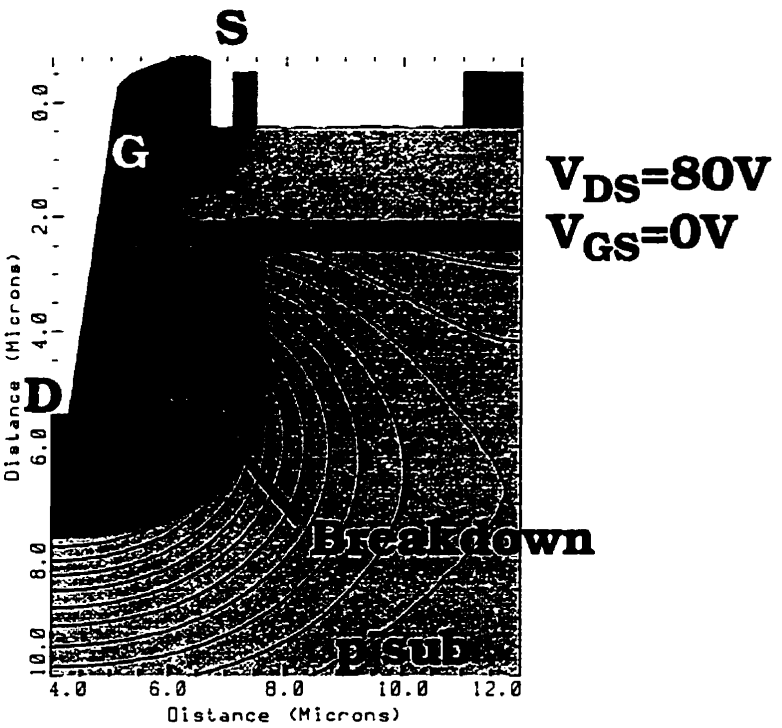


Figure 3.10 Off-state simulation on the device edge

3.3.3 Performance as a function of dose of the n^- extended drain

Dose of the n^- extended drain is one of the important parameters for the trade-off between the breakdown voltage and on-resistance. The optimum implantation dose of phosphorus was chosen to be 1.8×10^{13} cm^{-2}. In order to investigate the performance of the TLPM, process and device simulations were carried out for the different dose of the n^- extended drain. Figure 3.11 shows a simulation result for the off-state when the dose is 2.5×10^{13} cm^{-2}. Expansion of the depletion region is restricted in the n^- extended drain because of the larger amount of donor ions in the n^- extended drain associated with the higher dose in the n^- extended drain. As a result, breakdown occurs near the p base in the n^- extended drain at an operating voltage of V_{DS}=70 V (V_{GS}=0 V).

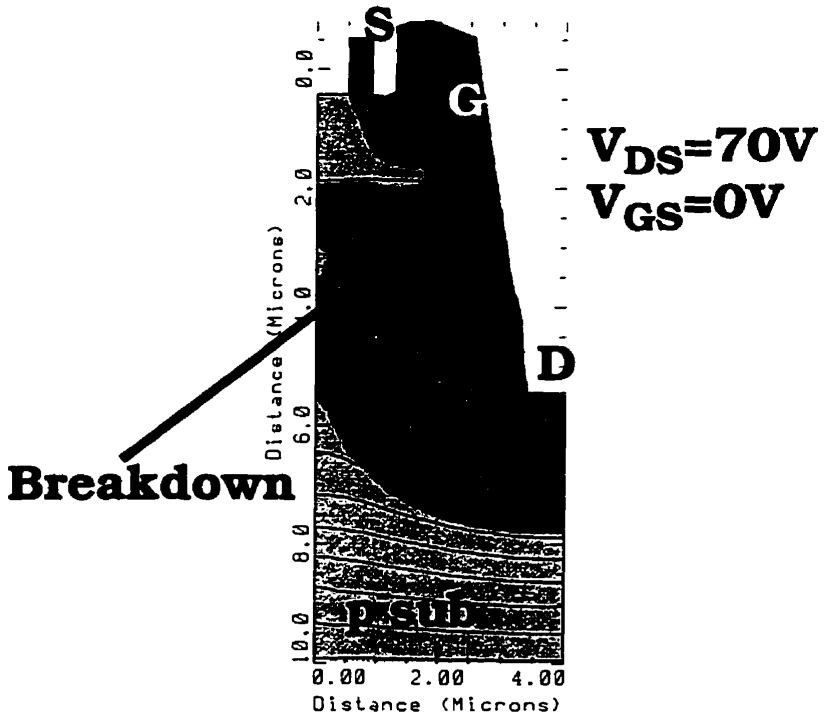


Figure 3.11 Off-state simulation for TLPM (each n^- drain dose is 2.5×10^{13} cm^{-2})

Figure 3.12 shows a simulation result for the off-state for a lower dose in the n^- extended drain, 0.5×10^{13} cm^{-2}. Breakdown occurs at the edge of the n^+ drain at an operating voltage of V_{DS}=45 V (V_{GS}=0 V). Since the donor ions in the n^- extended drain are much fewer than the acceptors in the p-type substrate, the n^- extended drain is fully depleted at a low drain voltage and the expansion of the depletion region into the p^- substrate is restricted. This increases the electric field at the edge of the n^+ drain due to a small effective radius of curvature of the n^+ drain diffusion, decided by the junction depth of the n^+ drain. As a result, breakdown occurs at a lower drain voltage.

Dependencies of breakdown voltage and specific on-resistance on the dose in the n^- extended drain are illustrated Figure 3.13. The breakdown voltage exhibits a maximum value, however, the on-resistance decreases as the dose increases.

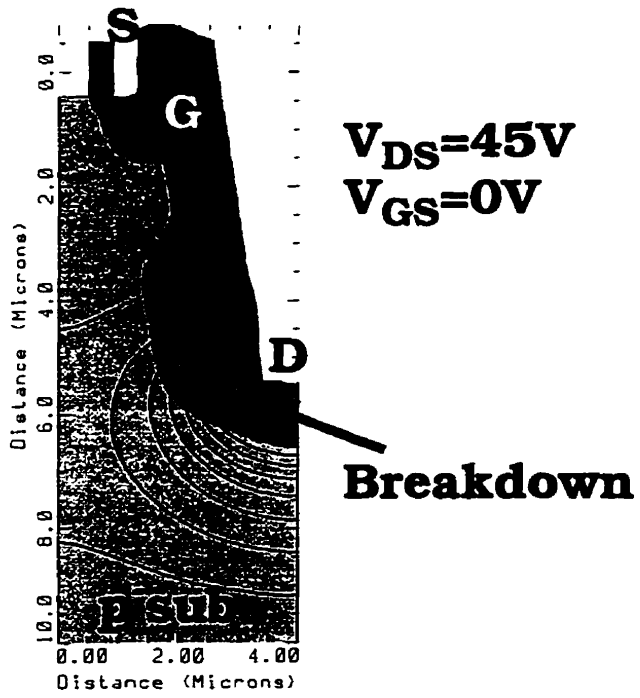


Figure 3.12 Off-state simulation for TLPM (each n^- drain dose is 0.5×10^{13} cm^{-2})

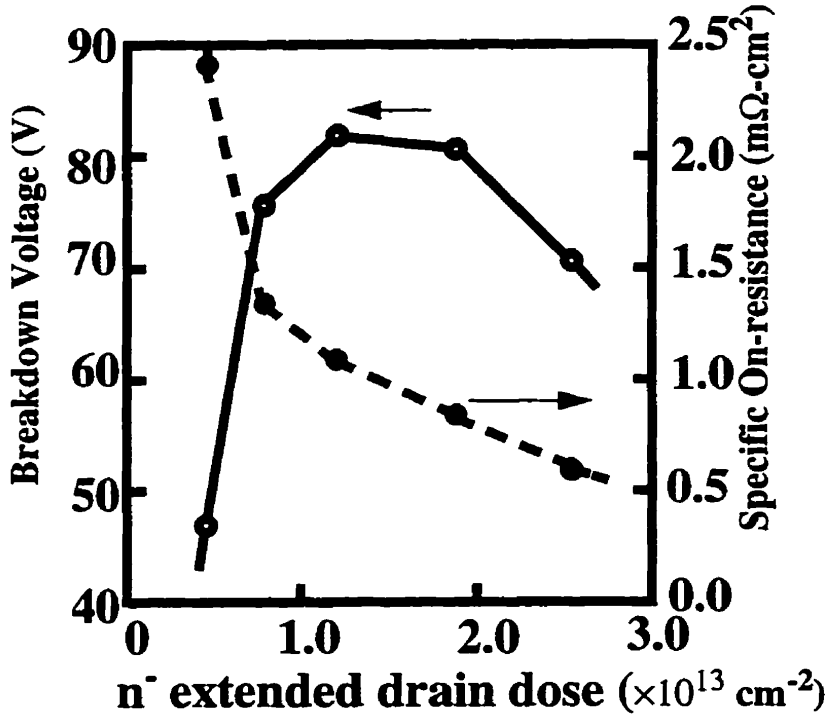


Figure 3.13 Dependence of the breakdown voltage and specific on-resistance on the dose in the n^- extended drain

3.3.4 Comparison of TLPM with a Conventional LPM (CLPM)

In order to compare TLPM with one of the typical Conventional Lateral Power MOSFETs (CLPMs), the structure shown in Figure 3.14 was simulated. The resistivity of the p^- substrate and the profile in the n^- extended drain were chosen to be similar in both devices.

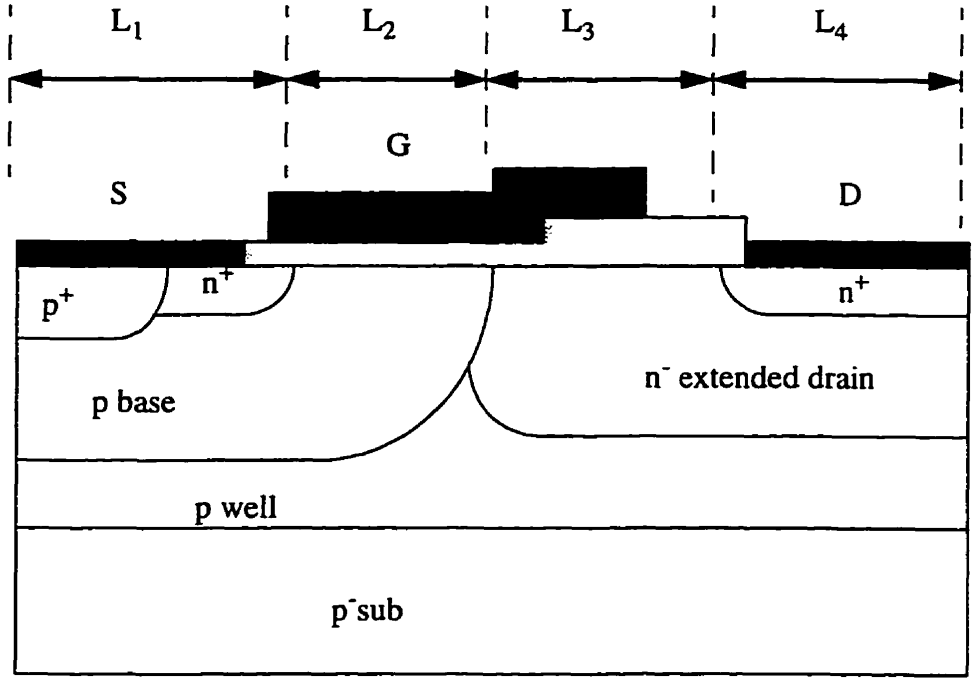
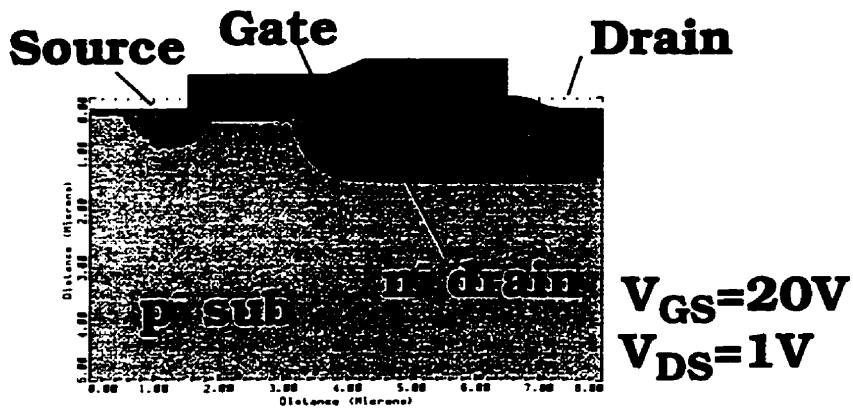
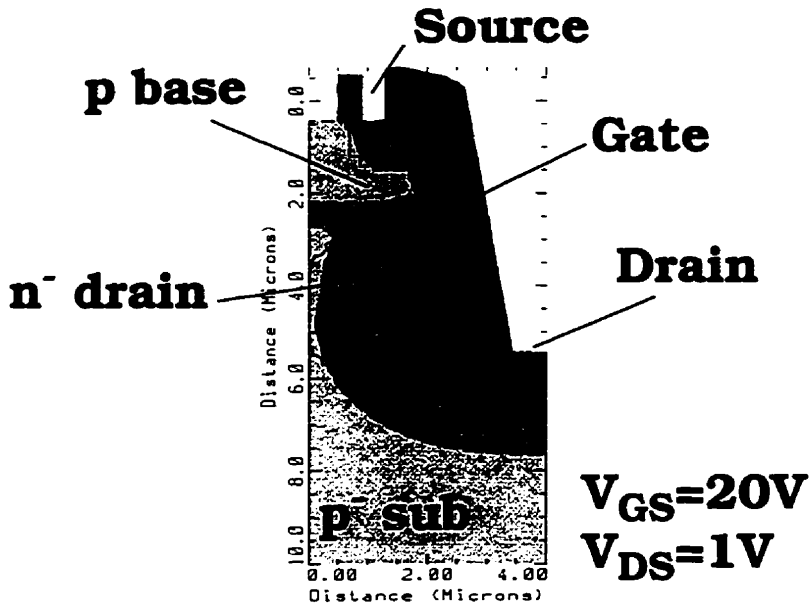


Figure 3.14 Simulated CLPM structure

An on-state calculations were carried out under the operating condition of V_{DS}=1 V and V_{GS}=20 V. The result for the CLPM is shown in Figure 3.15 (a). As indicated by the current flow lines, the electron current flows from the source to the drain through the surface of the p base and the n^- extended drain. The specific on-resistance of the CLPM is 1.6 $m\Omega\text{-}cm^2$ for a device with a breakdown voltage of 80 V.



(a) CLPM



(b) TLPM

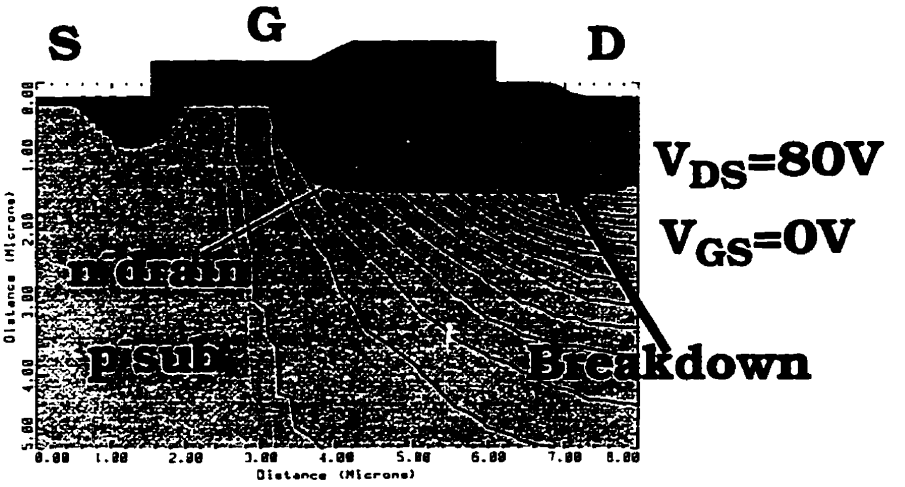
Figure 3.15 On-state simulation for the CLPM and the TLPM

On-state simulation was then carried out for TLPM as shown Figure 3.15 (b). The electron current flows from the source goes into the inversion channel, which is located in the vicinity of the sidewall, then travels across the n^- extended drain, reaching to the n^+ drain at the bottom of the trench.The operation condition is the same as the CLPM, V_{DS}=1 V and V_{GS}=20 V. In this simulation, the observed drain current is approximately the same

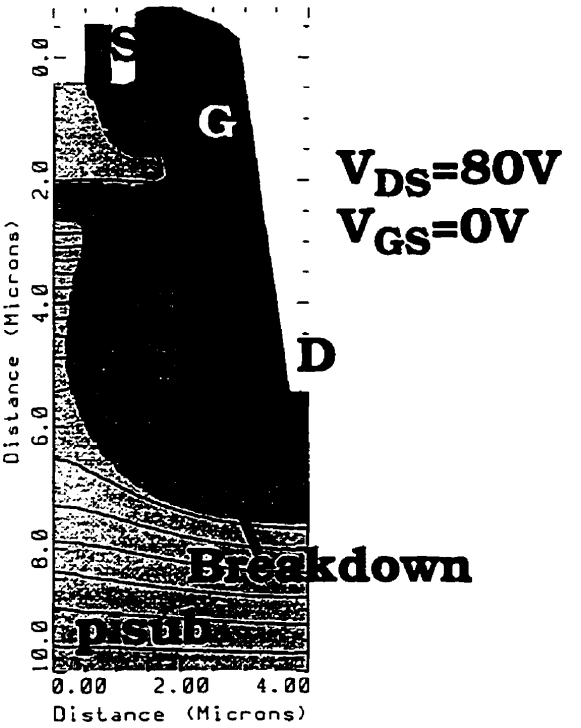
as that for the CLPM. Since the cell pitch for TLPM is 4 μm, which is half of the CLPM (8 μm), the specific on-resistance for TLPM is approximately half of the CLPM (0.8 mΩ-cm^2) for a device with a breakdown voltage of 80 V

Off-state simulations were also carried out to compare the CLPM and TLPM. Figure 3.16 (a) shows the blocking capability of the CLPM at $V_{GS} = 0$ V and $V_{DS} = 80$ V. The breakdown occurs near the drain contact in the n^- extended drain at a drain voltage of 80 V. The off-state simulation for the TLPM is shown in Figure 3.16 (b). The breakdown also takes place near the drain contact in the n^- extended drain at V_{DS}= 80 V, which is identical to the breakdown voltage of the CLPM.

The on-resistance of the TLPM and the CLPM were also compared by assuming that: (1) both LPMs with the same breakdown voltage have the same current handling capability, (2) a 1μm design rule was used, (3) the breakdown voltage is weakly dependent on the distance between the source and the drain and (4) the resistance in the plugged drain is small. Based on these assumptions, the relationship between the breakdown voltage and the ratio of the on-resistance of the TLPM and CLPM is shown in Figure 3.17. For instance, a ratio of approximately 0.5 is obtained for devices with a breakdown voltage of 80 V.



(a) CLPM



(b) TLPM

Figure 3.16 Off-state simulation for the CLPM and the TLPM

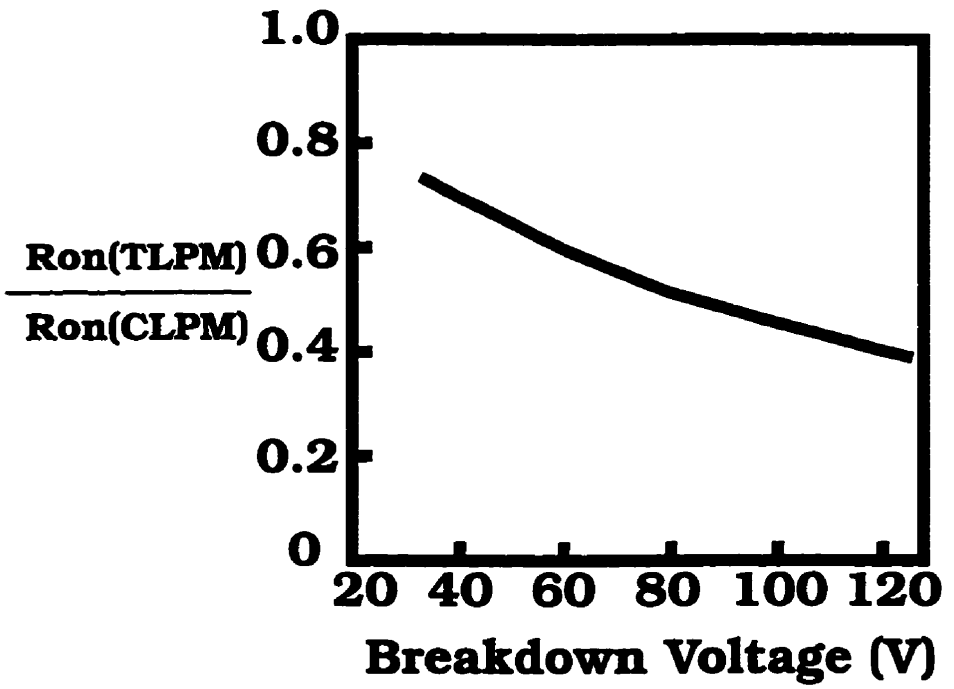


Figure 3.17 A relationship between breakdown and ratio of on-resistance between TLPM and CLPM

3.4 Experimental Results

3.4.1 Formation of Silicon Trench

The SEM micrograph after silicon trench etching is shown in Figure 3.18. After opening the oxide window, trench etching is performed by using RIE, using a gas combination of Cl_2 and BCl_3 [6]. A 17-minute silicon trench etching is performed continuously to achieve smooth sidewalls. As shown in Figure 3.18, a very smooth and sharp sidewall with an angle θ of 10 ° from the vertical is observed. This angle is small enough to keep deposited thin films on the sidewall after the subsequent RIE etching.

Figure 3.19 shows the SEM micrograph after the second silicon trench etching. Nitride film remains on the sidewall after the second silicon trench etching.

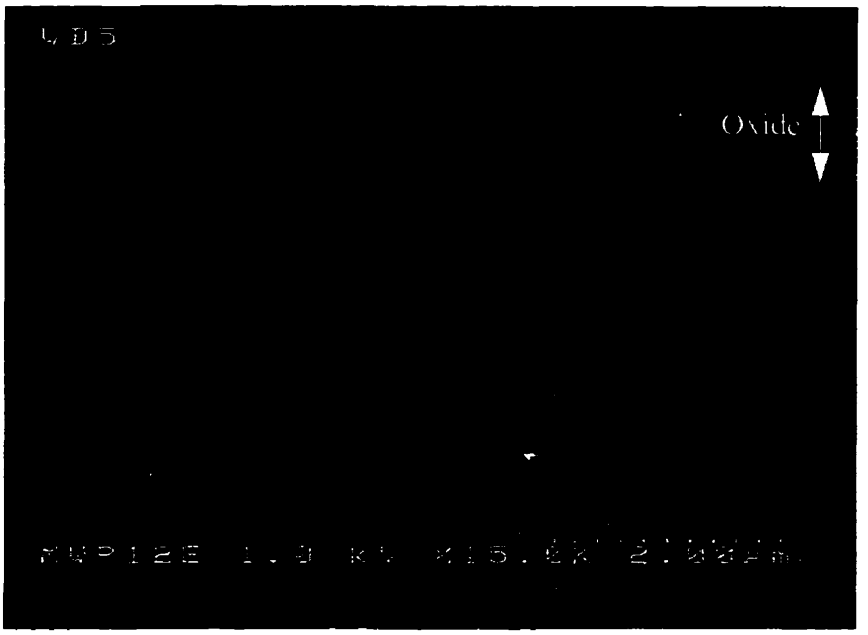


Figure 3.18 SEM micrograph after silicon trench etching

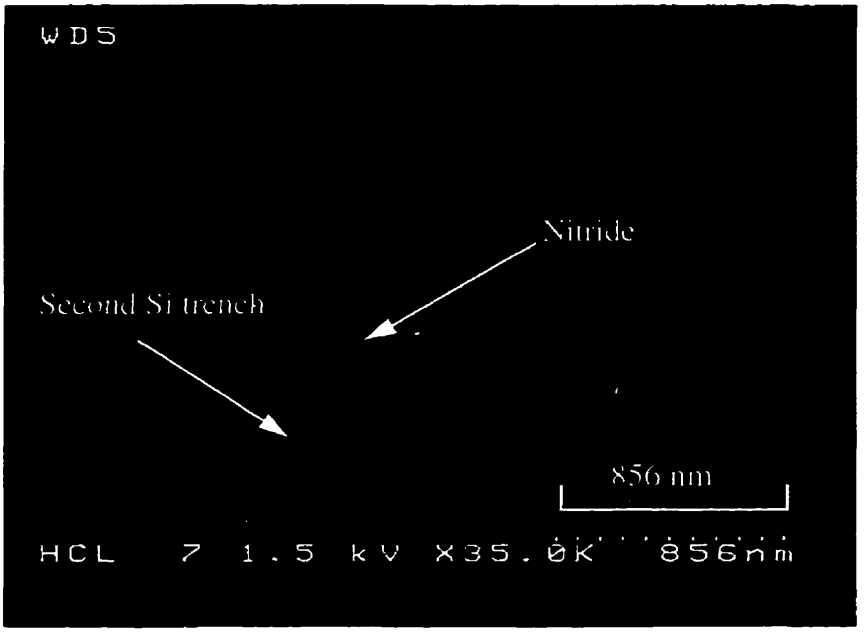


Figure 3.19 SEM micrograph after the second silicon trench etching

3.4.2 Gate Definition

Figure 3.20 shows micrograph of the top view of the TLPM after the gate definition, where the gate electrode is formed across the trenches. After the silicon trenches are formed, gate oxide is grown and thick oxide and polysilicon are deposited. Then photoresist is deposited and photolithography is carried out. Thereafter a combination of wet and dry etching is used to etch the oxide. Then polysilicon is etched by RIE.

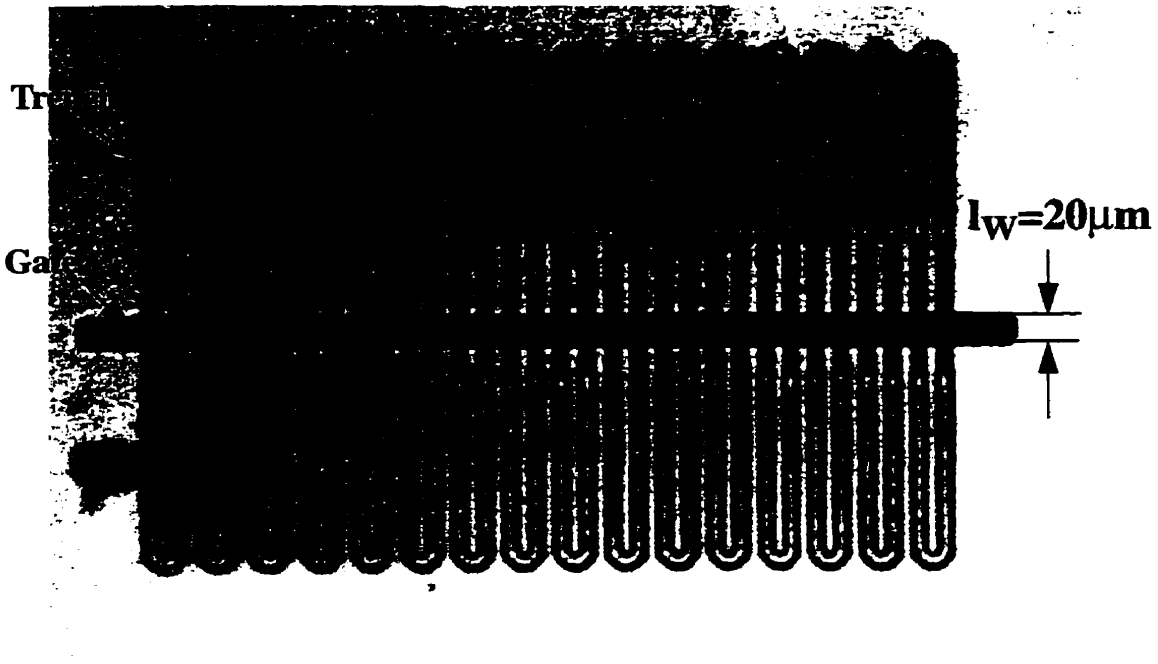


Figure 3.20 Micrograph of the top view of TLPM after the gate definition

3.4.3 Trench Bottom Contact Hole

An SEM micrograph after oxide deposition at the bottom and the top of the silicon trench is shown in Figure 3.21. The recessed thick oxide is observed at the bottom side of the sidewall and at the bottom of the trench. The gate electrode is observed on the sidewall of the trench. After the gate electrode is formed on the sidewall of the trench, 1.9 μm of

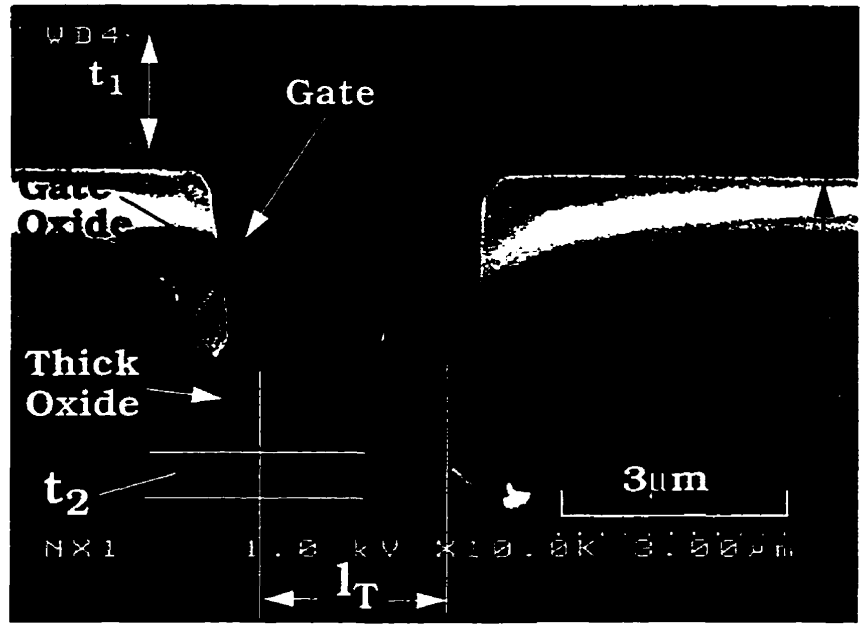


Figure 3.21 SEM micrograph after oxide deposition at the bottom and top of the trench

oxide t_1 is deposited by LPCVD, however, the deposited oxide inside the trench t_2 is thinner (0.8 μm) than that on the surface [6]. The ratio of oxide thickness t_2/t_1 as a function of bottom width in the trench l_T is illustrated in Figure 3.22 which indicates that as l_T gets smaller, the oxide inside the trench becomes thinner.

Figure 3.23 shows an SEM micrograph after RIE etching of the oxide to open the drain contact. It is observed that a contact hole with a width l_{BC} ($2l_6$) of 0.8 μm is completely opened and the silicon surface is bare at the bottom of the trench. However, the oxide on the surface and on the sidewall remains thick enough to keep good isolation between gate and the drain. The remaining oxide thickness on the surface (t_1-t_2) and the sidewall (t_{SW}) are 0.7 μm and 0.4 μm respectively. A gate region l_G of 0.7 μm is achieved, resulting in a distance between the source and the drain l_5 of 1.5 μm as compared to 5 μm ($l_2 + l_3$) for the CLPM. This results in a reduced pitch which is realized by the fact that the gate electrode and the drain contact holes are self-aligned to the trench.

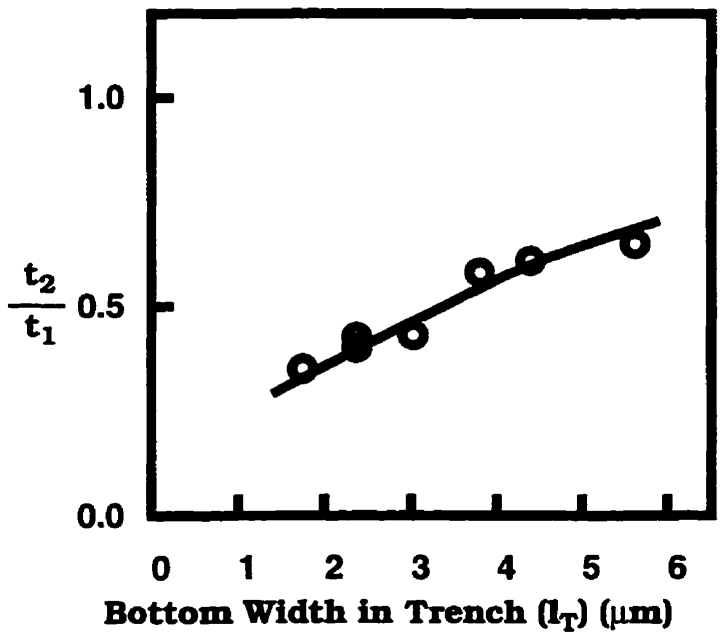


Figure 3.22 Ratio of oxide thickness versus l_T

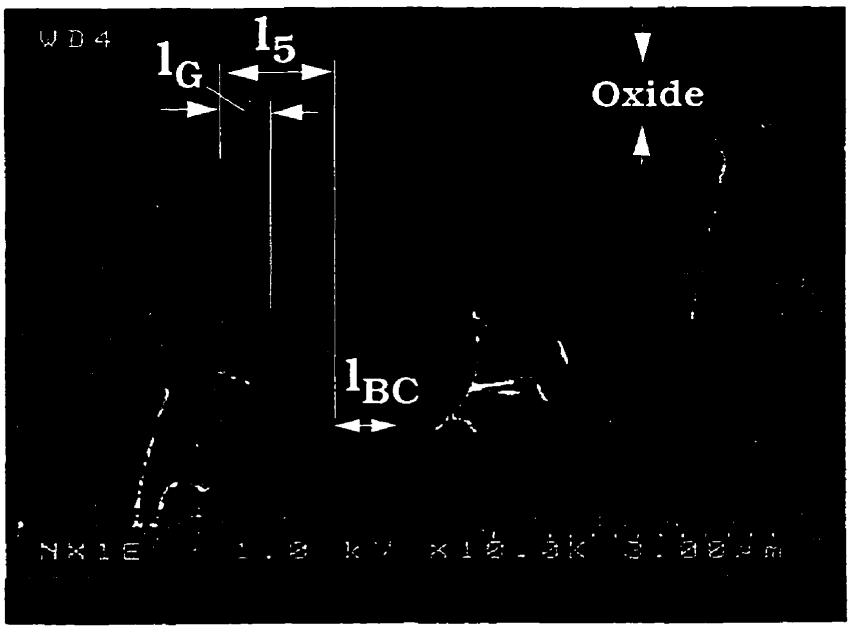


Figure 3.23 SEM micrograph after RIE etching of oxide to open the drain contact

Figure 3.24 shows the dependencies of contact hole width l_{BC} and oxide thickness on the sidewall t_{SW} as a function of bottom trench width l_T. Since t_{SW} is a weak function of l_T, the contact size gets larger as l_T increases.

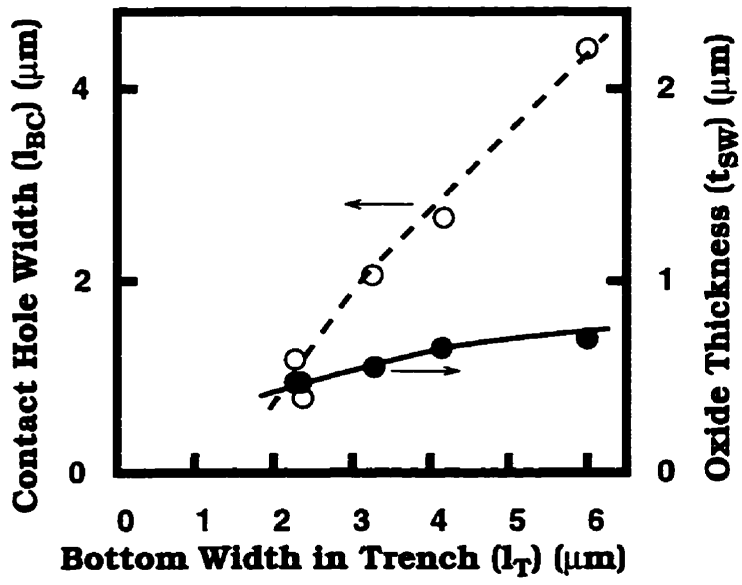


Figure 3.24 Contact hole width and oxide thickness on the sidewall versus l_T

3.4.4 Trade-off Between Specific On-resistance and Breakdown Voltage

The trade-off between specific on-resistance and breakdown voltage is shown in Figure 3.25. Previous work [7] together with the result for the CLPM investigated in this work are illustrated in this figure. The CLPM shows a specific on-resistance of 1.6 mΩ-cm^2 for a device with a breakdown voltage of 80 V. By comparison with the CLPM, the TLPM shows a 50% reduction in specific on-resistance 0.8 mΩ-cm^2, for a breakdown voltage of 80 V. This number is very close to the silicon limit [7].

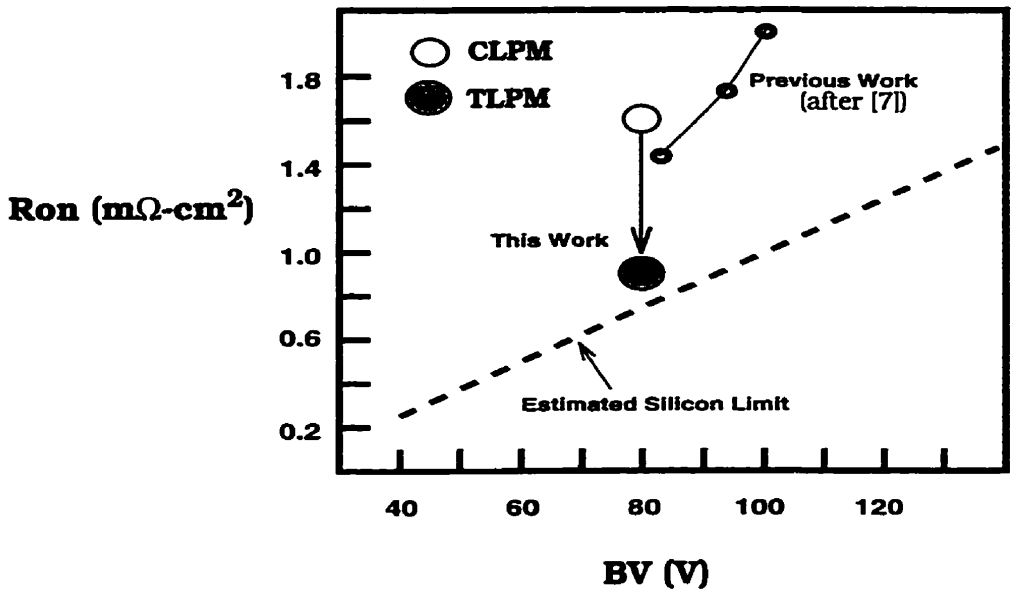


Figure 3.25 Trade-off between specific on-resistance and breakdown voltage

3.5 Summary

In this chapter, the proposed TLPM process presented in Chapter 2 was verified using a 2-D process and device simulators. Impurity profiles for the n^+ source, p base, n^- extended drain, and n^+ drain were also verified. In addition, the steps involved in the fabrication of the trench structure, such as formation of the gate electrode, growth of thick oxide on the sidewall and bottom of the trench were shown to be feasible. 2-D device simulations were carried out using the results of the process simulations. The structure of the proposed TLPM was compared to that of a CLPM. It was observed that the current handling capability of the TLPM (formed along the sidewall of the trench) is approximately identical with that of the CLPM (formed at the surface of the silicon substrate), while the device pitch for the TLPM (4 μm) was formed to be half of that of the CLPM (8 μm). In

addition, the predicted breakdown voltages for both (80 V) devices were found to be the same.

Experimental verification for the implementation of TLPM was presented. It was demonstrated that the thick oxide is formed on the lower side of the trench to increase breakdown voltage. It was also shown that the gate electrodes and the bottom drain contact holes are formed by using a self-aligned method, realizing a lateral distance l_5 between the source and the drain to be 1.5 μm as compared to 5 μm ($l_2 + l_3$) for CLPM thus resulting in a reduced specific on-resistance. The results showed that the specific on-resistance of TLPM is 0.8 mΩ-cm^2, approximately half that of a CLPM for a breakdown voltage of 80 V.

References

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CHAPTER 4

Conclusions

Motivated by limitations in the conventional design of lateral power MOSFETs in terms of trade-offs between specific on-resistance and breakdown voltage, a novel MOSFET with a trench structure was proposed in this thesis.

In Chapter 2, the novel Trench Lateral Power MOSFET (TLPM) and its fabrication process were presented. The gate, channel and n^- extended drain of the proposed TLPM were formed along the sidewall of the trench in order to increase the packing density of the device. The eight mask TLPM process uses self-aligned methods to form the gate electrode and trench bottom contact holes to the drain to achieve minimum pitch and very low on-resistance.

In Chapter 3, process and device simulations were carried out to verify the process and to investigate the performance of the proposed TLPM. TLPM was compared to a Conventional LPM (CLPM). The results showed that the current handling capabilities were approximately identical for both devices with a breakdown voltage of 80 V. The device pitch of the TLPM (4 μm) was half of that of the CLPM (8 μm), indicating that the specific on-resistance of TLPM was about half of CLPM.

Experimental verifications of the TLPM process were presented. It was observed that bottom trench contact holes were opened in a self-aligned method by combining RIE with LPCVD. The SEM micrograph demonstrated that the lateral distance between the source and the drain of TLPM was 1.5 μm as compared to 5 μm for the CLPM, hence reducing device pitch remarkably. The results showed that the specific on-resistance of the

TLPM is 0.8 $m\Omega$-cm^2, approximately half that of similar CLPM devices with a breakdown voltage of 80 V.

Future work may consist of modifying the existing design to achieve the lowest on-resistance for devices with different breakdown voltages, such as 30 V and 120 V which have applications in a variety of areas. Another objective may be the integration of the TLPM into a standard BiCMOS process to realize power ICs with high performance.

APPENDIX A

Test Chip Implementation

A.1 Test Chip Description

A plot of the test chip layout is shown in Figure A.1. The test chip includes nine test element groups (A-J) such as Trench Lateral Power MOSFETs (TLPMs), test structures for sheet and contact resistance, test structures for SEM inspection, and alignment marks. The designed TLPMs are classified into three groups in terms of the trench shapes, as shown in Figure A.2: (a) stripe trenches with 90 ° corners, (b) stripe trenches with rounded corners, (c) circled trenches. The main purpose of the design is to investigate the dependencies of breakdown voltages on the shape of the trench corners. The description of

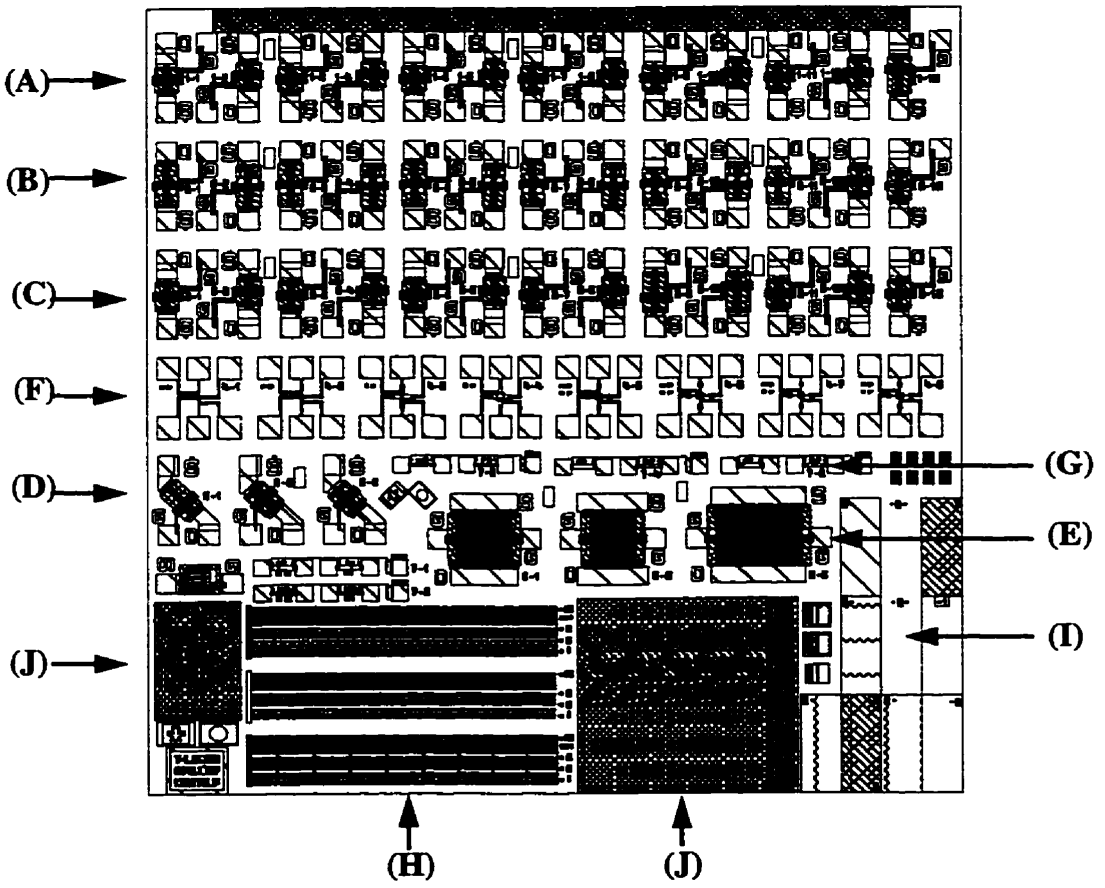
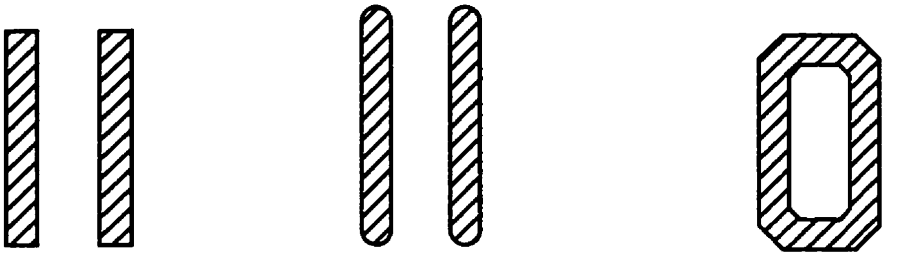


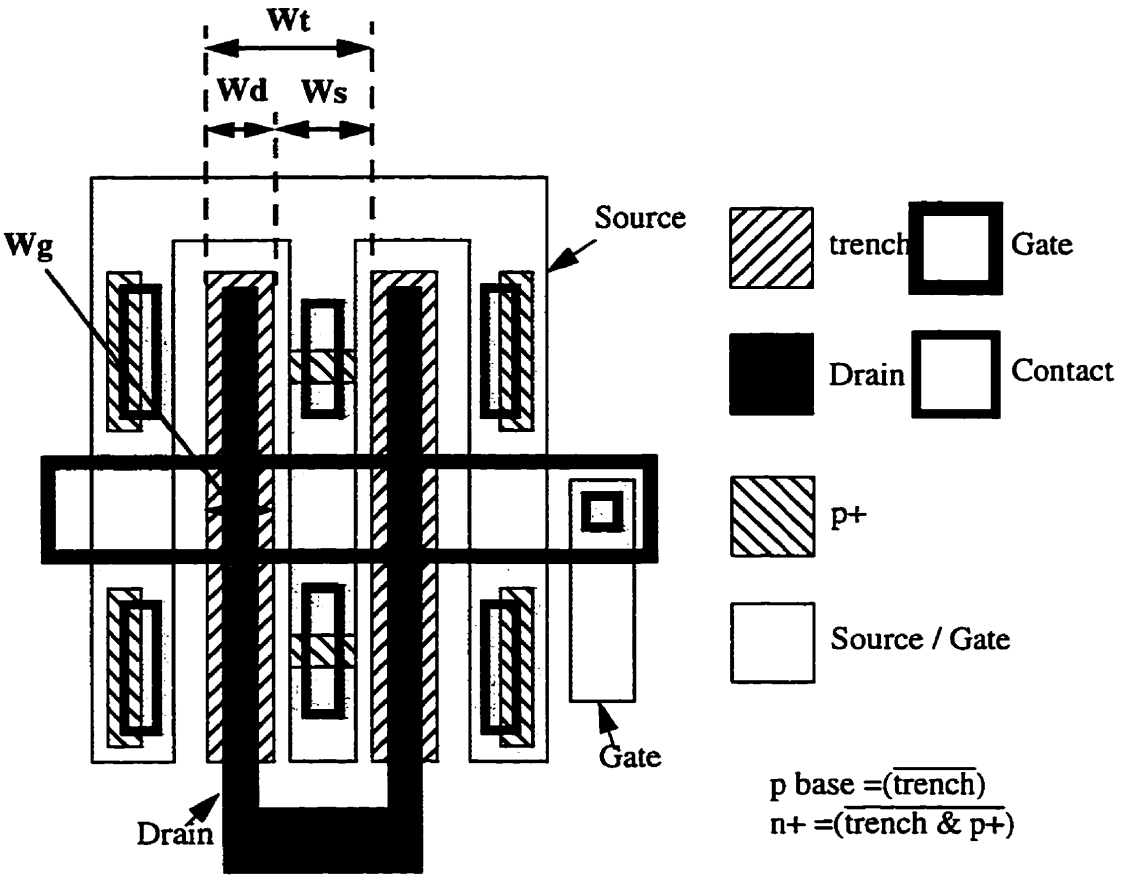
Figure A.1 Test chip layout which consists of ten test element groups A-J

each device is given in Table A.1-A.9, where W_{eff} represents the effective channel width of TLPMs and the definitions of other design parameters for TLPMs are illustrated in Figure A.3.



(a) 90 ° corners (b) Rounded corners (c) Circled trench

Figure A.2 Layout patterns of trenches



Wd: Trench width in the active area

Ws: Space between the two trenches in the active area

Wt: Sum of Wd and Ws

Wg: Trench width in the gate area

Figure A.3 Design parameters for TLPM

Table A.1 List of test element group (A): TLPMs (Stripe trenches with 90 ° corners)

File name	Wg (μm)	Wd (μm)	Ws (μm)	Wt (μm)	Weff (μm)	Location
str_g1t3s10u1	1	3	10	13	116	1-1
str_g2t4s9u1	2	4	9	13	116	1-2
str_g3t5s8u1	3	5	8	13	116	1-3
str_g2t4s6u1	2	4	6	10	116	1-4
str_g3t5s6u1	3	5	6	11	116	1-5
str_g2t3s5u1	2	3	5	8	116	1-6
str_g3t4s6u1	3	4	6	10	116	1-7
str_g5t5s8u1	5	5	8	13	116	1-8
str_g1t2s6u1	1	2	6	8	116	1-9
str_g1t7s10u1	1	7	10	17	116	1-10
dgs_typ12_SA1_3uni	1	2	10	12	232	1-13

Table A.2 List of test element group (B): TLPMs (Stripe trenches with rounded corners)

File name	Wg (μm)	Wd (μm)	Ws (μm)	Wt (μm)	Weff (μm)	Location
cir_g1t3s10u2	1	3	10	13	174	2-1
cir_g2t4s9u2	2	4	9	13	174	2-2
cir_g3t5s8u2	3	5	8	13	174	2-3
cir_g2t4s6u2	2	4	6	10	174	2-4
cir_g3t5s6u2	3	5	6	11	174	2-5
cir_g2t3s5u2	2	3	5	8	174	2-6
cir_g3t4s6u2	3	4	6	10	174	2-7
cir_g3t3s5u2	3	3	5	8	174	2-8
cir_g2t4s9u1	2	4	9	13	116	2-9
cir_g2t3s5u1	2	3	5	8	116	2-10

Table A.3 List of test element group (C): TLPMs (Circled trench)

File name	Wg (μm)	Wd (μm)	Ws (μm)	Wt (μm)	Weff (μm)	Location
strc_g1t3s10u1	1	3	10	13	116	3-1
strc_g2t4s9u1	2	4	9	13	116	3-2
strc_g3t5s8u1	3	5	8	13	116	3-3
strc_g2t4s6u1	2	4	6	10	116	3-4
strc_g3t5s6u1	3	5	6	11	116	3-5
strc_g2t3s5u1	2	3	5	8	116	3-6
strc_g3t4s6u1	3	4	6	10	116	3-7
strc_g5t5s8u1	5	5	8	13	116	3-8
strc_g2t4s9u3	2	4	9	13	232	3-9
strc_g2t3s5u3	2	3	5	8	232	3-10
strc_g7t7s10u1	7	7	10	17	116	3-11
strc_g3t3s5u1	3	3	5	8	116	3-12
strc_g2t2s4u1	2	2	4	6	116	3-13
strc_g2t3s5u1_allPB_ND	2	3	5	8	116	2-12
strc_g3t5s8u1_allPB_ND	3	5	8	13	116	1-12

Table A.4 List of test element group (D): TLPMs (45 ° rotated)

File name	Wg (μm)	Wd (μm)	Ws (μm)	Wt (μm)	Weff (μm)	Location
dgs_typ12_SA1_3uni_45	1	2	10	12	232	5-1
strc_g2t4s9u1_45	2	4	9	13	116	5-2
strc_g2t3s5u1_45	2	3	5	8	116	5-3

Table A.5 List of test element group (E): TLPMs (Large channel width)

File name	Wg (μm)	Wd (μm)	Ws (μm)	Wt (μm)	Weff (μm)	Location
typ8c_M_g2t3s5	2	3	5	8	11832	6-1
typ6c_M_g2t2s4	2	2	4	6	11832	6-2
typ13cir_M_g3t5s8	3	5	8	13	11136	6-3

Table A.6 List of test element group (F):

Kelvin structures for contact resistance measurement

File name	Description	Location
contact_ndev_con	contact size = 3 μm by 3 μm	4-1
contact_pdev_con	contact size = 3 μm by 3 μm	4-2
contact_gate_con	contact size = 3 μm by 3 μm	4-3
contact_epoly_con	contact size = 3 μm by 3 μm	4-4
contact_ndrain_epoly10	trench width= 10 μm	4-5
contact_ndrain_epoly5	trench width= 5 μm	4-6
contact_ndrain_epoly3	trench width= 3 μm	4-7
contact_ndrain_epoly2	trench width= 2 μm	4-8

Table A.7 List of test element group (G): Structures for sheet resistance measurement

File name	Description	Location
pad_res_gate_con1_2	gate (contact: 1 X 4 μm & 2 X 4 μm)	7-1
pad_res_ndev_con1_2	ndev (contact: 1 X 4 μm & 2 X 4 μm)	7-2
pad_res_ndev_pdev	ndev and pdev	7-3
pad_res_gate_epoly	gate and epoly	7-4
pad_res_gate_epoly	gate and epoly	7-5

Table A.8 List of test element group (H): Structures for SEM inspection

File name	Description
sem	cross section for the active area
sem_gate	cross section for the gate area
sem_epoly	cross section for the active area with drain poly-Si

Table A.9 List of test element group (I): Structures for step height measurement

File name	Description
alpha_con	substrate-contact
alpha_con_gate	gate polysilicon-contact
alpha_epoly	drain polysilicon-substrate
alpha_gate	gate polysilicon-substrate
alpha_met	metal-substrate
alpha_trench	substrate-trench

Table A.10 List of test element group (J): Alignment marks

File name	Description
alm_main	Main alignment marks
alm_sub	Sub alignment marks

A.2 Fabricated Test Chip

The Trench Lateral Power MOSFETs (TLPMs) were fabricated and a micrograph of a typical device along with the corresponding device layout are shown in Figure A.4. The device has an interdigitated surface geometry which consists of two silicon trenches with a width of 3 μm. The gate is located across the trenches. The channel width is 116 μm. The active area is 1856 μm^2. The device is presently being fully characterized.

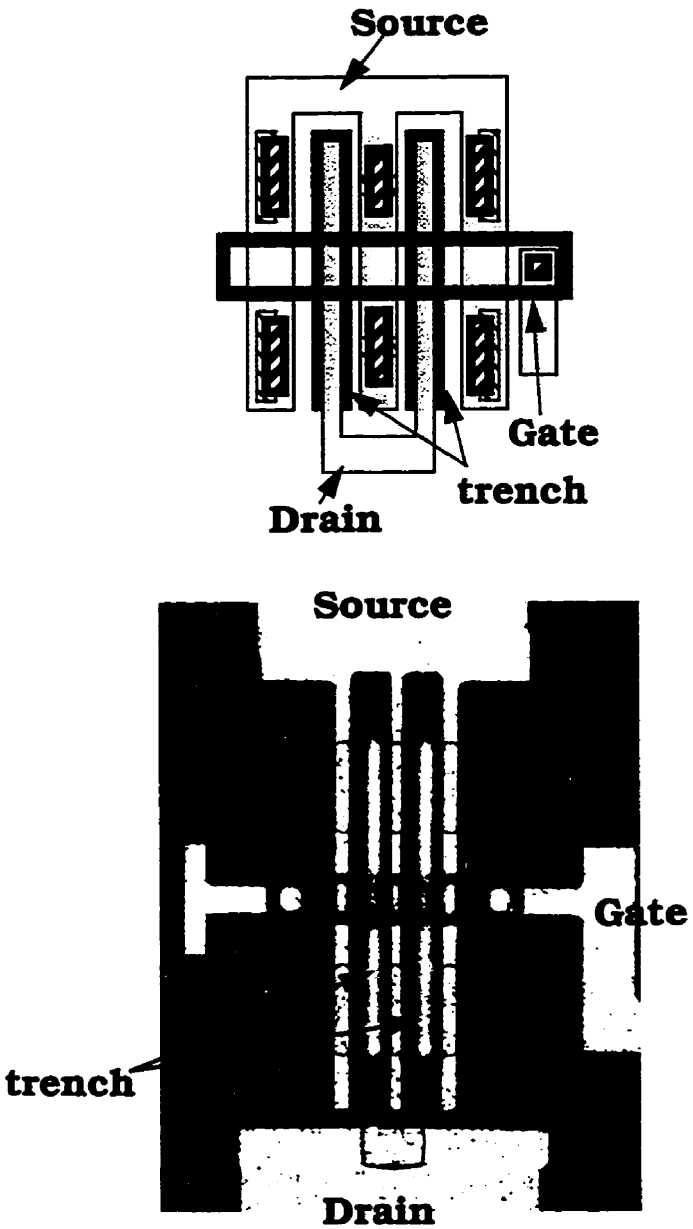
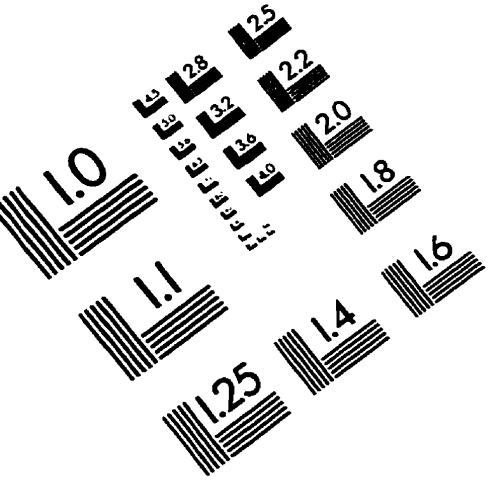
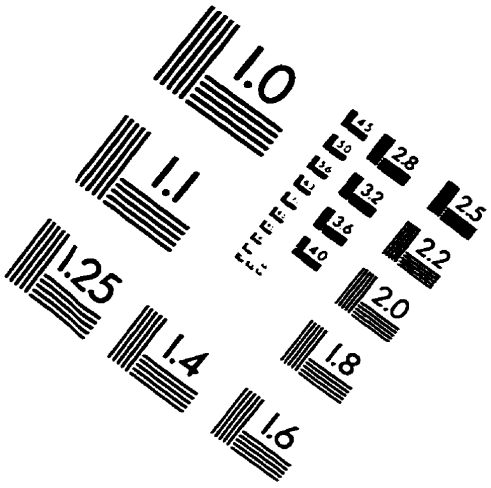
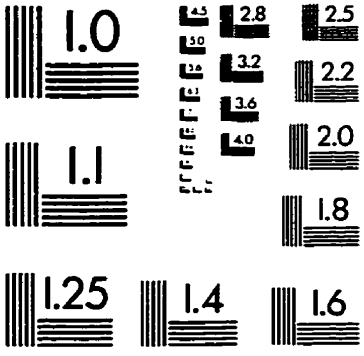


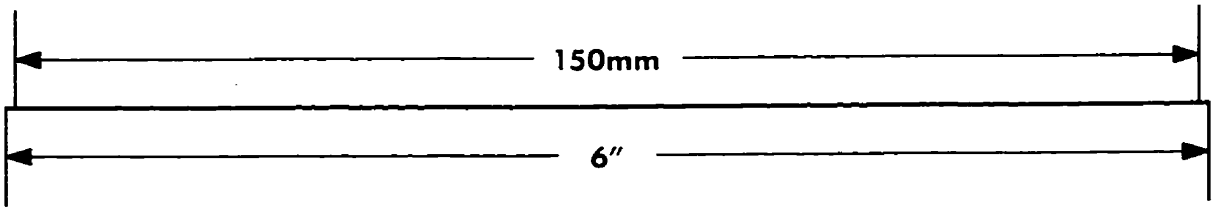
Figure A.4 Micrograph of TLPM along with the corresponding device layout

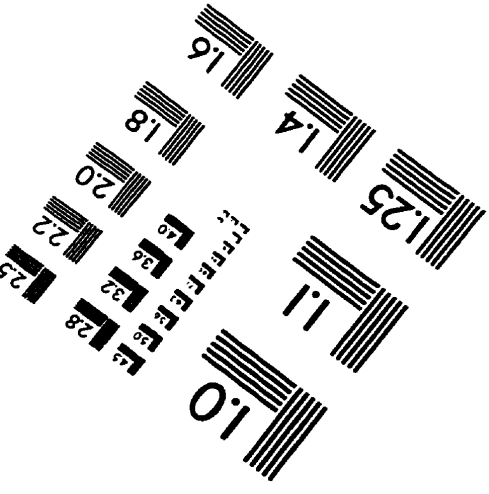
IMAGE EVALUATION
TEST TARGET (QA-3)

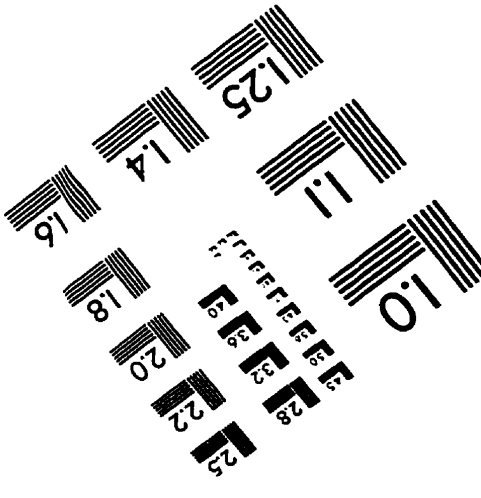












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