ANALOG AND MIXED-SIGNAL DFT USING WIDEBAND UNDERSAMPLING

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ABSTRACT

Integrated Circuit (IC) design and manufacturing technology is growing rapidly. Advances in IC processes provide systems that operate at high speed with increasingly more complex circuits on a silicon die. While design and process technologies are growing, testing technology is struggling to keep up. Testing costs have become a major expense for IC manufacturers. Although digital circuit testing technology is quite mature, analog circuit testing is still a major challenge. Most analog IC testing is simple go/no-go based testing which can not be used for high speed devices and is becoming inadequate for complex ICs

A high frequency analog IC testing technique using a periodic input stimuli and a sequential undersampling algorithm has been developed at the University of Regina. This algorithm overcomes many of the loading problems associated with high speed analog signal testing. The utility of the undersampling technique was shown in the previous work conducted at the University of Regina using a NORTEL 1.2μm process prototype IC. This thesis expands that work by improving the performance of the original sampling circuits, investigating the possibility of generating control signals on-chip to reduce test cost, and developing a structured analog Design For Testability (DFT) approach. This approach can be used for high speed testing and is based upon wideband undersampling technique similar to those used in sampling oscilloscope and mixed-signal testers.

Structured analog DFT is a systematic approach developed to simplify the overall design and test procedures for analog and mixed-signal ICs. The most common DFT approach is to provide access to internal nodes. The problem with many of the DFT

By using the undersampling DFT approach, multiple samplers are constructed on-chip where signals being tested can be mixed-down to a lower frequency before being brought off-chip. The frequency response limitations of the off-chip driver can be avoided and access to multiple internal nodes can be provided with only a few external pins. Other advantages include small silicon overhead, low power consumption, and the potential for automated mixed-signal DFT.

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GLOSSARY OF TERMS

ADC ..... Analog to Digital Converter

ASIC ..... Application Specific Integrated Circuit

ATDI ..... Analog Test Data In

ATDO ..... Analog Test Data Out

ATE ..... Automatic Test Equipment

ATIP ..... Analog Test Input Port

ATOP ..... Analog Test Output Port

BIST ..... Built In Self Test

BiCMOS ..... Bipolar Complementary Metal Oxide Semiconductor

BS ..... Boundary Scan

CAD ..... Computer Aided Design

Cadence ..... A software design tools for the design, development, and simulation of integrated circuits

CMC ..... Canadian Microelectronics Corporation

CMOS ..... Complementary Metal Oxide Semiconductor

DAC ..... Digital to Analog Converter

DFT ..... Design For Testability

DSP ..... Digital Signal Processing

DUT ..... Device Under Test

HAST ..... High Speed Analog Signal Tester

HP ..... Hewlett Packard

IC ..... Integrated Circuit

IEEE ..... Institute of Electrical and Electronics Engineers

IEEE1149.1 ..... Standard Test Access Port and boundary-scan architecture

I/O ..... Input / Output

JTAG ..... Joint Test Action Group

MADBIST ..... Mixed Analog Digital Built In Self Test

MCM ..... Multi Chip Module

MUX ..... Multiplexer

deMUX ..... deMultiplexer

Nortel ..... A supplier of telecommunication devices in Ottawa, Ontario

PCB ..... Printed Circuit Board

P1149.4 ..... Proposed mixed-signal testability bus standard

PLL ..... Phase Lock Loop

RF ..... Radio Frequency

TAP ..... Test Access Port

TCK ..... Test Clock

TDI ..... Test Data In

TDO ..... Test Data Out

TMS ..... Test Mode Select

THD ..... Total Harmonic Distortion

VLSI ..... Very Large Scale Integration

TABLE OF CONTENTS

Chapter 1 Introduction 1

1.1 Mixed-Signal ICs and Testing Costs 3

1.2 Mixed-Signal ICs and Design For Testability 4

1.3 Digital and Analog Hardware Testers 5

1.4 Signal Buffering 6

1.5 DFT Techniques 7

1.6 Signal Probing 8

1.7 Undersampling DFT Approach 9

1.8 Thesis Coverage 10

Chapter 2 Mixed-Signal DFT Techniques 11

2.1 DFT Standards 11

2.2 DFT Techniques 13

2.2.1 Multiplexer-Based DFT 14

2.2.2 Analog-Bus-Based DFT 16

2.2.3 Scan-Path-Based DFT 17

2.2.4 Analog BIST Technique 19

2.3 Cost of Analog DFT Techniques 20

Chapter 3 High Speed Mixed-Signal DFT Technique 23

3.1 Undersampling Theory 23

3.2 Analog Signal Tester Design 29

3.2.1 OpAmp-DUT IC 32

3.2.3 Open-Front End IC 36

3.2.4 On-Chip Pulse Generator IC 38

3.2.5 Multi-Node Analog DFT IC 40

Chapter 4 Testing and Simulation Results 45

4.1 Test Signals and Equipment 45

4.1.1 Switch Control Pulses Train 46

4.1.2 Sinusoid Test Signal 46

4.1.3 Square Wave Test Signal 48

4.2 Prototype IC Testing and Simulation Results 49

4.2.1 OpAmp DUT IC 49

4.2.2 Probe-Pad IC 53

4.2.3 Open-Front End IC 58

4.2.4 On-Chip Pulse Generator IC 62

4.2.5 Multi-Node Analog DFT IC 66

4.3 Summary of Prototype and Simulation Test Results 69

Chapter 5 Conclusions and Future Work 71

5.1 Conclusions 71

5.2 Future Work 72

References .....

Appendix 1 CMOS Transmission Gate and Inverter **87**

A1.1 CMOS Transmission Gate and Inverter Layout Cellview 87

A1.2 CMOS Transmission Gate and Inverter Block Diagram 88

Appendix 2 Layout Design of CMOS Analog OpAmp and OpAmp DUT IC **89**

A2.1 CMOS Analog OpAmp Layout Cellview 89

A2.2 CMOS Analog OpAmp Block Diagram 90

A2.3 OpAmp DUT IC 91

Appendix 3 Layout Design of the Probe-Pad IC **92**

Appendix 4 Layout Design of the Open Front End IC **93**

A4.1 Layout of the Open Front End IC design 93

A4.2 Layout of a minimum dimension n-type pass gate 94

Appendix 5 Layout Design of the On-Chip Pulse Generator IC **95**

Appendix 6 Layout Design of the Multi-Node Analog DFT IC **96**

A6.1 Layout of minimum dimension n-type pass gate 96

A6.2 Layout and schematic of the analog OpAmp 96

A6.3 Layout of the Multi-Node Analog DFT IC 98

Appendix 7 THD data tables and calculations **100**

A7.1 THD of the sinusoid test signal 100

A7.2 THD of the sinusoid test signal and the output of the OpAmp DUT IC 101

A7.4 Added harmonics distortion at the output of the Open-Front End IC..... 103

Appendix 8 Schematic for a Mini-Circuits GaAs Switch.....104

Figure 2.1: Architecture of a generic mixed-signal IC 11

Figure 2.2: Block diagram showing analog test buses 13

Figure 2.3: Architecture of a Multiplexer-Based DFT technique 15

Figure 2.4: Architecture of an Analog-Bus-Based DFT technique 16

Figure 2.5: Architecture of a Scan-Path-Based DFT technique 18

Figure 2.6: Architecture of a BIST DFT technique 20

Figure 3.1: Diagram showing $f(t)$ signal being sampled to $f_s(t)$ at the rate of f_c 24

Figure 3.2: Diagram showing the sampling process 24

Figure 3.3: Spectrum of a sampled bandlimited signal 25

Figure 3.4: Spectrum of a sampled sinusoid of frequency f_i 26

Figure 3.5: Equivalent time and frequency domain of the sampling signal 27

Figure 3.6: Time domain response for undersampled sinusoid 28

Figure 3.7: Amplitude spectrum for sampled square wave of frequency f_i 29

Figure 3.8: Tester block diagram 30

Figure 3.9: Schematic for OpAmp DUT IC 33

Figure 3.10: Schematic for probe-pad IC 35

Figure 3.11: Open-Front End IC block diagram 37

Figure 3.12: On-Chip Pulse Generator IC block diagram 39

Figure 3.13: Analog DFT system block diagram 40

Figure 3.14: Schematic for one-of-four decoder 42

Figure 3.15: Symbolic schematic for the prototype IC 43

Figure 4.2: Direct sinusoid test signal compared with actual signal fed into IC die 47

Figure 4.3: Square wave generation using a GaAs switch 49

Figure 4.4: Schematic for the OpAmp DUT IC 49

Figure 4.5: Frequency response of the OpAmp DUT 50

Figure 4.6: Gain compression measurement using power sweep 51

Figure 4.7: 1dB compression point of the OpAmp DUT IC 52

Figure 4.8: Frequency response of the Probe-Pad IC measured at the output pin 54

Figure 4.9: Frequency response of the Probe-Pad IC measured at the probe pad 55

Figure 4.10: 1dB compression point of the probe-pad IC 56

Figure 4.11 Schematic for the Open-Front End IC 58

Figure 4.12: Frequency response of the Open-Front End IC on a PCB 59

Figure 4.13: Frequency response of the Open-Front End IC in Daico test fixture 60

Figure 4.14: Simulation of pulses generated by the RC circuit on the On-Chip Pulse Generator IC 63

Figure 4.15: Frequency response of the on-chip pulse generator IC with -9dBm and –15dBm input 65

Figure 4.16: Simulated frequency response of the OpAmp DUT with –20dBm input ... 67

Figure 4.17: Simulated frequency response of the OpAmp DUT on the Multi-Node DFT IC with a -13dBm input 68

Figure 5.1: Schematic for multi-tone signals generation circuit 73

Figure A1.1: The layout cellview of a CMOS transmission gate and inverter 87

Figure A1.2: Schematic for a CMOS transmission gate and inverter 88

Figure A2.2: Schematic for the CMOS analog OpAmp 90

Figure A2.3: Layout of the OpAmp DUT design 91

Figure A3.1: Layout of the probe-pad IC 92

Figure A4.1: Layout of the Open Front End IC 93

Figure A4.2: Layout of a minimum dimension n-type pass gate 94

Figure A5.1: Layout of the On-Chip Pulse Generator IC 95

Figure A6.1: Layout of a minimum dimension n-type pass gate 96

Figure A6.2: Layout of an analog OpAmp 97

Figure A6.3: Schematic for an analog OpAmp 98

Figure A6.4: Layout of the Multi-Node Analog DFT IC 99

Figure A8.1: Schematic for a Mini-Circuits ZYSWA-2-50-DR GaAs Switch 104

INTRODUCTION

Recent advances in Integrated Circuit (IC) technology have had a great impact on design and test engineers [5, 10]. Advances in integrated circuit process technologies provide circuits that operate at higher speed. The dimensions of integrated circuit features have become smaller while the IC die have become larger. Circuits on IC die have become denser and more sophisticated than ever before. According to a Semiconductor Industry Association (SIA) forecast, in the next decade, device pin counts could reach as high as 500 to 3000, operating frequencies from 225MHz to 700MHz, four to seven metalization layers, and supply voltages from 3.3 to 0.9V [8, 10, 67]. A large research effort is being carried out on developing methods for testing these ICs [3-28, 31-51, 57-69, 71-78, 96, 98-103].

In 1987, about 80% of the complex ICs being tested were purely digital. In 1990, nearly half of the ICs tested were mixed-signal devices [50]. CAD tools and fabrication technology have made it possible to integrate an entire system including digital microcontrollers, memories, analog and power devices onto a single silicon chip [50, 51, 64, 65, 67-69, 74, 94, 103]. Common mixed-signal ICs include analog circuits like Analog to Digital Converters (ADCs), Digital to Analog Converters (DACs), Phase Lock Loops (PLLs), Operational Amplifiers (OpAmps), and filters. After fabrication, analog and digital circuits are tested to verify that they meet design specifications [103]. Analog specifications are often formulated as constraints on continuous functions of independent variables such as frequency response. In mixed-signal testing, AC parameters such as;

44, 79, 85]. Analog circuit specifications are generally more complex than their digital counterpart.

There is a growing trend of embedding analog functions in digital devices [44]. The analog portion of a mixed-signal IC is actually shrinking in terms of cell count ratio and chip area. Instead, more analog functions are now being performed by digital or mostly digital circuits [4, 12, 13, 26, 28, 33, 44, 50, 51]. While decreasing the size of IC dimensions leads to higher operating frequencies, some characteristics of digital signals have to be analyzed from an analog point of view [27, 44, 53]. Testing on digital circuits is normally performed to determine the existence of catastrophic processing and manufacturing faults. Testing on analog circuits is based on a different philosophy. There are only limited standards for testing analog circuits behavior. How thoroughly a circuit is tested depends mostly on a test engineer's analog electronics and Digital Signal Processing (DSP) knowledge [36, 53]. Some of the main difficulties in dealing with analog circuit testing are as follows [3-6, 8, 9, 12, 13, 16-18, 22-25, 32-36, 41-44, 52-62, 73-76, 82-85, 96, 98-102]:

- Analog circuits have complicated input to output characteristics that may vary from one circuit to another, hence, requiring different test stimuli for testing.
- Analog circuits are susceptible to noise and electromagnetic interference and require a stable ambient environment.
- Analog circuits are often interconnected with other circuits and are not stand-alone.

normal and faulty conditions.

- Technology disparity exists between newly designed circuits and existing testing equipment (i.e. test equipment cannot keep up with the performance of new designs).

These testing difficulties have resulted in an imbalance in the levels of analog and digital testing for mixed-signal ICs.

1.1 Mixed-Signal ICs and Testing Costs

According to a recent SIA forecast, test cost will soon reach 30% of total product cost [67]. While the analog portion of an IC is comparatively small in terms of area and cell count, testing the analog portion of an IC constitutes the most expensive test costs. In general, testing costs can be classified into two categories [5, 7-10, 13-15, 20-23, 27, 37, 38, 44, 55, 67, 71, 72, 76]:

- Direct testing costs
- Indirect testing costs

Direct testing costs include the cost of the test systems used and losses due to the introduction of test circuits. Indirect testing costs include the costs for developing test programs and costs for implementing DFT. The price of an increasing number of mixed-signal devices is dominated by the cost of performing production testing [48]. Test equipment cost and the time to perform tests on the device have become one of the largest expenses of semiconductor manufacturers [5, 7, 21, 44, 48, 67, 71, 72, 76].

The technology to reduce these test costs is not keeping up with IC design, simulation and process technology. Ideally, these test costs should grow linearly along

implement Design for Testability (DFT) from the IC design stage all the way through to the production stage [8, 13, 46, 67].

1.2 Mixed-Signal ICs and Design For Testability

In order to offset increasing IC test costs, the Institute of Electrical and Electronics Engineers (IEEE) working groups 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) and proposed P1149.4 Mixed-Signal Testability Bus Standard are actively developing digital and mixed-signal test standards and testing methodologies [59, 60]. In particular, P1149.4 focuses on device and assembly level testing. Their goal is to improve testability in order to reduce test development time, testing costs, and improve test quality [59, 60].

One of the more important aspects of this work is circuit testability. DFT means adding circuitry to increase testability in order to save money in the long term [8, 67]. Based on current designs, an approximate 15% increase in circuit area is required for DFT. Unfortunately, adding test circuits increases chip area and will tremendously increase manufacturing costs for volume and area intensive ICs [8, 67].

Testability can be defined as the "controllability" and "observability" features of a circuit [3, 6-9, 11-14, 16-21, 24-28, 32-38, 44, 55-57, 61-69, 82-85]. There are four basic requirements for mixed-signal DFT techniques, they are [59, 50]:

1. Controllability of signals
2. Observability of signals

sensitive nodes

4. Expandability to cover board and system testing

Controllability is defined as the ease with which a test engineer can control signals in a circuit from the input pins while observability can be defined as the ease of determining the behavior of a circuit at the output pins [55, 95]. The added test circuit must not interfere with the normal operation of the nodes under test. DFT techniques for mixed-signal ICs should also conform to the IEEE1149.1 and P1149.4 standards for test stimuli and circuit response signals [59-60].

1.3 Digital and Analog Hardware Testers

While digital testing algorithms are well established, mixed-signal testers have yet to reach the same level of maturity [40, 42, 49, 53]. Mixed-signal testers are mostly designed to suit specific applications, for example, communication systems. These application specific testers are expensive and quickly become obsolete with technology advancement. Digital and mixed-signal testers typically cost from $200,000 to over $2,000,000 per tester. Most smaller companies can not afford to acquire these testers [42, 50, 53].

A traditional approach to mixed-signal testing has been to add some digital functionality to an analog tester. These are commonly referred to as big A/little D based testers [44]. This approach is unable to provide sufficient digital capability for most advanced processors and other equally complex ICs. These testers also may not have the digital testing edge-placement accuracy, speed, pin-count and digital time-to-market software development and debug tools to make a cost-effective test solution [44].

digital signals but is not suitable for analog signal testing [42, 44, 49]. Most digital testers are too noisy to function well in the analog realm as they often use low cost off-the-shelf switching power supplies, due to their relatively low cost [44]. Analog circuit testing requires fine signal resolution but most digital testers are unable to minimize the noise generated by the fast rise and fall times of digital signals [50]. Bid D/little A systems are also limited by their ADC and DAC resolution, and clock jitter.

Hardware and software support places additional limitations on hardware testers. Most hardware testers are microcomputer and/or DSP based test stations. DACs, ADCs, and VXI/VME buses are usually used for test station-Device Under Test (DUT) interface purposes and memory banks are allocated for data storage. A main disadvantage of all these IC testers is their lack of accessibility to internal IC nodes.

1.4 Signal Buffering

Testing mixed-signal ICs requires accessibility to internal node of the analog and digital function blocks [6, 24, 25, 53, 61, 73, 99, 102]. To examine the behavior and electrical properties at a particular node, the signal is usually buffered off chip. Buffering signals off chips suffers a number of limitations [38, 53], including:

- If analog buffers are used to drive internal signals off-chips, the frequency response of the test station is bandlimited by the response of the analog buffer.
- The capacitance and inductance of the output bonding-wire-pads, package pins, bonding wires and external equipment connections restricts the level of test performance.

internal DUT [4, 69].

- At least one input/output (I/O) pin is required for each node under test.
- Additional test circuits increase chip area and power consumption.

Signal buffering may generally be used for only low frequencies applications with a small number of analog circuits.

1.5 DFT Techniques

The most common mixed-signal DFT approach is the divide and conquer approach [6, 13, 24, 25, 40, 53, 55, 56, 61, 95, 99, 102]. During system design, both digital and mixed-signal designs are partitioned into smaller parts called macros [24, 25, 53]. The main goal for systems partitioning is to enhance accessibility directly to the module under test. Partitioning tries to minimize dependency between modules and limit test complexity. The response of each module can be observed at its output boundary by applying stimuli at its input boundary.

DFT techniques can be divided into two categories; ad hoc techniques and structured approaches [24, 25]. Structured approaches can be applied to a wide range of designs and circuits to reduce complexity and aid test stimuli generation and verification [95]. Four of the most common structured mixed-signal DFT approaches are [24, 25, 53]:

1. Multiplexer-based DFT scheme
2. Analog-bus-based DFT scheme
3. Scan-path-based DFT scheme
4. Analog Built-In-Self-Test (BIST) scheme

design [6, 24, 25, 53, 62, 68]. With the addition of a few test busses and/or on-chip switches, test stimuli can be transported to the DUT and the response signals can be brought off-chip to be analyzed. One of the main concerns in applying these DFT techniques is the loading factor at the node under test. Inclusion of DFT test circuits tends to load the node under test, making high frequency measurements difficult if not impossible. Other limitations of these approaches can include large chip overhead and power consumption.

Another approach to ease testing demand is to place circuitry on the devices to test themselves. This structured approach is referred to as Built In Self Test (BIST) or Mixed Analog Digital Built In Seft Test (MADBIST) [17, 39, 47, 55, 64, 74]. The DUTs' responses are compared to a known correct circuit response for verification. One of the advantages of applying BIST or MADBIST is that several DUTs can be run in parallel to save test time and costs. The main disadvantage is that this approach is meant for go/no-go type testing and not for performance diagnosis based testing.

1.6 Signal Probing

The most common way to measure the signal level at a node is to probe it. Analytical and production probing can be used to detect faults, wafer defects and signal extraction. However, analytical and production probing requires small probe pads at each node under tests. Even though probe pads' dimensions are relatively small compared to bonding pads, the associated parasitic capacitances can greatly reduce the performance at the node under test [4, 9, 19, 29, 48, 53, 62].

heterodyne electrostatic force microscopy are examples of contactless measurement systems that reduce loading effects at the node under test [4, 53, 93]. However, probing techniques, using either direct contact or contactless probing require accurate positioning mechanisms and are time consuming. Probing is not generally an effective production test solution, especially for smaller sized companies.

1.7 Undersampling DFT Approach

Most of the DFT approaches mentioned above are not feasible for testing high speed signals. Loading effects on the node under test limit an IC's performance. Adding the circuitry on chip leads to larger integrated circuit silicon area and increases parasitic loading. In order to test larger mixed-signal die at high operating speed, these factors need to be minimized. One of the solutions to reduce these effects is to undersample the on-chip signals [38, 44, 53]. This technique is commonly used with signals whose frequency components exceed the maximum sampling capability of a waveform digitizer [16, 20, 38, 44, 53, 75, 100].

A High-speed Analog Signal Testing (HAST) procedure has been developed at the University of Regina [38, 53]. This undersampling testing technique was successfully demonstrated using NORTEL's 1.2μm CMOS technology. An OpAmp was used as an on-chip DUT and it's -3dB bandwidth and slew rates were measured.

In its simplest form, the HAST procedure can be implemented in a design by adding two components on-chip: an analog switch to sample the response signal at a particular node under test and a buffer to drive the sampled values off-chip [38, 53]. The

and driven off-chip at low frequency.

The HAST procedure employs a "Trickle Charge" technique in order to minimize loading at the node under test [38, 53]. To achieve this, narrow sampling pulses are required to close an analog sampling switch momentarily. When the analog switch is closed for a very small time, only a small amount of charge is transferred from the node under test, which keeps loading on the test node to a minimum. This thesis expands the original research work to further minimize the loading effects on the test nodes and investigated the performance of the sampling circuits. A prototype IC was also designed to investigate the possibility of generating control pulses on-chip.

The original HAST approach uses two input pins and an output pin to test a DUT [53]. If the number of device to be tested is increased, this approach is not feasible. The silicon area occupied by the additional circuits and bonding wire pads; as well as, the number of input/output pins have to be reduced. This thesis will review further improvements to the original HAST procedure including a DFT approach to provide access to multiple nodes under test.

1.8 Thesis Coverage

This chapter has provided an overview of analog and mixed-signal ICs testing. Chapter 2 describes in further detail common DFT techniques. Chapter 3 explains the HAST procedure and its use in a wideband undersampling DFT approach. Test measurements and simulation results are covered in chapter 4. Chapter 5 provided a conclusion of the research and proposes future work that should be considered.

MIXED-SIGNAL DFT TECHNIQUES

2.1 DFT Standards

Analog circuit testing is a complex procedure as circuits are usually connected sequentially between the primary inputs and outputs forming a daisy chain of analog circuit blocks. When an IC has both digital and analog circuitry, using the IEEE 1149.1 Test Standard, the two portions are separated by Boundary Scan (BS) cells at the digital/analog interface (see figure 2.1) [24, 25, 94, 102]. The analog portion is further divided into smaller functional units called macros [6, 102]. Each macro is typically equivalent to an analog module available from a design library [24, 25, 94].

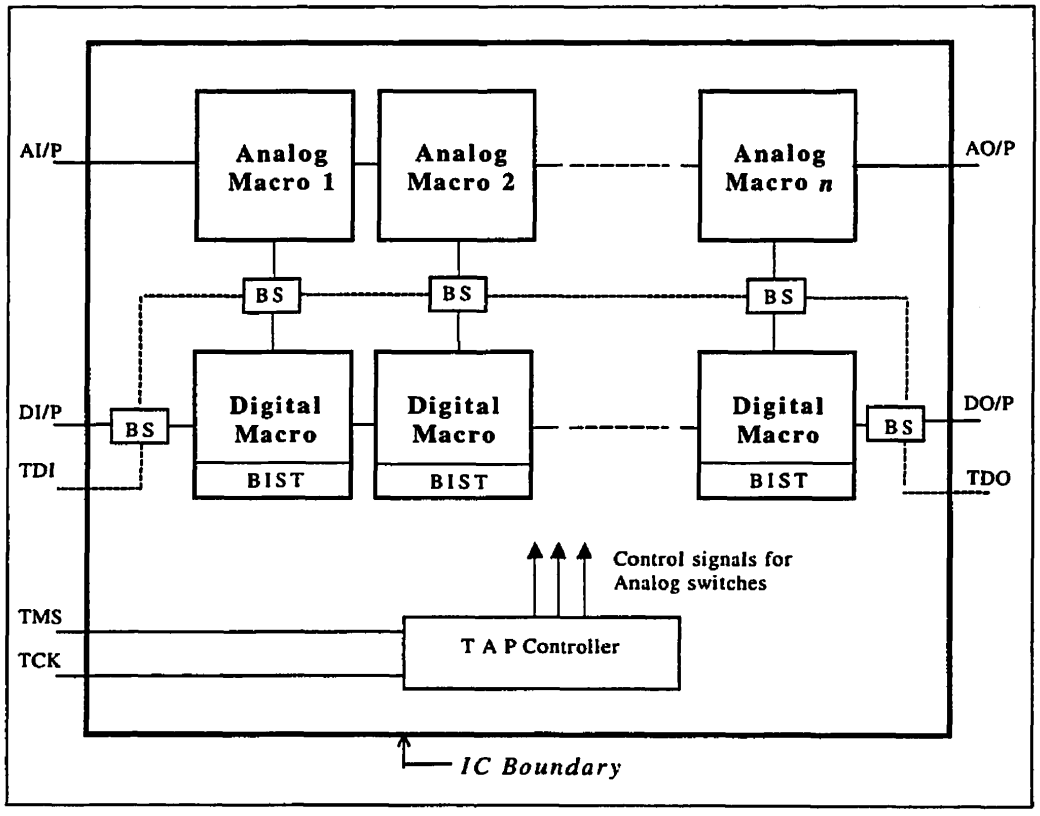

Figure 2.1 Architecture of a generic mixed-signal IC [24].

Outputs (AO/P), Digital Inputs (DI/P), and Digital Outputs (DO/P) [24, 25]. Access to internal nodes is commonly provided through analog switches that are incorporated within each macro. The control signals for the analog switches are digital and are obtained via the IEEE 1149.1 Test Access Port (TAP) controller using Joint Test Action Group (JTAG) bus [6, 24, 25, 61, 73, 99].

The JTAG bus is a serial bus containing four signal lines: Test Data In (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK) [24, 25]. Two optional lines, Analog Test Data In (ATDI) and an Analog Test Data Out (ATDO), are used to transport analog test signal to the analog macros and capture the response of the analog macros [24, 25].

Since the analog portion of a mixed-signal IC is more complex and expensive to test, most of the proposed mixed-signal IC DFT techniques focus on analog DFT techniques [24, 25]. There are two approaches to observing the results of the analog test [8, 24, 25, 35, 47, 61]:

- By employing voltage or current capture stations which are similar to Built In Logic Block Observers (BILBOs) in the digital domain, and
- to route the output signals onto an analog test bus so that the circuit response can be evaluated off chip.

Some aspects of analog DFT are being incorporated into a proposed Analog Test Bus Standard, P1149.4 [24, 25, 61]. The proposed 1149.4 Standard is based on a mixed-signal test bus which provides three test features; interconnect test, component/cluster test, and IC/macros test [56, 61]. One of its primary objectives is to test the IC and its

[56]. The P1149.4 Standard uses an interface that is common for both analog and digital signals. It provides a digital control mechanism coupled with analog test paths which can incorporate boundary scan to provide testing and diagnosis [61]. The test stimuli and responses are transported via the analog test buses (see figure 2.2) [56]. The buses are routed near the analog macros such that each analog macro can access the buses.

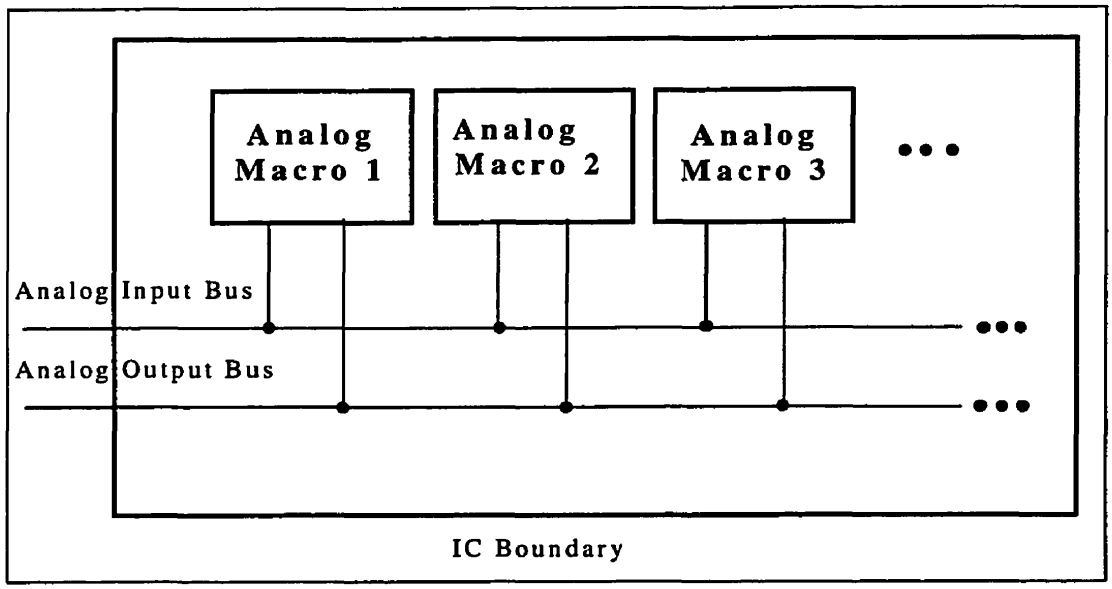

Figure 2.2 Block diagram showing analog test buses

Ideally the test scheme should not degrade the operation of the analog sub-macros during system operation. The integrity of signals during test should also be preserved [24, 25].

2.2 DFT Techniques

There are four basic analog DFT techniques which can be used independently or in combination with IEEE1149.4 Test Standards and P1149.4 Standards [6, 24, 25, 73]. The four basic techniques are as follows:

1. Multiplexer-based DFT technique

3. Analog shift register/analog scan path DFT technique
4. Analog BIST technique

All four DFT techniques enhance testability and also provide access to the analog macros. Each technique has its own advantages and disadvantages. In each of the above technique, the control signals are digital and can be scanned in via the IEEE1149.1 TAP [24, 25]. The four DFT techniques can be mixed and matched to select the most effective test strategy for a mixed-signal IC [24, 25]. Since the analog portion of an IC consists of small macros, analog DFT strategies are similar to the divide and conquer technique in digital testing [24, 25]. The four DFT techniques are generic and can be applied to a large class of devices. They provide a structured approach for testing an IC's internal nodes [5, 6].

2.2.1 Multiplexer-Based DFT

In multiplexed-based DFT, the controllability and observability of internal nodes is increased by placing analog MUXes at each analog macro (see figure 2.3) [1, 4-8]. The MUX at the front end of each macro determines the mode of operation, either normal operation mode or test mode. The output response of the macro is observed by using an analog MUX, which is connected to all of the macro outputs [5,6]. This output MUX determines which analog macro's responses is to be observed during test mode.

During test mode, the front-end MUX will route the analog input bus to the input of the analog macro under test; and the output MUX will route the response of the analog macro under test to the output port [6, 24, 25, 61]. During normal operation mode, all the

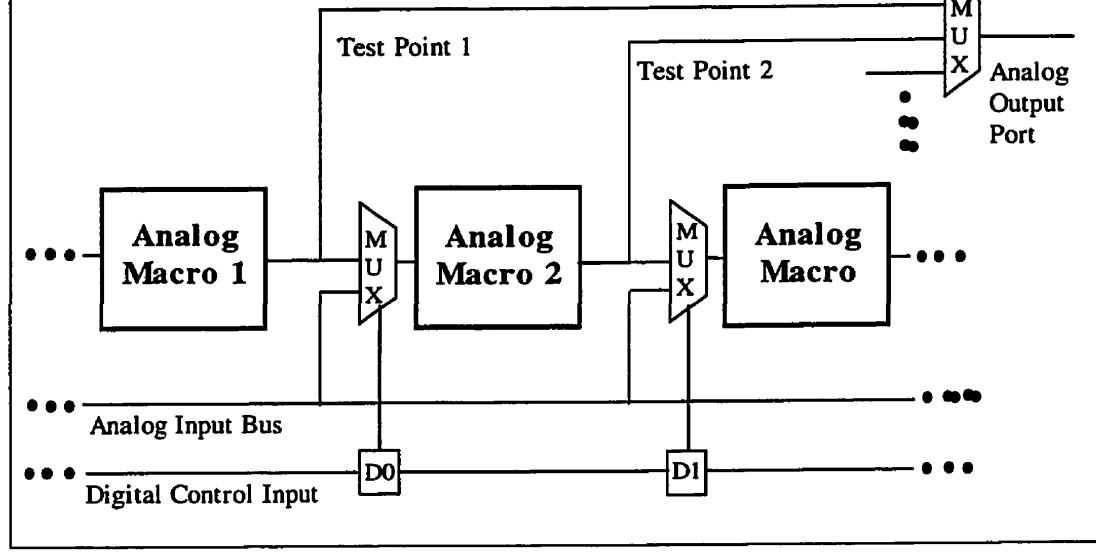

Figure 2.3 Architecture of a Multiplexer-Based DFT technique

front-end MUXes will route the output of the previous stage analog macro to the input of the analog macro. This scheme can selectively test individual macros and hence can be used for circuit diagnosis [5, 6].

There are several limitations of using this DFT technique. Adding MUXes on chip occupies costly chip area. This technique is band-limited by the response of the MUXes added to the macros and is generally not suitable for high frequency testing. In general, a primary input of an analog macro requires signals from the primary output of another analog macro and may require feedback connections and resistance termination. If no sampling algorithm is applied to the output MUX, analog signals may be loaded or by-passed by the MUXes. Hence, this technique may not be suitable when all analog macros need to operate in normal operation mode.

This DFT technique uses analog buses with analog switches to drive and sense one or more macros [6, 34]. These test buses provide controllability and observability to resources outside of the IC (see figure 2.4) [24, 25, 61]. The interface between the analog macros and the test busses is normally controlled by using transmission gates or pass-gates.

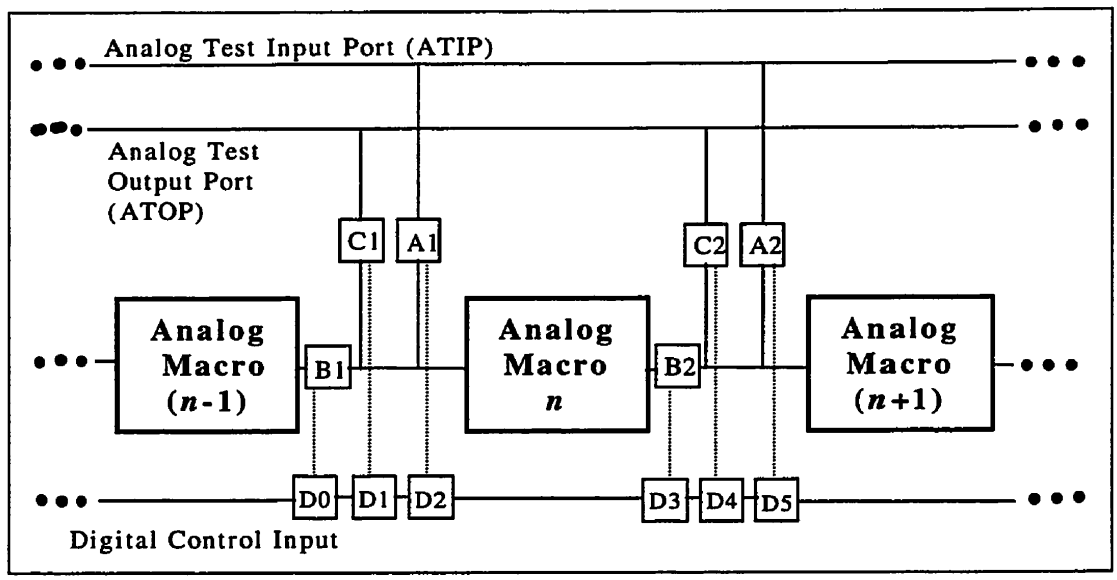

Figure 2.4 Architecture of an Analog-Bus-Based DFT technique

From figure 2.4, Analog Test Input Port (ATIP) and Analog Test Output Port (ATOP) are two analog busses used with analog switches to access analog macros [24, 25]. The test stimuli transported through ATIP can be routed to the analog macro under test by opening and closing the appropriate switches. The response of the analog macro under test can be observed in the same manner. High performance of the transmission gates or pass-gates is required because multiple gates are connected to the busses, thereby increasing the circuit loading [24, 25].

applied to macro *n* from ATIP by closing switch A1 and opening switch B1 and C1. The output of macro *n* is observed at ATOP by closing switches B2 and C2. All other switches are opened. To test more than one macro at a time, appropriate combinations of switches will have to be opened or closed.

Tung et. al. have proposed a modified test bus approach using an ADC and external DSP processor for production go/no-go type analog circuit testing [102]. In this scheme, test stimuli are fed into the macro under test and its response is routed to a DAC by opening and closing the appropriate bus-routing-switches. The output of the DAC can then be analyzed by a DSP unit. This scheme digitizes on-chip signals to eliminate package pin loading of the macro under test. This technique requires an on-chip ADC resulting in increased silicon area. It is also limited by the resolution of the ADC and its sampling rate [102].

The analog bus technique gives controllability and observability for each analog macro. It also gives the added flexibility of test combinations of macros. The limitations these DFT technique include at least two analog switches are needed to test a macro. This results in metal interconnect routing complexity and increasing silicon area. High speed performance of the DFT technique is limited by the performance of the analog switches and the loading of the analog busses and off-chip loading added to the macros.

2.2.3 Scan-Path-Based DFT

For the scan-path technique, a serial path of analog switches is used to apply the test inputs and measure the output response (see figure 2.5) [24, 25]. This technique gives observability and controllability to an individual analog macro or a combination of

which are not under test can be disconnected or bypassed [24, 25].

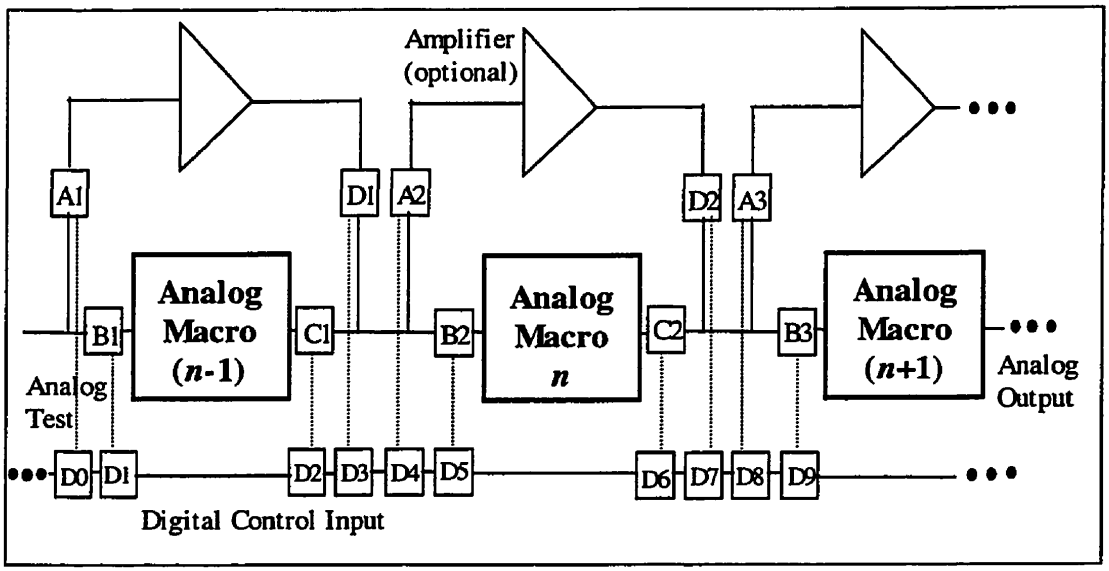

Figure 2.5 Architecture of a Scan-Path-Based DFT technique

For example, to test analog macro *n*, all other macros are bypassed using appropriate switches. Switch B2 is closed to apply the test signal and switch C2 is closed to observe the output while switches A2 and D2 are opened. If the chain is too long, or if there is performance degradation along the path, amplifiers can be used to preserve the signal integrity [24, 25].

This scheme gives flexibility in terms of which macros' response is to be tested. Limitations of this DFT include:

- If the scan chain is too long, adding amplifiers takes up additional silicon area.
- At least 3 analog switches are added to a macro resulting in complex metal routing and increasing silicon area.

analog switches and is band-limited by the amplifiers frequency response if they are used [24, 25].

2.2.4 Analog BIST Technique

A few DFT techniques were proposed by the educational and research community for testing analog circuits on-chip. A number of these DFT techniques can be classified as analog BIST techniques based on go/no-go testing. Typically, BIST is used at the device level to solve device level test problems including lack of pin access, ability to carry out at-speed tests and improved diagnosis.

BIST builds the key functions of an external tester directly into a silicon device allowing it to test itself [15, 17, 39, 47, 61, 64, 68, 74, 76, 87, 97]. These functions include a source of test stimuli, a means of capturing the circuit response, a knowledge of correct response from the circuit under test, and a self test controller. There are two main methods for observing and determining a pass/fail response of the device under test:

- To compare the observed response with expected response in real time, and
- to apply data compression algorithm to the observed response forming a signature and then compare the final signature with expected response.

A basic BIST architecture is shown in figure 2.6.

Lubaszeski et. al. and Renovell et. al. proposed analog signature analyzers using an integration function as the compression technique [35, 47]. Using a multiple-input analog signature analyzer, access to internal nodes can be provided.

Analog BIST is useful for testing very dense Application Specific Integrated Circuits (ASICs) as most macros can be tested in parallel, as long as the testing procedure

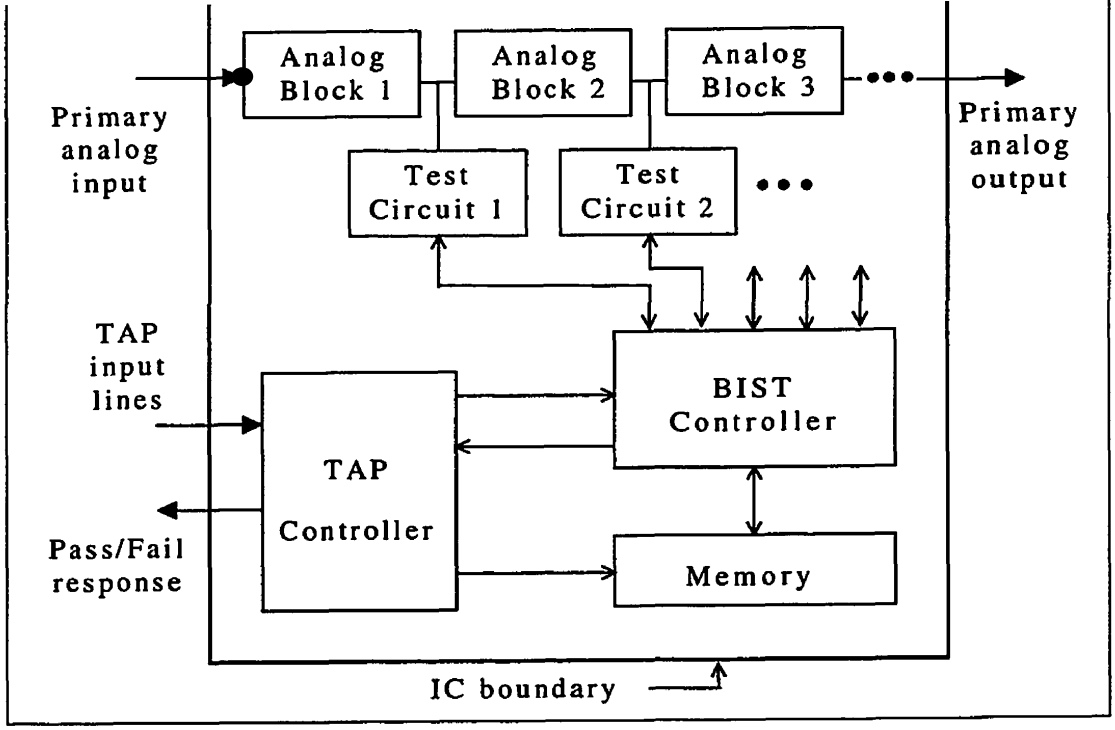

Figure 2.6 Architecture of a BIST DFT technique

does not exceed the device's maximum power consumption. The main drawbacks of analog BIST are its low speed performance and typically large chip area required. The final product of a BIST test is a pass or fail response as opposed to a performance diagnosis [61, 102].

2.3 Cost of Analog DFT Techniques

In general, mixed-signal DFT techniques should fulfill the following basic requirements:

1. Minimum impact on the system performance
2. Low chip area overhead
3. Low power consumption

additional routing metal), must add minimal loading to the analog macros under test. Without a proper sampling algorithm or isolation between the macro under test and the off-chip circuitry, DFT techniques are limited by the response of the buffers and switches. Adding test circuitry on-chip always increases silicon chip overheads as test MUXes, buffers and switches occupy additional chip area. In addition, the number of pins dedicated for testing purposes should be minimized to avoid increased I/O pads and package costs. Table 2.1 shows the advantages and disadvantages of the four DFT techniques mentioned in the previous section.

Table 2.1 Advantages and disadvantages of the current DFT techniques

DFT technique:	**Advantages and disadvantages:**
Multiplexer-Based DFT	Can selectively test individual macros. MUXes take up chip area. Band-limited by the response of the MUXes and not suitable for high speed testing.
Analog-Bus-Based DFT	Provides access to individual or combination analog blocks. Placement of analog switches may result in routing complexity and take up chip area. Limited by the performance of the analog switches.

DFT technique:	Advantages and disadvantages:
Scan-Path-Based DFT	Provides access to individual or combinational analog blocks. May result in routing and interconnect complexity. If amplifiers are used, the performance of the DFT is band-limited by the amplifiers and take up extra chip area. Limited by the performance of the analog switches.
Analog BIST Technique	Analog macros can be tested in parallel. Low speed performance and large chip area. Only provide pass/fail end result.

HIGH SPEED MIXED-SIGNAL DFT TECHNIQUE

A high speed analog testing technique, based upon an undersampling approach, was developed at the University of Regina and a thesis was published by Simon et. al. in 1995 [38, 53]. This new testing technique may be useful for enhancing existing analog testing procedures, and for implementing a structured DFT approach for mixed-signal ICs where multiple on-chip nodes can be examined by incorporation of a number of on-chip undersamplers.

3.1 Undersampling Theory

The utility of the undersampling approach for analog IC testing has been investigated by B. Simon et. al. [38, 53]. The testing approach was developed based upon wide band undersampling techniques similar to those used in sampling oscilloscopes and mixed signal IC testers [16, 20, 38, 53, 75, 88, 89, 100, 105]. Using a sequential undersampling algorithm to control a switch, high frequency periodic signals can be mixed down in frequency and driven off-chip using a low bandwidth buffer [16, 20, 38, 53, 75, 88, 89, 100, 105]. Using this approach, the frequency response limitations of the off-chip driver can be avoided.

Assuming $f_o(t)$ is the output of a continuous varying signal $f_i(t)$ which is being sampled at a rate of f_c samples per second (see figure 3.1 and 3.2). The sampled signal $f_o(t)$ can be represented in terms of $f_o(t)$ [16, 20, 38, 52, 53, 75, 88]

$$f_o(t) = f_i(t)S(t) \tag{3.1}$$

where $S(t)$ is a periodic series of pulses of unit amplitude, width τ, and period $T = 1/f_c$.

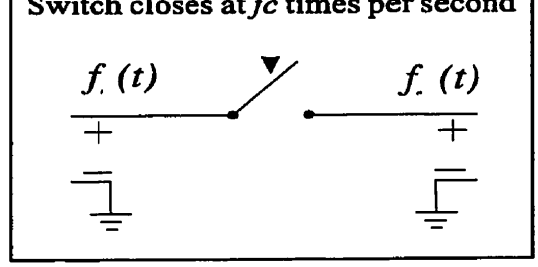

Figure 3.1 Diagram showing $f_i(t)$ signal being sampled to $f_o(t)$ at the rate of f_c

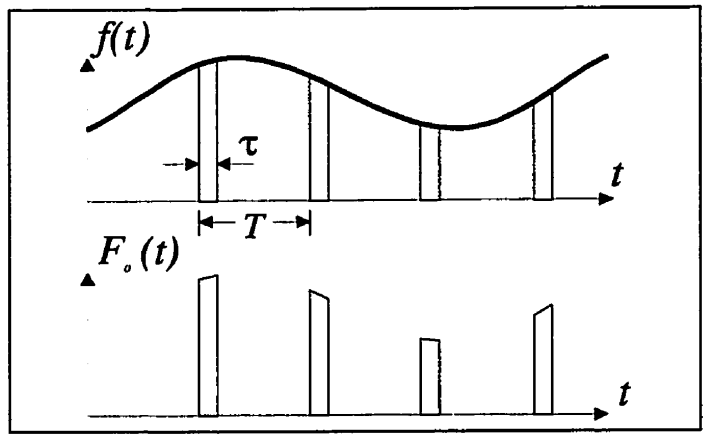

Figure 3.2 Diagram showing the sampling process

From the frequency convolution theorem, the product of the two time domain functions $f_i(t)$ and $S(t)$, is equivalent to the convolution of the respective Fourier transforms $F(\omega)$ and $S(\omega)$ [52, 75].

$$G(\omega) = \frac{1}{2\pi} F(\omega) * S(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(x) S(\omega - x) dx \qquad (3.2)$$

Ideally, the sampling time (τ) of the periodic sampling function $S(t)$ equals 0. Its Fourier transform $S(\omega)$ will be undiminished power components extending to infinity, and equally spaced at intervals of $1/T$ (see formula 3.3).

$$S(\omega) = 2\pi d \sum_{n=-\infty}^{\infty} \left(\frac{\sin n\pi d}{n\pi d} \right) \delta(\omega - n\omega_c) \qquad d = \frac{\tau}{T} \qquad \omega_c = \frac{2\pi}{T} \tag{3.3}$$

When τ is non-zero and as τ increases, the high frequency components of $S(\omega)$ decrease. In a practical sense, τ will never be 0, resulting in amplitude and phase distortion in $S(\omega)$ [36, 75]. Note that the amplitude of the sampling signal is attenuated by a factor of $\sin(n\pi d)/n\pi d$. Substituting equation 3.3 into equation 3.2 and noting that:

$$\int_{-\infty}^{\infty} F(x)\delta(\omega' - x)dx = F(\omega') \tag{3.4}$$

will yield:

$$G(\omega) = dF(\omega) + d \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \frac{\sin n\pi d}{n\pi d} F(\omega - n\omega_c) \tag{3.5}$$

Using the Fourier transform $G(\omega)$ derived in equation 3.5, the spectrum of a band-limited input signal of bandwidth B, sampled at f_c, is shown in figure 3.3. Note that the amplitude of the sampled signal is also attenuated by a factor of $\sin(n\pi d)/n\pi d$.

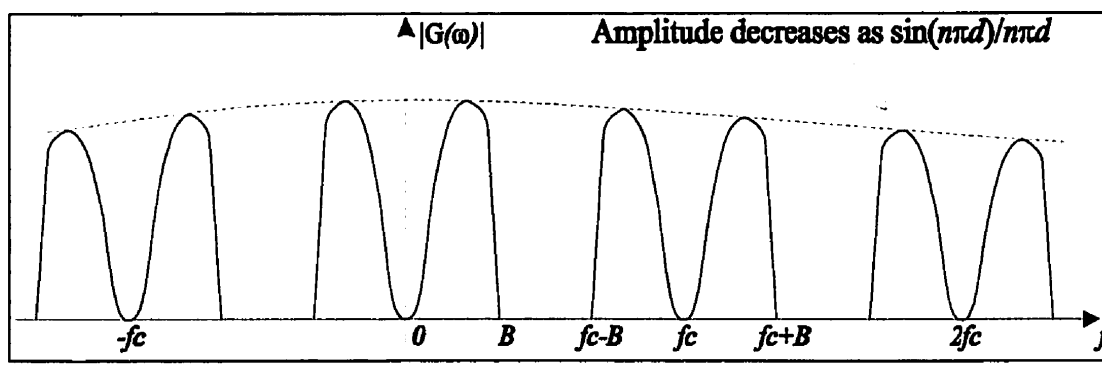

Figure 3.3 Spectrum of a sampled bandlimited signal

prevent aliasing of higher frequency Fourier components into the band-limited signal, the sampling frequency f_c must be at least two times the maximum input signal frequency [16, 20, 52, 75, 88]. The signal is considered undersampled if the input signal has a frequency component greater that $f_c/2$ [16, 20, 52, 75, 79, 88].

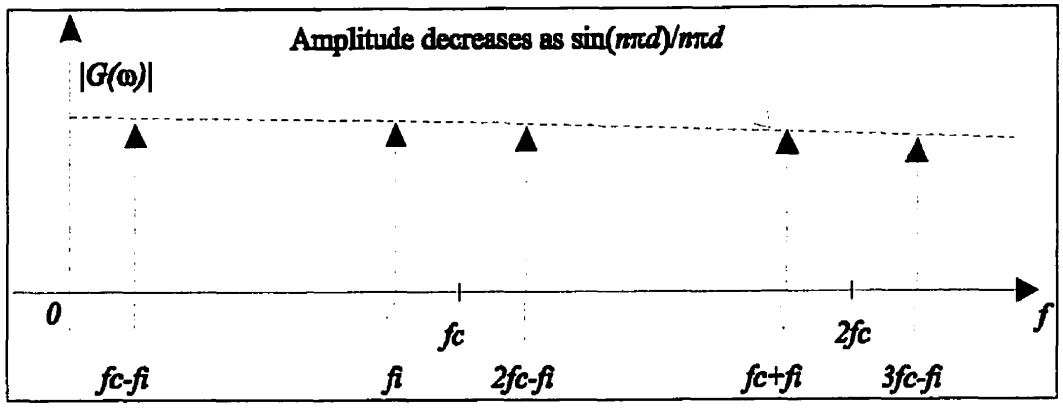

Figure 3.4 Spectrum of a sampled sinusoid of frequency f_i

For an input sinusoid of frequency f_i, where f_i is greater than $f_c/2$, the positive frequency components of the sampled signal can be seen in figure 3.4 [16, 20, 38, 75, 88]. The f_c-f_i component is a replica of the original sinusoid input signal f_i shifted down in frequency. If the input signal frequency is known in advance, and the sampling frequency is selected to be very close to the input signal frequency, the resulting component f_c-f_i is at a much lower frequency than the input signal [16, 20, 36, 52, 53, 75, 88]. This f_c-f_i component can then be extracted from the other power components with a simple filtering process and driven off-chip with minimal loading effects [38, 53].

In Simon et. al., filtering processes were conducted by choosing the input signal to be very close to the sampling frequency. The resulting component, f_c-f_i was brought off chip for analysis. For every input signal of frequency f_i, a corresponding sampling

also be sampled by any of the harmonics of the sampling frequency f_c. As long as the input signal is close to nf_c (where n = 1, ..., ∞) and the resulting component f_c-f_i is within the bandwidth of the output buffer, the component f_c-f_i can be buffered off-chip for analysis. The sampling process using harmonics of the sampling frequency f_c is based on the same theory used in heterodyne conversion for microwave frequency counters [16, 20, 36, 52, 75, 88, 104, 105]. The prototype testing covered in this thesis applied the sampling process using sampling signal f_c or any of its harmonics.

If $S(t)$ is a periodic pulse train as shown in figure 3.5; the Fourier transform $S(\omega)$ will have power components evenly spaced at $f_s = 1/T$. Input signal f_i can be sampled at nf_c where n = 1,.., ∞. Using this method, if f_c is a periodic series of pulses, only the input test signal needs to be adjusted to be close to f_c or any of its harmonics. The drawback of using this method is that the harmonics of nf_c are attenuated by a factor of $\sin(n\pi d)/n\pi d$. If the sampling time (τ) is small, the effect of $\sin(n\pi d)/n\pi d$ is reduced.

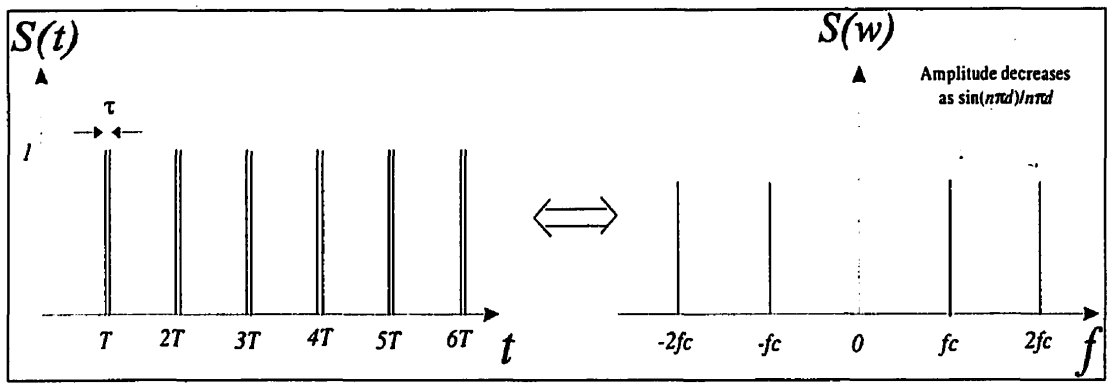

Figure 3.5 Equivalent time and frequency domain of the sampling signal

In the time domain, the slight offset between f_c and f_i means the sampling pulses are tracing a complete signal waveform [38, 53, 88, 105]. If the difference between f_c

waveform cycle.

For example, a 11.25MHz input test signal with a 10MHz sampling frequency is shown in figure 3.6. The two signals will be moving (1/10MHz-1/11.25MHz)=11.11ns relative to each other for every cycle of the switch. It takes a total of 88.88ns/11.11ns = 8 samples to represent one complete cycle of the input signal. The output signal will have a frequency Δf = 1.25MHz.

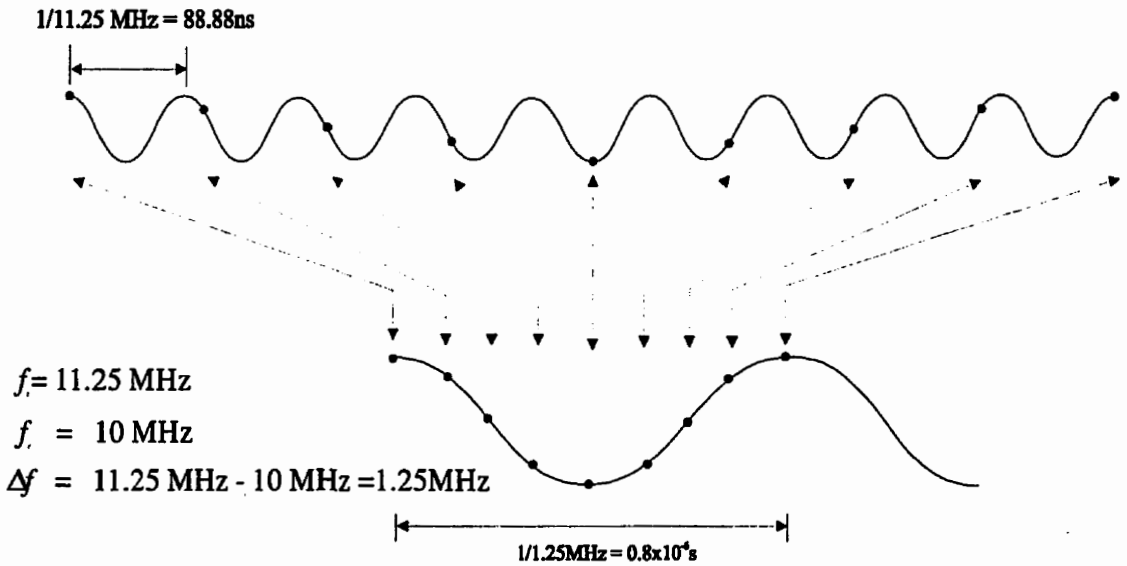

Figure 3.6 Time domain response for undersampled sinusoid

The undersampling approach is also valid for measuring wideband signal [16, 20, 38, 53, 75, 88, 105]. For a 50% duty cycle input square wave of frequency f_i and a sampling rate of f_c (see figure 3.7), the low frequency components (0, Δf, $3\Delta f$, $5\Delta f$, ...) are the replica of the input square wave shifted down in frequency. Aliasing of the higher frequency components occur at $nf_c/2$, where n = 1,...,∞. If the frequency difference f_c-f_i is

negligible effect on the overall response.

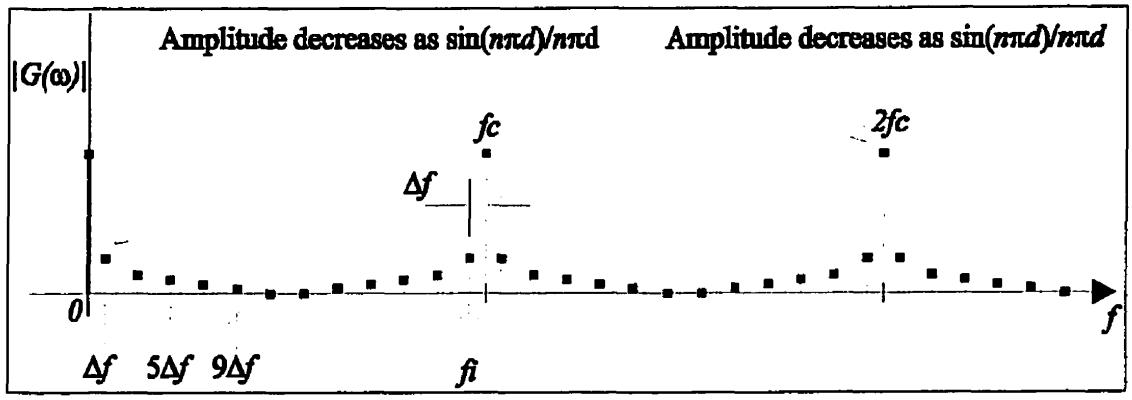

Figure 3.7 Amplitude spectrum for sampled square wave of frequency f_i

The advantage of using the simple repetitive signals discussed above is that the basic operating characteristics of a DUT can be determined from the system response. A sinusoidal frequency sweep can be used to determine AC parameters such as frequency response and harmonics distortions. Square waves can be used to measure transient parameters such as slew rate, overshoot and settling time.

3.2 Analog Signal Tester Design

In its simplest form, only three components are required on-chip to carry out the test procedure (see figure 3.8) [38, 53]. The first component is an analog switch. The switch is used to sample the on-chip test signal at the node under test. The sampled values are then stored on the second component, a hold capacitor. The capacitor is to hold the sampled values and minimize error due to charge redistribution. The size of the capacitor can be determined through simulation. The third component is an OpAmp which is used as an output buffer to drive the sampled values off-chip. There are four

- Repetitive input signals
- Narrow pulse on switch control
- Small frequency shift between the input signal and the switch control
- On-chip hold capacitor

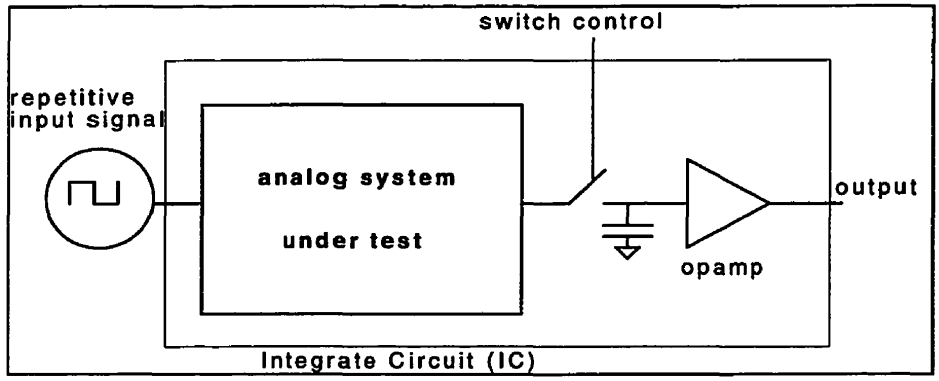

Figure 3.8 Tester block diagram

By applying a repetitive input signal of known frequency, the response of the analog system will be a lower frequency replica of the input signal [38, 53]. If the test signal and a harmonic of the sampling signal have a small frequency difference Δf, the frequency response limitation of the output buffer can be avoided. The power consumption of the output buffer will also be reduced as the output signal is of much lower frequency than the test signal.

One of the key aspects of DFT is to minimize circuit loading to the node under test. Using an undersampling approach, minimal loading on the node under test is achieved when narrow pulses (typically 2ns or less) are applied to the switch control signal. Narrow pulses allow a small amount of charge to pass through the switch on each pulse. With the sampling switch being closed only momentarily, the loading on the node

sampling switch input. The momentarily charging technique is called trickle charging [38, 53].

If the rise and fall time of the sampling pulses is short and sampling time (τ) is small, the harmonics of f_c can be used to sample the test signal. High quality pulses are required to produce meaningful f_c-f_i components. Poor quality pulses can produce spectral components other than nf_c and increase $\sin(n\pi d)/n\pi d$ attenuation. This will result in added noise and distorted output signals.

In CMOS technology, the analog switch is commonly implemented with a transmission gate or a single pass transistor. In BiCMOS technology, a higher performance switch can be implemented using a diode bridge. By minimizing the geometry of the switch and applying the trickle charge technique, the loading on internal test nodes can be kept to a minimum.

The on-chip holding capacitor is used to integrate the trickle charge through the analog switch [38, 53]. The capacitor is also used to reduce charge coupling capacitance between the switch control signal and the output of the analog switch. The switch will also filter out undesired high frequency components of the sampled signal. Some of the limitations of the undersampling approach include:

- Undersampling approach requires a continuous and repetitive input signal.
- By mixing signals down to lower frequencies, the sample capturing time (i.e. testing time) is increased.

- A high performance pulse generator is required for high frequency measurements.

Table 3.1 summarizes the prototype ICs designed for testing and simulation purposes.

Table 3.1 Summary of prototype IC designs for simulation and testing

IC design name:	Purpose:
OpAmp DUT IC	To validate the concept of the undersampling technique approach for high speed testing.
Probe-Pad IC	To compare the results obtained using the OpAmp DUT IC with the results obtained from the probing technique.
Open-Front End IC	To test the performance of the sampling switch
On-Chip Pulse Generator IC	To generate control pulses on-chip and compare the test results with the results obtained using the Open-Front End IC
Multi-Node Analog DFT IC	To implement the undersampling approach for multi-node testing architecture

3.2.1 OpAmp DUT IC

An IC was designed by Simon et. al. using Cadence design tools and fabricated using Nortel's 1.2μm CMOS process which was provided through CMC [53]. The

validate the concept of undersampling approach and its utility for a high speed testing environment. A sinusoid signal was used for AC measurements and a square wave was used for transient measurements. Simulation results and prototype testing results were also reported [53].

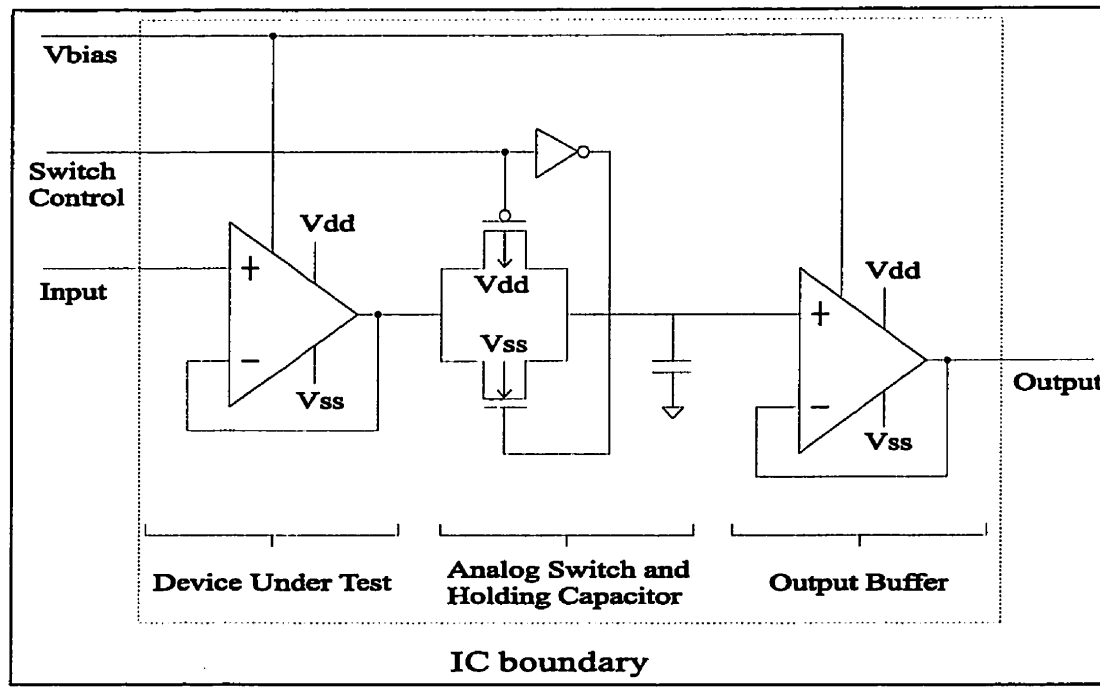

Figure 3.9 Schematic for OpAmp DUT IC

The IC contained three main circuits [18]. The first circuit was a transmission gate and an inverter which were used as an analog switch. The layout and schematic of the transmission gate and the inverter are attached in Appendix 1.1 and 1.2 respectively. The output of the transmission gate was connected to a 0.95pF hold capacitor. The second circuit was a unity gain OpAmp which was used as an buffer to bring the sampled signals off-chip. The layout and schematic of the OpAmp are attached in Appendix 2.1 and 2.2 respectively. The third circuit was an identical unity gain OpAmp which was

examined. The layout design of the OpAmp DUT design is shown in Appendix 2.3. Note that due to the arrangement of the inverter at the transmission gates, samples are taken at the node under test when there is a low signal pulse at the control switch. When the control switch signal level is at the V_{dd} power rail, the analog switch is opened.

The total silicon area occupied by the test circuitry (output buffer, holding capacitor and sampling switch) is 90μm x 185μm. The area occupied by the OpAmp DUT is 80μm x 140μm. The channel width and length of the transmission gates are listed in table 3.2 below:

Table 3.2: Dimensions of the source region of the CMOS transmission gate

	W (μm)	L (μm)
N-type	12.0	5.0
P-type	32.1	5.0

The loading at the node under test was calculated as 0.12pF [18]. A total of three pins were required for testing purposes:

- Repetitive input stimuli
- Control switched
- Output pin

3.2.2 Probe-Pad IC

An second IC was also designed by Simon et. al. using Cadence design tools and fabricated using Nortel's 1.2μm CMOS process. The prototype IC was not tested and was not included in Simon et. al.'s thesis. The schematic of the design is shown in figure 3.10. The IC design was exactly the same as the OpAmp DUT IC with the addition of a 40μm x 40μm probing pad. With the probing pad, the signal at the node under test could

was to compare the results obtained using undersampling technique with the results obtained from the probing technique.

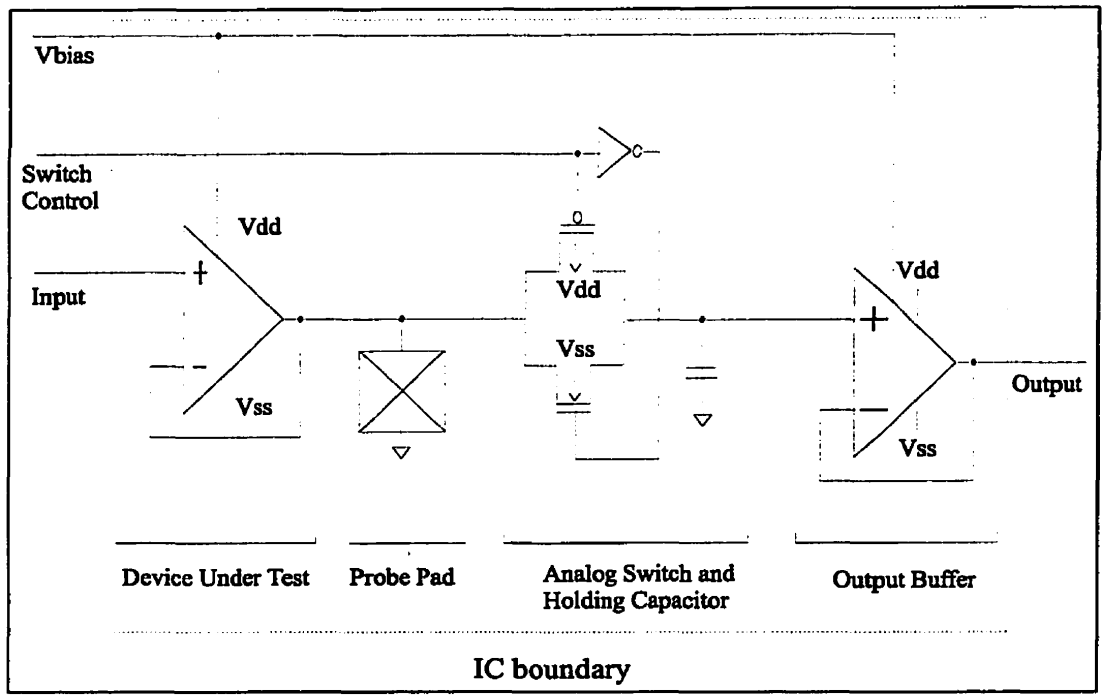

Figure 3.10 Schematic for Probe-Pad IC

The inclusion of the probe pad increases the loading on the node under test due to the parasitic capacitances of the probe pad and probe tip. The layout of the design can be found in Appendix 3. For Nortel's 1.2μm CMOS4S process, the parasitic capacitances due to the probe pad can be calculated by using the following formula [107]:

$$C_d = C_{ja}\,(a\,b) + 2C_{jp}\,(a + b) \qquad (3\text{-}6)$$

Where

C_{ja} = 2.7×10^{-5}pF/μm^2 = capacitance per unit area of metal layer,

C_{jp} = 0.4×10^{-4}pF/μm^2 = periphery capacitance per unit length of metal layer,

b = length of the probe pad.

The total parasitic capacitance was calculated as [53]:

$C_{total} = 0.12pF+(2.7x10^{-5}pF/\mu m^2)x(40\mu mx40\mu m)+2x(0.4x10^{-4}pF/\mu m^2)x(40\mu m+40\mu m)$

$= 0.17pF$

Note that this result does not take into account the metal routing capacitance.

3.2.3 Open-Front End IC

The test circuitry described in section 3.2.1 is capable of measuring higher speed signals but is limited by the frequency response of the OpAmp DUT. A third IC was designed using Cadence design tools and fabricated using Nortel's 1.2μm CMOS process (see figure 3.11). For this design, the frequency response is no longer limited by the DUT as the input signal is fed directly into the sampling switch. The IC was designed to test the sampling switch and output buffer in isolation. By applying a sinusoid signal directly into the sampling switch, the frequency response of the test circuitry can be examined. By applying a square wave into the sampling switch, the transient response can be measured.

The IC contained an OpAmp as the output buffer and a n-type CMOS pass gate as the analog switch. The OpAmp used for the output buffer was identical to the OpAmp used in section 3.2.1 and 3.2.2. The layout of the circuit can be found in Appendix 4.1.

To further reduce the loading on the DUT, a minimum geometry n-type CMOS pass gate was used as the analog switch. The layout of the minimum geometry n-type pass gate is shown in Appendix 4.2. As the analog switch is made of an n-type transistor,

When the switch control signal level is at the ground (V_{ss}) rail, the switch is opened.

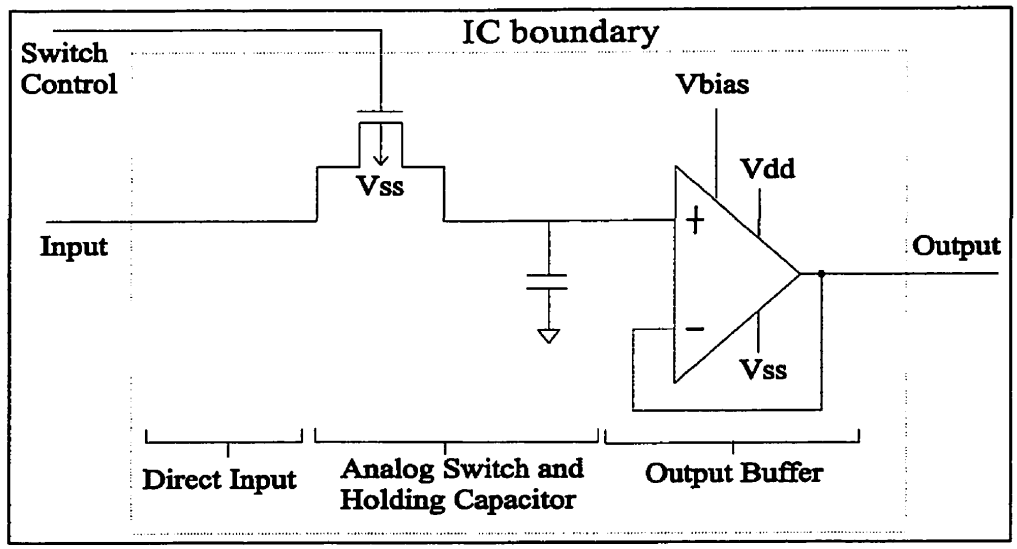

Figure 3.11 Open-Front End IC block diagram

The total silicon area of 100μm x 140μm is slightly less compared to the IC described in section 3.2.1 due to the reduced area of the sampling switch. The channel width and length of the n-type pass gate are listed in table 3.3 below:

Table 3.3: Dimensions of the source region of the CMOS n-type pass gate.

	W (μm)	L (μm)
N-type	4.6	5.0

The minimum dimension pass gate was used to minimize the loading on the node under test. By using equation 3-6; the parasitic capacitances were calculated as:

$$C_{d(n\text{-}type)} = [4.6 \times 5.0 \times (2.9 \times 10^{-4})]pF + [2 \times (4.6 + 5.0) \times (3.3 \times 10^{-4})]pF$$

$$= 0.013pF$$

transmission gate design (0.12pF) [53]. The number of I/O pins required is identical to the OpAmp DUT IC.

3.2.4 On-Chip Pulse Generator IC

One of the key advantages of using the undersampling approach is its relatively low cost in term of testing equipment. As shown in figure 3.1, there are only two inputs required to test the system response of the DUT; a repetitive test stimuli and a switch control signal. Test equipment cost can be further reduced if either one or both of these signals can be generated on-chip. This section covers on-chip narrow pulse generation while on-chip sinusoid generation is covered in chapter 5.

A prototype IC was designed using Cadence design tools and fabricated using Nortel's 1.2μm CMOS process which was provided through CMC. The schematic of the IC design is shown in figure 3.12 and the layout of the circuit can be found in Appendix 5. The objective of this IC was to investigate the performance of an on-chip RC network integrated with an inverter to generate narrow pulses on-chip. The IC design is identical to the Open-Front End IC except that the switch control pulses were generated on chip. Three additional components were added onto the Open-Front End IC: (1) 0.95pF capacitor, (2) 1KΩ polysilicon resistor, and (3) a protection diode.

Instead of using a narrow pulses generator, a fast rising and falling edge square wave is needed to generate the narrow pulses on chip. Test equipment cost can be reduced as fast rising and falling edge square wave generators are relatively cheap compared to narrow pulses generator. At each rising and falling edge, the voltage level

network. The DC level of the RC network is fed in through V_{bias}. The positive spikes are shunted to the V_{dd} rail for circuitry protection while the negative spikes will drive the gate of an inverter to generate positive pulses.

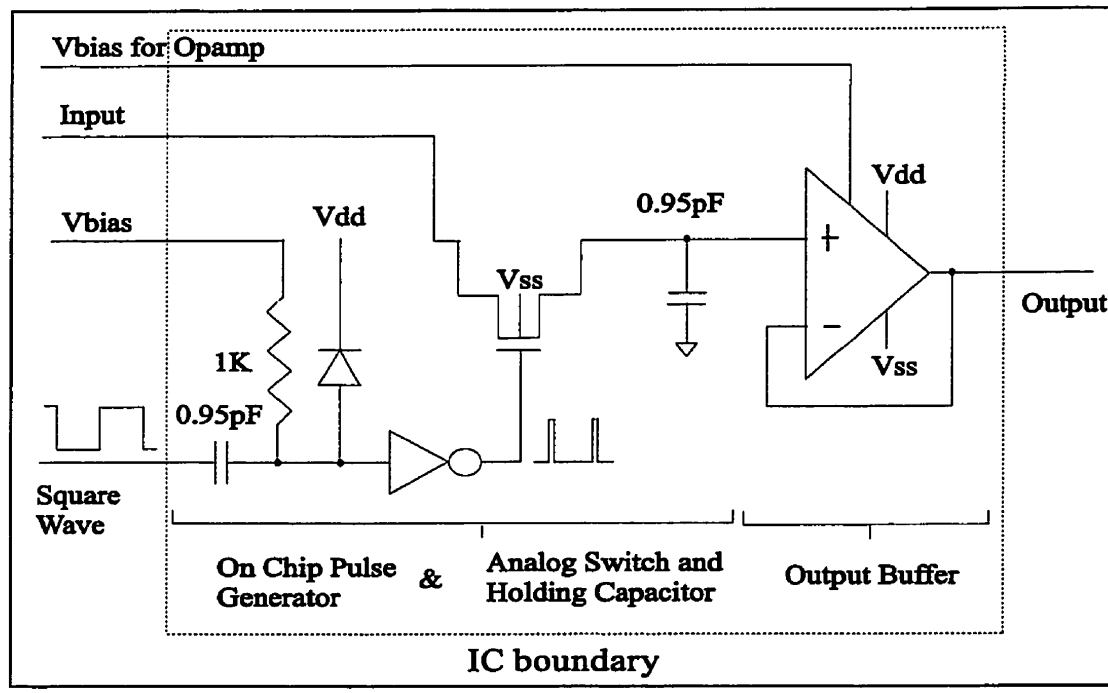

Figure 3.12 On-Chip Pulse Generator IC block diagram

The width of the positive pulses at the output of the inverter depends on the width of the negative spikes at the RC network. The width of the negative spikes depends on the V_{bias} level and the rise and fall time of the square wave input. The narrow positive pulses generated at the output of the inverter were used to turn on the analog switch. Test results collected from this prototype IC can then be compared with the results collected using the Open-Front End IC.

(resistor, capacitor, diode and inverter) is required. The total silicon area of the test circuitry design is 80μm x 250μm. A total of four I/O pins were required as follows:

- Repetitive input stimuli
- Square wave
- RC network biasing voltage
- Output pin

3.2.5 Multi-Node Analog DFT IC

For implementation of the undersampling approach in the production line, it would be more economic and pin count efficient if multiple nodes can be accessed with only a few additional pins. A DFT procedure has been developed for on-chip multi-node testing (see figure 3.13).

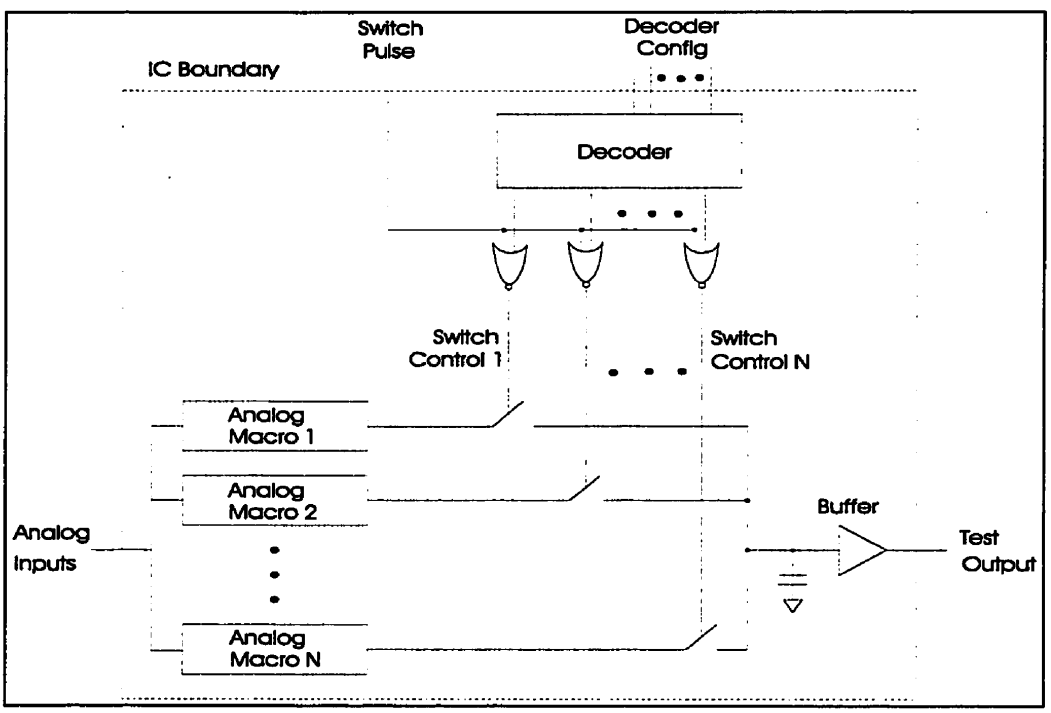

Figure 3.13 Analog DFT system block diagram

In its simplest form, four components are required on-chip to carry out the testing procedure:

- A digital decoder
- An analog switch for each internal node of an IC to be sampled
- A storage capacitor
- An OpAmp buffer

The Digital decoder is used to select which of the Analog Macros (1 through N) is to be accessed at a given instant of time. It can be configured through the decoder configuration inputs. When a particular switch is selected to be active, a narrow pulse, controlled by the switch control signal, will momentarily close an internal switch and sample the signal at that node.

By using minimum geometry transistors and applying the trickle charge technique, loading on the node under test can be minimized. For each analog macro to be accessed, an analog switch is required. By applying repetitive analog input signals of known frequency, the response of the analog systems will also be repetitive. The sampled signals are stored on the internal hold capacitor and buffered off-chip to the test output. Only one holding capacitor and one output buffer are required for an entire IC. The outputs of all the sampling switches can be bussed together to the hold capacitor and the output buffer.

An IC was designed to test the new DFT approach. The IC was designed using Cadence design tools and fabricated using Mitel's 1.5μm CMOS process. The IC contained four analog test circuits and sampling switches. The IC also contained a one of four decoder, a hold capacitor and an output buffer. Minimum geometry n-type pass

pass gate can be found in Appendix 6.1. The schematic of the one of four decoder circuits is shown in figure 3.14. It consists of four two-input NAND gates with their output connected to four two-input NOR gates. The NAND and NOR gates were used to generate narrow positive pulses to trigger charge through the analog switches (see figure 3.14).

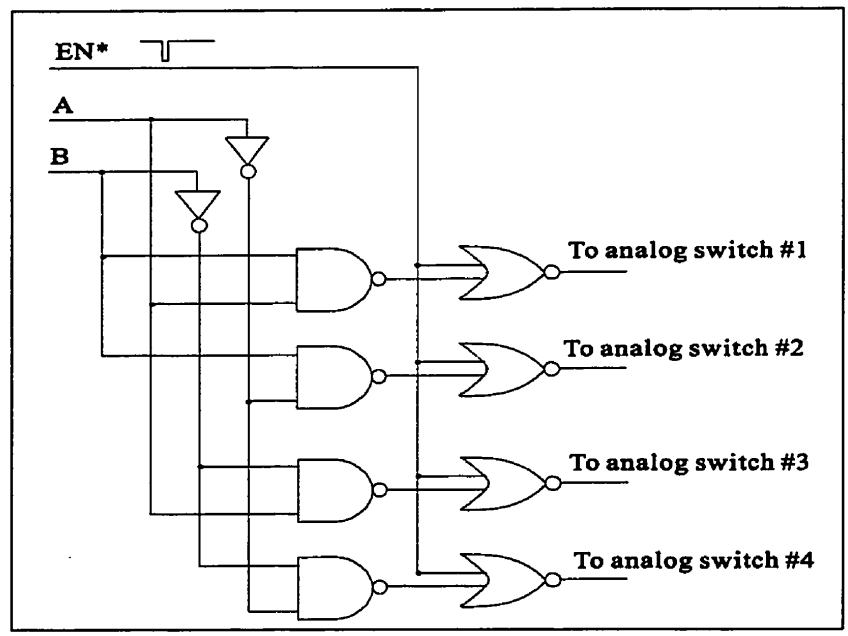

Figure 3.14 Schematic for one-of-four decoder

From figure 3.14, with any combinations of the A and B inputs, there is always a low signal at the output of the NAND gates while the other NAND gates' are high signals. When there are narrow negative pulses at the EN* port, the combination of the decoder configuration inputs and the EN* input will generate narrow positive pulses to trigger the analog switches.

macros consist of, see figure 3.15:

1. A unity gain OpAmp as DUT
2. An inverter as DUT

The characteristics and response of the macros could be determined by applying the undersampling DFT technique. The layout and schematic of the analog OpAmp can be found in Appendix 6.2.

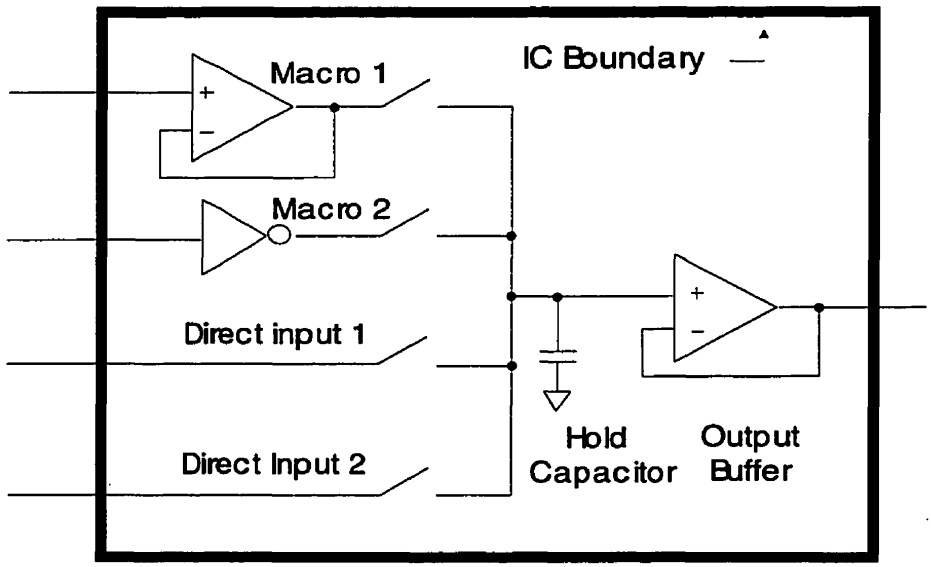

Figure 3.15 Symbolic schematic for the prototype IC

The total silicon area occupied by the test circuitry is approximately 300μm x 340μm. The layout of the circuit can be found in Appendix 6.3. Note that the chip area occupied by the test circuitry was not optimum. The test circuitry (output buffer, hold capacitor, four sampling analog switches, digital decoder) is 200 μm x 340μm. Each additional test node requires a sampling switch and a switch control line with an additional silicon area of 16.2μm x 13.1μm.

the input stimuli) is four. This includes an output port, two decoder configuration inputs and an enable input. For production implementation, the stimuli input signals are the actual nodes under test. For DFT automation, only 3 extra pins are required; an output pin, a serial input line for decoder configuration and an enable input. Each test node requires that only a switch (either a pass gate or a transmission gate) be attached at circuitry to be tested. The additional decoder circuitry required for each new test node can be generated using conventional digital synthesis techniques.

TESTING AND SIMULATION RESULTS

4.1 Test Signals and Equipment

To demonstrate the utility of undersampling DFT technique, the prototype ICs described in chapter 3 were tested for:

- Frequency response
- Slew rates
- 1 dB compression point
- Total harmonics distortion

A test station consisting of 4 main components was developed (see figure 4.1). The components are: (1) pulses train generator, (2) repetitive test signal source, (3) output signal analyzer, and (4) prototype IC test fixture and power supply.

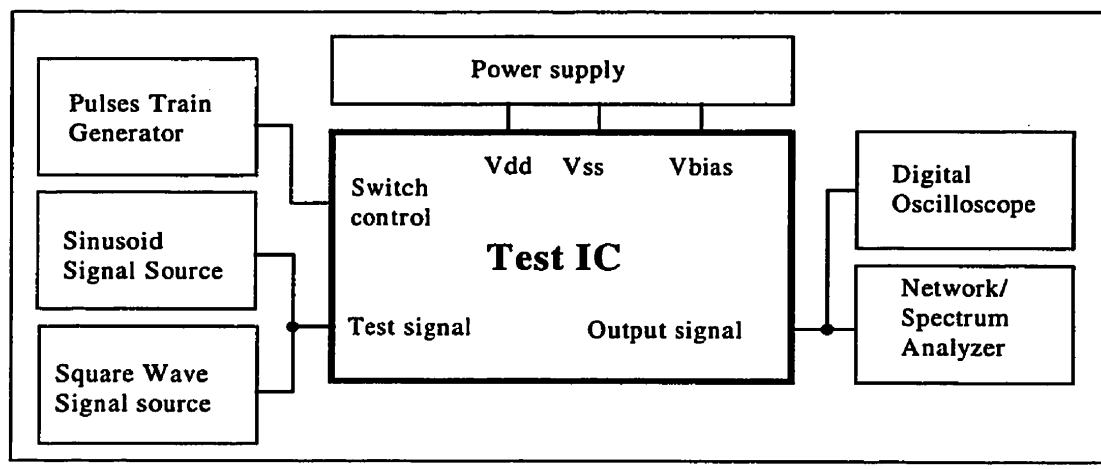

Figure 4.1 Prototype IC and equipment setup

Sinusoid signals were used to examine AC parameters of the DUT, while square waves were used to examine transient parameters. A digital oscilloscope was used to display and store the output signal in the time domain while a network/spectrum analyzer was used for frequency domain analysis. The test fixture is the package which contained the prototype IC to be examined. In most cases, a custom double sided Printed Circuit Board (PCB) was designed to hold the prototype ICs.

4.1.1 Switch Control Pulses Train

The pulses train signal source must be capable of generating clean narrow pulses to trigger analog switches. An HP 80000 data generator with a HP E2903A 1GHz data module was used to generate narrow pulses to test the prototype ICs. The HP E2903 data module is able to generate pulses with a minimum pulse width (τ) of 500ps and a rise and fall time of 150ps. For testing the prototype ICs, the E2903A data module was configured to generated a 1MHz pulse train.

4.1.2 Sinusoid Test Signal

A HP 8464A RF generator, which is capable of generating sinusoid waveforms from 100KHz to 1GHz, was used to generate sinusoid test signals. When sinusoid signals of higher frequency were required, the tracking generator of an Advantest RS3361 spectrum analyzer was used to generate sinusoid signals from 1GHz to 3GHz.

When test signal frequency increases, the amplitude of the sinusoid signal fed into the IC dice is attenuated due to parasitic components in the IC package. To measure this attenuation, the output of the HP 8464A RF generator was connected to the Advantest RS3361 spectrum analyzer. The amplitudes of the sinusoid generated by the RF

being fed into the IC die, a probe station with a low capacitance (0.04pF) probe tip (Picoprobe model 28), was used to measure the amplitude of the sinusoid signal at the wire bonding pad of the die. From figure 4.2, the signal measured was attenuated by 3dB at 950MHz using a 40-pin Dual In-line Package (DIP). The attenuation was largely due to the IC package and the connecting leads. The signal gain measured from 400MHz to 800MHz was largely due to resonance in the package parasitic components [4, 69]. A 10GHz test fixture (Daico DEFT9100) and bare IC die were also used for testing high frequency signals. The Daico test fixture eliminated any input signal attenuation or gain.

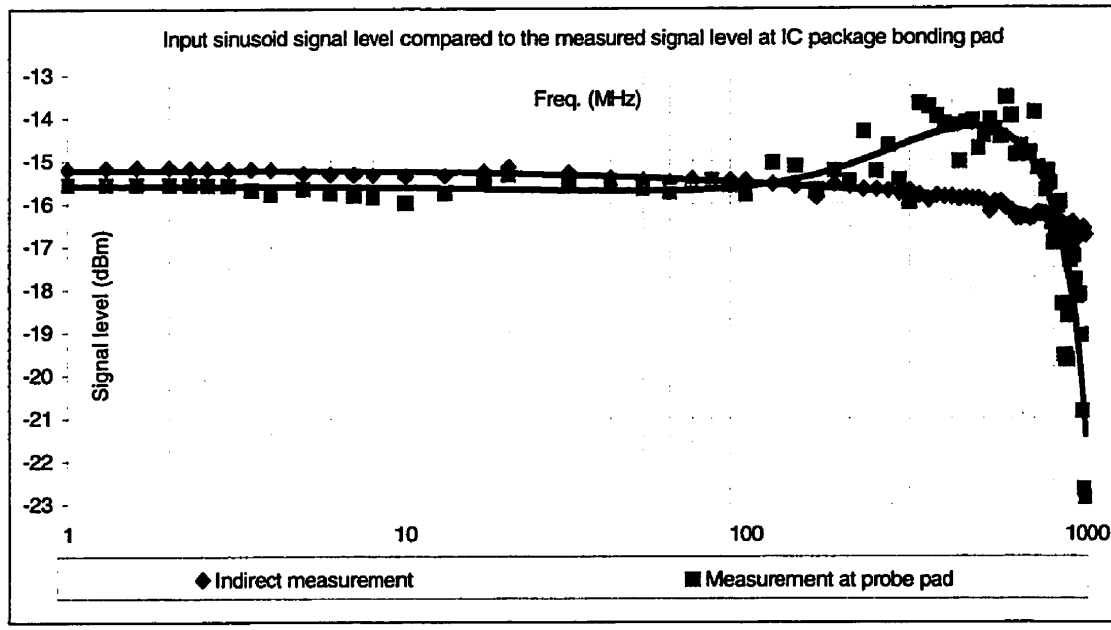

Figure 4.2 Direct sinusoid test signal compared with actual signal fed into IC die

The sinusoid signal generated by the HP 8464A RF generator was also measured in terms of its Total Harmonics Distortion (THD). THD is defined as the ratio of the fundamental signal power to the sum of the harmonic powers, and can be found by using

$$P(mW) = 1mW \times 10^{P(dBm)/10} \tag{4-1}$$

$$V_{RMS} = \sqrt{P(W) \times 50\Omega} \tag{4-2}$$

$$THD = \sqrt{\frac{V_{RMS_2}{}^2 + V_{RMS_3}{}^2 + \ldots + V_{RMS_n}{}^2}{V_{RMS_1}{}^2}} \tag{4-3}$$

where P is the power and V_{rms} is the root mean square voltage.

To measure the added THD of the signal tester, the THD of the signal generator was subtracted from the THD of the output. THD measurements of the sinusoid signal generated by the HP 8464A were taken at various frequencies and amplitudes using up to 7 harmonics (see Appendix 7.1).

4.1.3 Square Wave Test Signal

A Mini Circuits ZYSWA-2-50DR GaAs switch was used to generate square wave signals (see figure 4.3). The schematic of the GaAs switch is attached in Appendix 8. The GaAs switch requires a TTL level signal to trigger the two switches in the GaAs IC.

An HP 3325A function generator was used to generate the TTL triggering signal. The frequency of the output square wave is equivalent to the TTL triggering signal. From the schematic, the amplitude of the output square wave depends on the DC voltage at the RF input port. The RF input port was set to $2.0V_{dc}$ in order to generate a $1.2V_{p\text{-}p}$ square wave with fast rising and falling edges (see table 4.1).

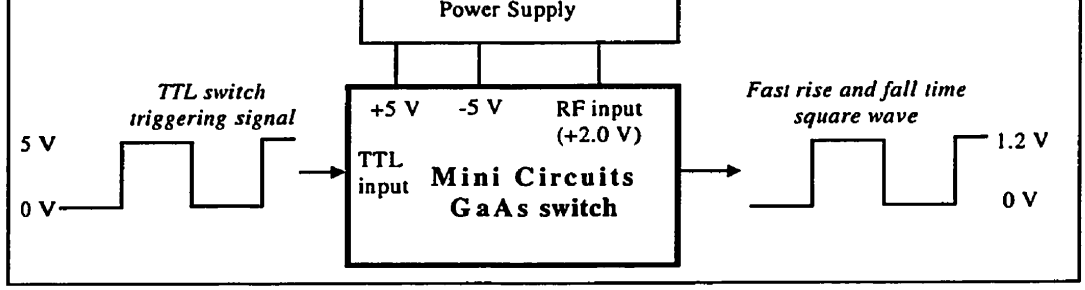

Figure 4.3 Square wave generation using a GaAs switch

Table 4.1. Slew rates of a 50% duty cycle square wave test signal

Rising edge V/μs:	Falling edge V/μs:
833.3	-1000.0

4.2 Prototype IC testing and simulation results

4.2.1 OpAmp DUT IC

The purpose of the OpAmp DUT IC was to demonstrate the utility of the undersampling technique to access on-chip internal nodes. The DUT to be examined was a two stage OpAmp for which AC and transient parameters were to be examined (see figure 4.4).

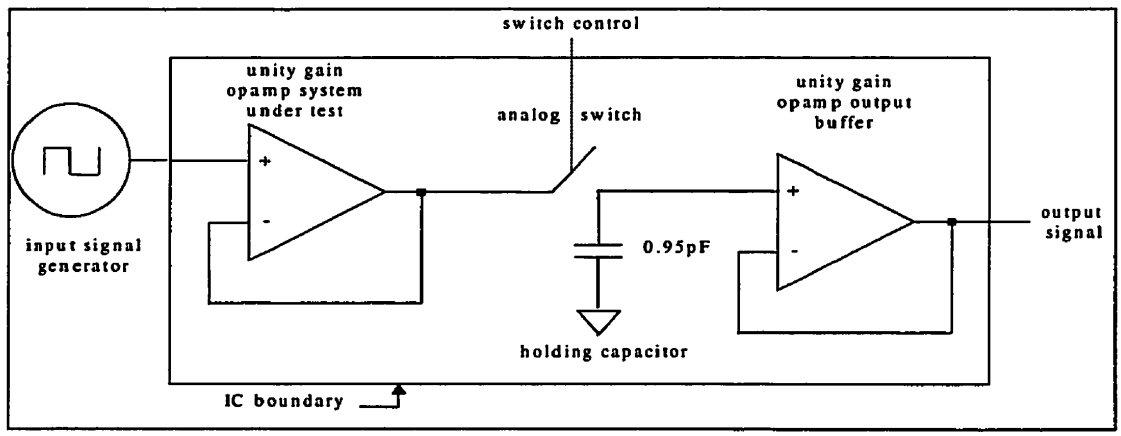

Figure 4.4 Schematic for the OpAmp DUT IC

sinusoid stimuli and a periodic series of narrow pulses to the prototype IC. The response of the OpAmp was measured with the HP 4195A network analyzer and HP 41800A active probe. The HP E2903A data module was set to generate a narrow pulse train with a pulse width of 2ns at a sampling frequency of 1MHz. The RF generator was set to output a −15.5dBm sinusoid signal. To implement the sequential undersampling technique, the sinusoid signal was set to provide a small offset in frequency with respect to the sampling frequency or its harmonic. For example, to provide a Δf of 1KHz; the RF generator was set to generate a sinusoid of 9.991MHz. This signal was mixed with the 10th harmonics of f_c. A series of data points was taken by varying the sinusoid signal frequency. The frequency response of the OpAmp is shown in figure 4.5. From the figure, the measured 3dB bandwidth was 180MHz.

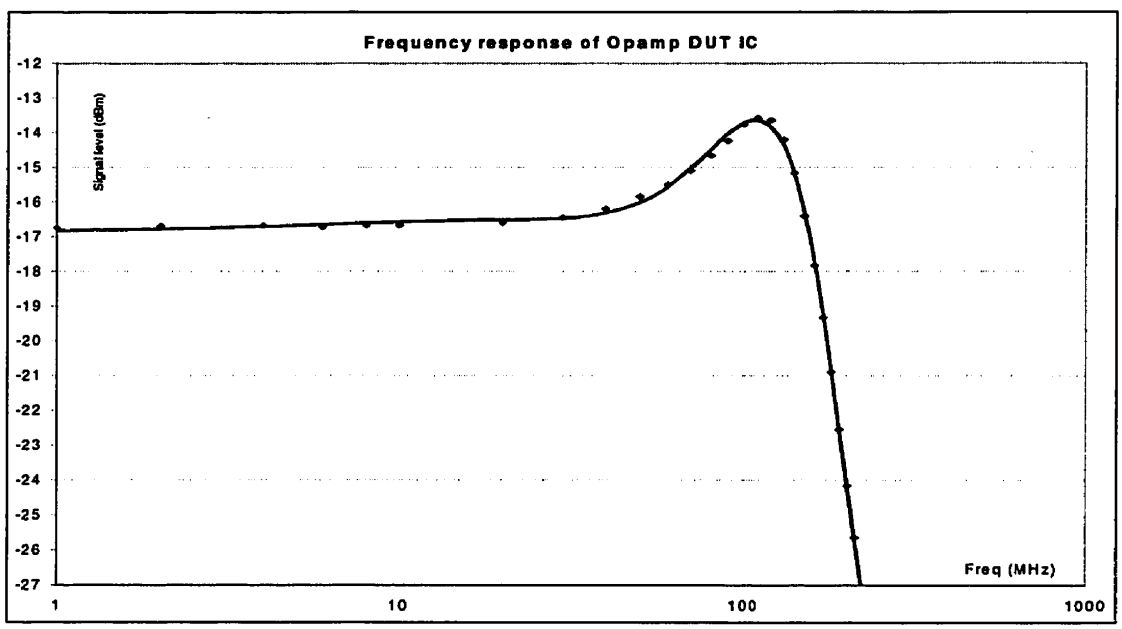

Figure 4.5 Frequency response of the OpAmp DUT

The slew rates of the OpAmp DUT was investigated by using the GaAs switch as the repetitive test signal. The switch control signal remained unchanged at an f_c of 1MHz and pulse width of 2ns and a square wave input frequency of 1.000150MHz resulted in an output square wave of 150Hz. The measured slew rates are 133.3V/μs and –116.0V/μs.

The linearity of the OpAmp was determined by measuring its 1dB compression point. The 1dB compression point is defined as the output power for amplifiers at which the gain is 1dB less than the low-power value (see figure 4.6a) [104]. Since the DUT was a unity gain OpAmp, the output power should equal to the input signal power. As shown in figure 4.6b, the 1dB compression point is noted as α.

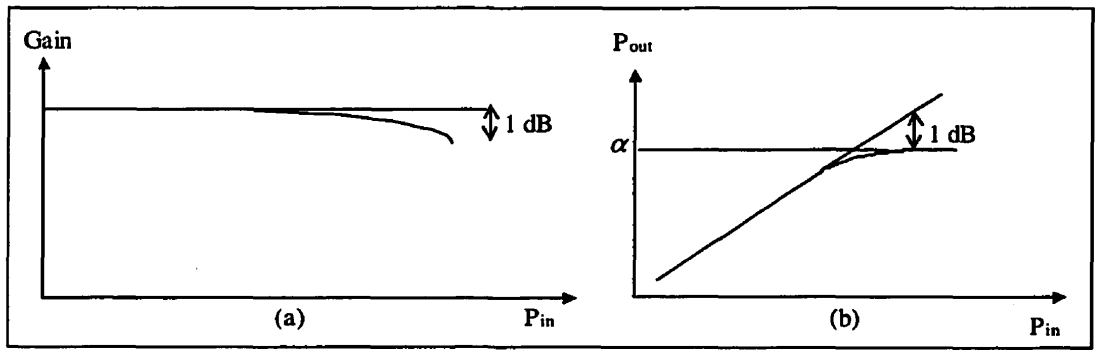

Figure 4.6 Gain Compression measurement using power sweep

To measure the 1dB compression point of the OpAmp, a 0.999MHz sinusoid signal was mixed with f_c. The amplitude of the sinusoid was initially set at -35.0dBm and the output was measured. Measurements were taken by gradually increasing the input signal level until the 1dB compression point was reached (see figure 4.7). From the plot, the 1dB compression point was determined to be -16.5dBm.

sinusoid while the pulses train remained unchanged. The spectra components of the test signal and the output signal (up to the 7th harmonic) are listed in Appendix 7.2. A THD of 0.119% was calculated for the input signal while a THD of 0.139% was calculated for the output signal. The added distortion to the OpAmp DUT was 0.020% or –74.0dB. Table 4.2 summarizes the test results obtained from the OpAmp DUT IC.

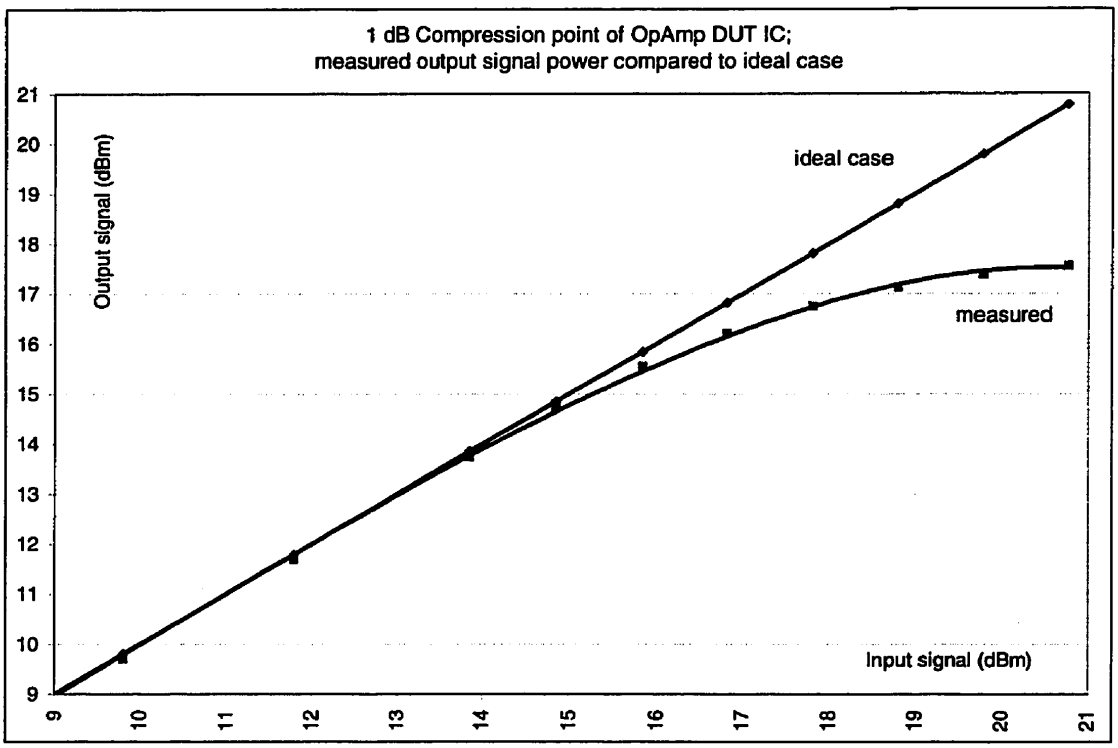

Figure 4.7 1 dB compression point of the OpAmp DUT IC

Table 4.2 Summary of test results obtained from the OpAmp DUT IC

Parameter:	Measured value:
3dB bandwidth	180MHz

Slew rates	133.3 V/μs; -116.0V/μs
1dB compression point	-16.5dBm
Added distortion to the output	-74.0dB

4.2.2 Probe-Pad IC

The Probe-Pad IC layout design was identical to the OpAmp DUT IC with the addition of a probe pad at the output of the OpAmp DUT. The main purpose of the IC was to demonstrate the utility of the undersampling testing approach for high speed testing and the effect of parasitic loading. Figure 3.10 shows the schematic of the prototype IC. Similar testing procedures conducted on the OpAmp DUT IC were conducted with this prototype IC.

The loading effect due to the probe pad can be illustrated by the frequency response degradation of the OpAmp DUT. Following the same testing procedure conducted on the OpAmp DUT IC with an input signal level of –17.0dBm, the frequency response measured at the output pin is shown in figure 4.8. From the plot, the 3dB bandwidth of the DUT was 120MHz with a pulse width of 2ns.

To measure the slew rates of the OpAmp, a 1.000150MHz square wave, generated by the GaAs switch, was used as the repetitive input signal. The switch control signal was set at an f_c of 1MHz with a pulse width of 2ns resulting in an output square wave of 150Hz. The measured slew rates are 133.3V/μs and –102.6V/μs.

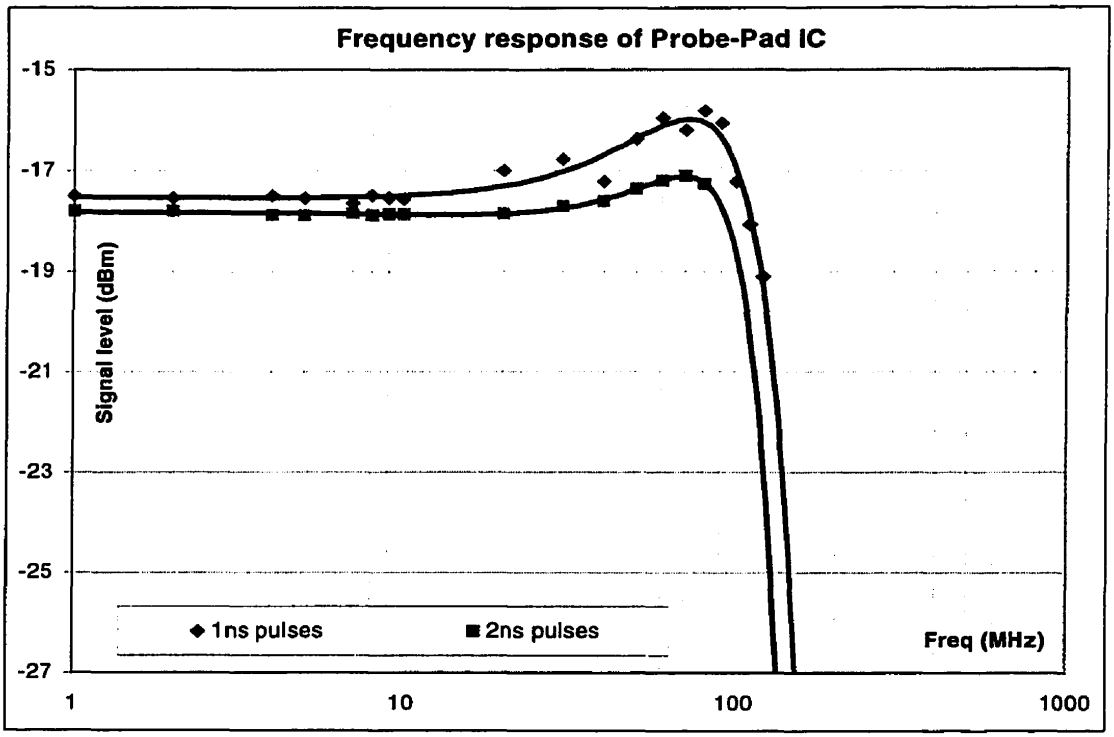

Figure 4.8 Frequency response of the Probe-Pad IC measured at the output pin

The frequency response of the DUT was also measured at the probe pad by using a low capacitance probe, Picoprobe model 28 (0.04pF loading factor). With an input signal level of –15.0dBm, the frequency response measured at the probe pad is shown in figure 4.9. From the plot, the 3dB bandwidth of the DUT was 120MHz with a pulse width of 1ns, which was the same as the measurements at the output pin (see figure 4.8).

To measure the slew rates of the OpAmp, a 1.000150MHz square wave, generated by the GaAs switch, was used as the repetitive input signal. The switch control signal was set at an f_c of 1MHz with a pulse width of 2ns resulting in an output square wave of 150Hz. The measured slew rates are 133.3V/μs and –102.6V/μs.

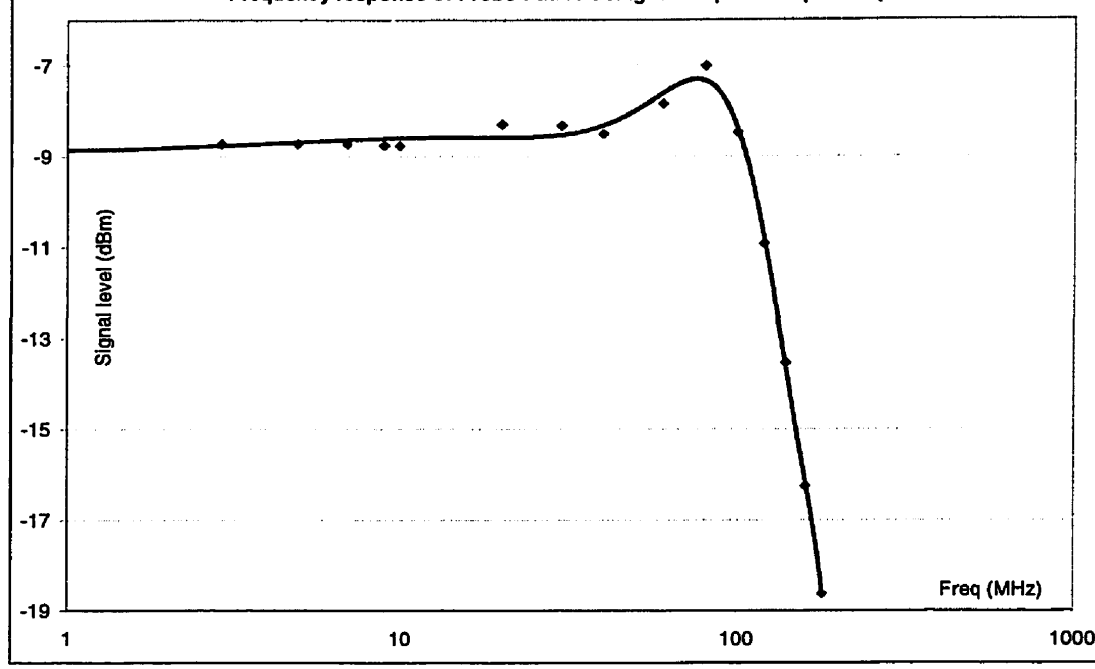

Figure 4.9 Frequency response of the Probe-Pad IC measured at the probe pad

Following the same procedures as in the previous section, the 1dB compression point was measured to be -16.5dBm (see figure 4.10). For THD measurements, the spectra components of the test signal and the output signal (up to the 7th harmonic) are listed in Appendix 7.3. Measurements were taken by using a 9.991 MHz sinusoid input at -11dBm. The THD of the input signal was 0.119% while the THD of the output signal measured with a pulse width of 2ns was 0.158%. The added distortion to the test signal was 0.039% or -68.2dB. Table 4.3 summarizes the test results obtained from the Probe-pad IC while table 4.4 shows the comparison of test results obtained from the OpAmp DUT IC and Probe-Pad IC.

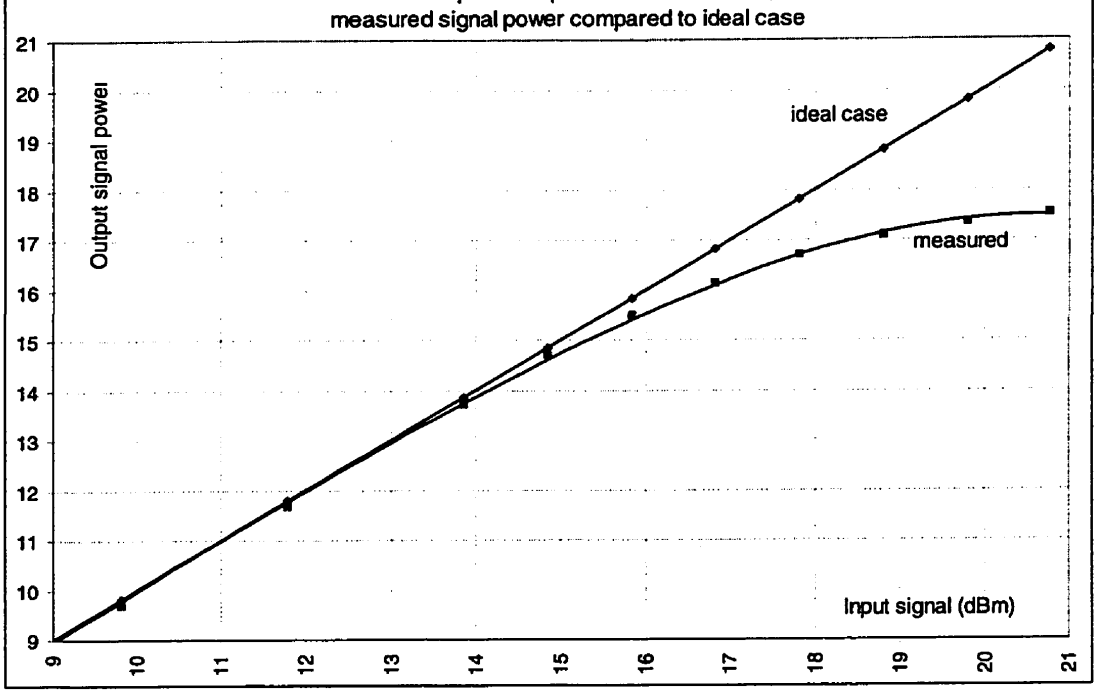

Figure 4.10 1 dB compression point of the Probe-Pad IC

Table 4.3 Test results obtained from the Probe-Pad IC

Parameter:	Measured value:
3dB bandwidth	120MHz
3dB bandwidth (measured at probing pad)	120MHz
Slew rates	133.3 V/μs; -102.6V/μs

Parameter:	Measured value:
1dB compression point	-16.5dBm
Added distortion to the output	-68.2dB

Table 4.4 Comparison of test results of the OpAmp DUT IC and Probe-Pad IC

Parameter:	OpAmp DUT IC	Probe-Pad IC
3dB bandwidth	180MHz	120MHz
Slew rates	133.3 V/μs; -116.0V/μs	133.3 V/μs; -102.6V/μs
1dB compression point	-16.5dBm	-16.5dBm
Added distortion to the output	-74.0dB	-68.2dB

Compared to 3dB bandwidth of the two ICs with and without the probe pad, the reduced DUT bandwidth was due to the parasitic capatitances of the probe pad. The reduced performance showed the superiority of the undersampling method for high speed testing. Compared to the slew rates measured with the OpAmp DUT IC (133.3V/μs, -116.0V/μs), the slew rates measured for the Probe-Pad IC had a slower falling edge. The reduction in slew rates measured was due to the parasitic capacitances of the probe pad. Theoretically, the rising edge slew rate should decrease but the signal measured showed

distortion of the output signal. The 1dB compression point for both ICs was −16.5dBm.

4.2.3 Open-Front End IC

For the OpAmp DUT IC and the Probe-Pad IC, the frequency response were limited by the DUT. The Open front End IC design is identical to the OpAmp DUT IC with two exceptions (see figure 4.11):

- The input signal is fed directly into the sampling switch
- A minimum dimension n-type pass gate was used as the analog switch, replacing the transmission gate and inverter

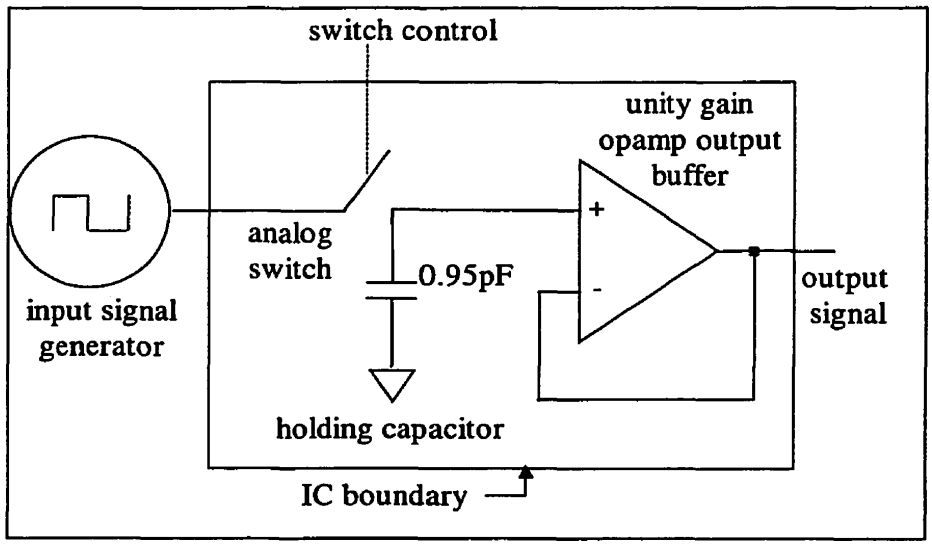

Figure 4.11 Schematic for the Open-Front End IC

With the input signal fed directly to the sampling switch, the performance of the sampling switch was examined. The minimum dimension pass gate was used to minimize the loading on the node under test.

with a pulse widths of 2ns, 1ns and 500ps (see figure 4.12). For input signal level of –15.0dBm, the 3dB bandwidth of the sampling switch was measured at 250MHz for τ of 2ns, 560MHz for τ of 1ns; and 950MHz for τ of 500ps.

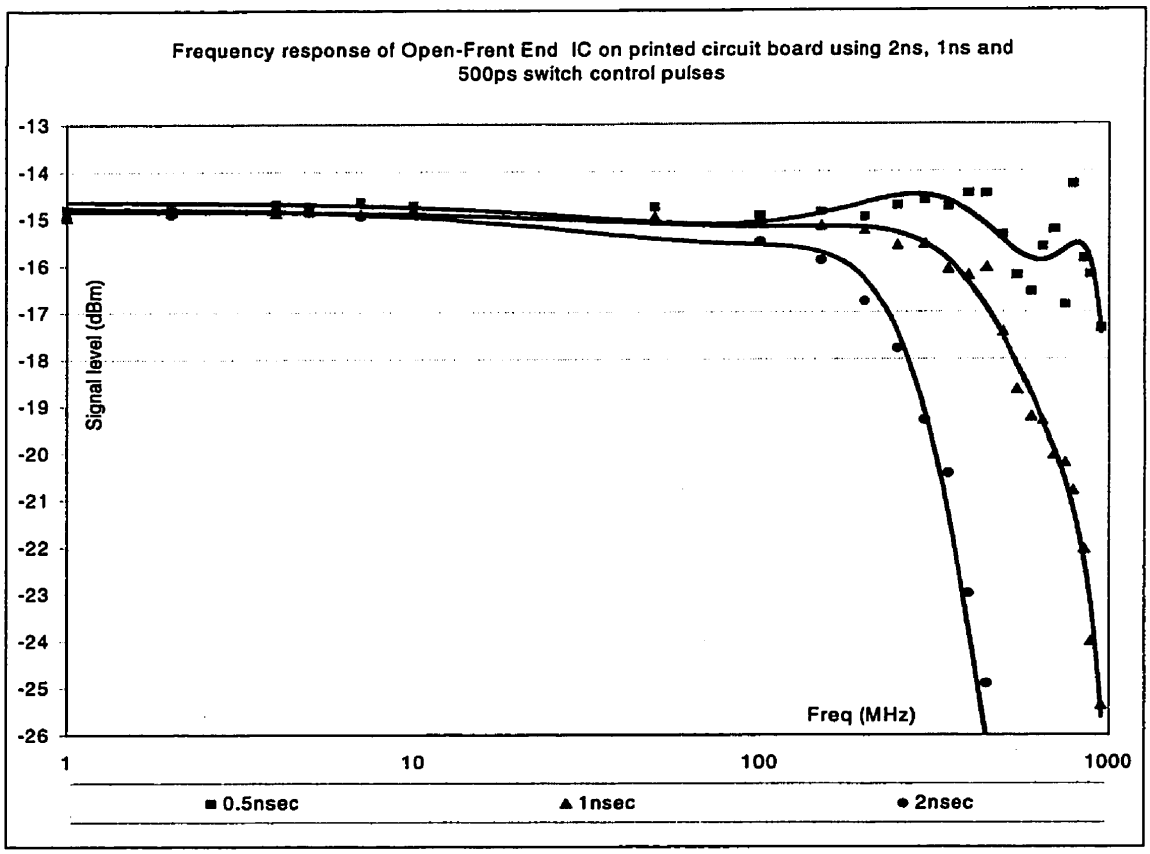

Figure 4.12 Frequency response of the Open-Front End IC on PCB

Recall that the test signal fed into the DIP IC was attenuated by 3dB at 950MHz. A low insertion loss test fixture was required to measure higher frequency signals. A bare silicon dice of the Open-Front End IC was bonded onto a micro S test package and a Daico DEFT9100 micro S device low insertion loss test fixture was used to examine the

examined with pulse widths of 1ns and 500ps is shown in figure 4.13.

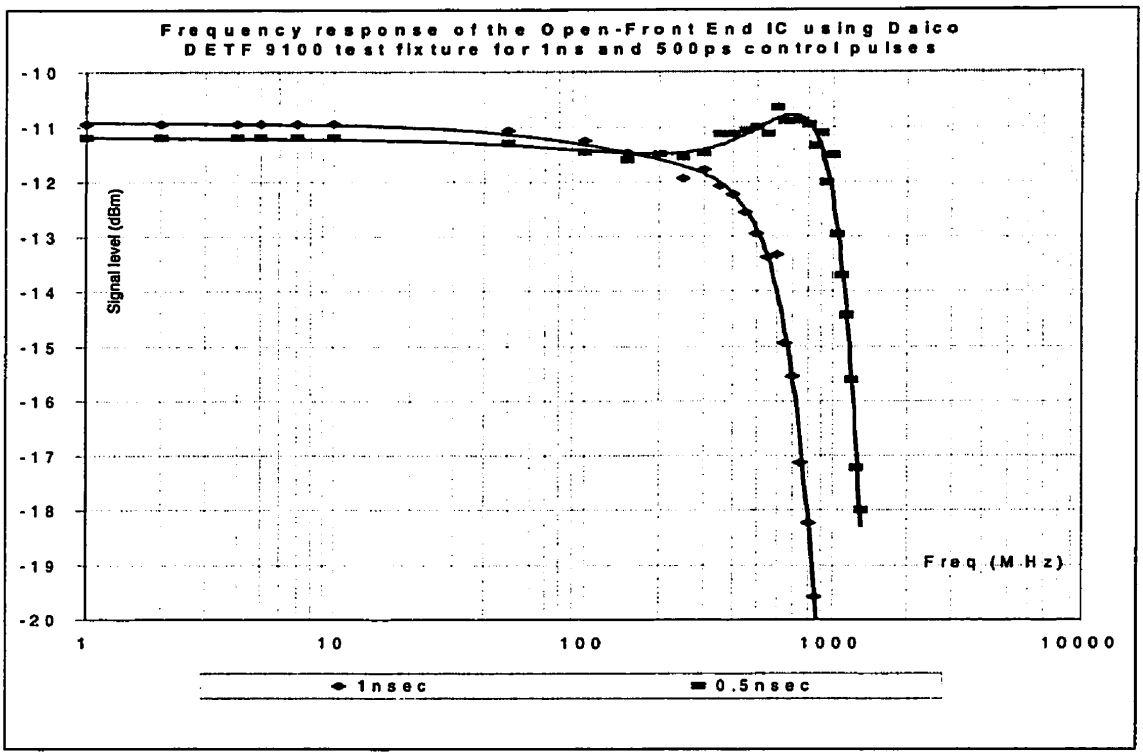

Figure 4.13 Frequency response of the Open-Front End IC in Daico test fixture

From figure 4.13, the frequency response of the sampling switch was found to be 620MHz for a pulse widths (τ) of 1ns and 1.1GHz for a τ of 500ps, compared to 560MHz and 950MHz measured for the prototype ICs using DIP packages. The sampling switch was able to measure signals up to 1.1GHz with a low insertion loss test fixture. By applying the trickle charge technique with narrow sampling pulse widths of 0.5ns, loading on the node under test was kept to a minimum and higher 3dB bandwidth was measured.

To measure the slew rates of the sampling switch, a 1.00015MHz square wave generated by the GaAs switch was used as the repetitive input signal. The switch control

slew rates are 296.3V/μs and –444.5V/μs for τ of 0.5ns; 484.9V/μs and –666.8V/μs for τ of 1ns; and 484.9V/μs and –533.4V/μs for τ of 2ns.

For THD measurements, the spectral components of the test signal and the output signal (up to the 7th harmonic) are listed in Appendix 7.4. Three measurements were taken by using -11.0dBm, 9.991MHz sinusoid and pulse widths of 2ns, 1ns, and 500ps. The THD of the output signal was measured as 0.072% (-62.7dB) for a pulse width of 2ns, 0.282% (-51.0dB) for pulse width of 1ns; and 1.141% (-38.9dB) for a pulse width of 500ps. The high harmonic distortion includes distortions from the DUT, sampling switch and output buffer. Charge coupling between the switch signal and the sampling switch output also degraded the sampling switch performance. Table 4.5 summarizes the test results obtained from the Open-Front End IC.

Table 4.5 Test results obtained from the Open-Front End IC

Parameter:	Measured value:
3dB bandwidth (in DIP package)	250MHz (τ of 2ns) 560MHz (τ of 1ns) 950MHz (τ of 0.5ns)
3dB bandwidth (in DAICO test fixture)	620MHz (τ of 1ns) 1.1GHz (τ of 0.5ns)

Parameter:	Measured value:
Slew rates	484.9V/μs; -533.4V/μs (τ of 2ns) 484.9V/μs; -666.8V/μs (τ of 1ns) 296.3V/μs; -444.5V/μs (τ of 0.5ns)
Added distortion to the output	-62.7 (τ of 2ns) -51.0 (τ of 1ns) -38.9 (τ of 0.5ns)

4.2.4 On-Chip Pulse Generator IC

Testing conducted in this section is to investigate the possibility of generating on-chip narrow pulses as control signals. With a fast rise and fall time square wave as the input to the pulse generator, the output of the Pulse Generator RC network was used to drive an inverter, see figure 4.14.

A simulation was conducted using HSPICE simulation software. Square waves with rise and fall time of 150ps were configured as input to the RC network and the RC network was biased at $2.5V_{dc}$. Simulation showed that both positive and negative spikes were generated by the RC network. At a threshold voltage of $2.3V_{dc}$, the pulse width of the negative spikes was determined to be 3ns. These negative spikes were used to drive the input gate of an inverter. At a threshold voltage of $2.5V_{dc}$, positive pulses with a pulse width of 3ns were used to drive the analog switches.

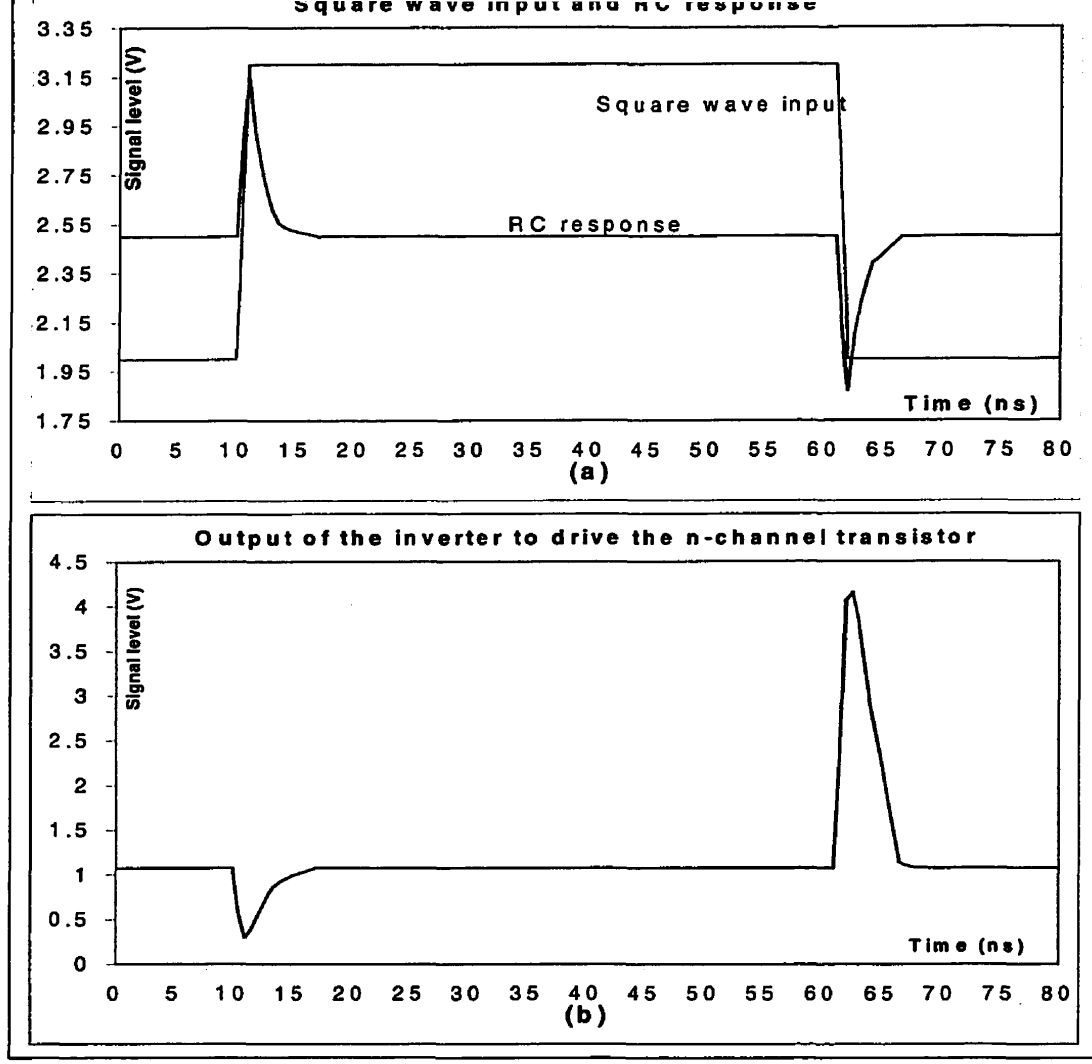

Figure 4.14 Simulation of pulses generated by the RC network on the On-Chip Pulse Generator IC

Using a square wave of 1MHz as the input of the RC network, a pulses train of 1MHz was generated at the output of the inverter. Recall that the main objective of this IC was to generate narrow pulses on chip, with which the harmonics of the sampling signals could be used to sample high frequency input signals. Referring to figure 3.5 and figure 4.14, the pulses generated at the output of the inverter had slow rising and falling

at high frequencies. The amplitude attenuation made sampling signals at high frequencies not feasible as the output of the sampled signal would also be attenuated.

For prototype testing, the frequency response of the sampling switch with the RC network was examined by using –9dBm and –15dBm sinusoid test stimuli, RC network bias voltage of $0.7V_{dc}$, and 1MHz square waves input signal. Several measurements were taken and found that the On-Chip Pulse Generator provided best results when the RC network was biased at $0.7V_{dc}$. The 3dB bandwidth of the sampling switch were measured as 330MHz for –9dBm sinusoid input and 340MHz for –15dBm sinusoid input (see figure 4.15 and table 4.6). To measure the slew rates, a 0.999850MHz square wave generated by the GaAs switch was used as the repetitive input signal. The switch control signal was set at an f_c of 1MHz and the RC network was bias at $0.7V_{dc}$. The measured slew rates are listed in table 4.6. Table 4.7 shows the comparison of test results obtained from the Open-Front End IC and On-Chip Pulse Generator IC.

Table 4.6 Test results obtained from the On-Chip Pulse Generator IC

Parameter:	Measured value:
3dB bandwidth	330MHz (for –9.0dBm input) 340MHz (for –15.0dBm input)
Slew rates	444.4V/μs; -76.2V/μs

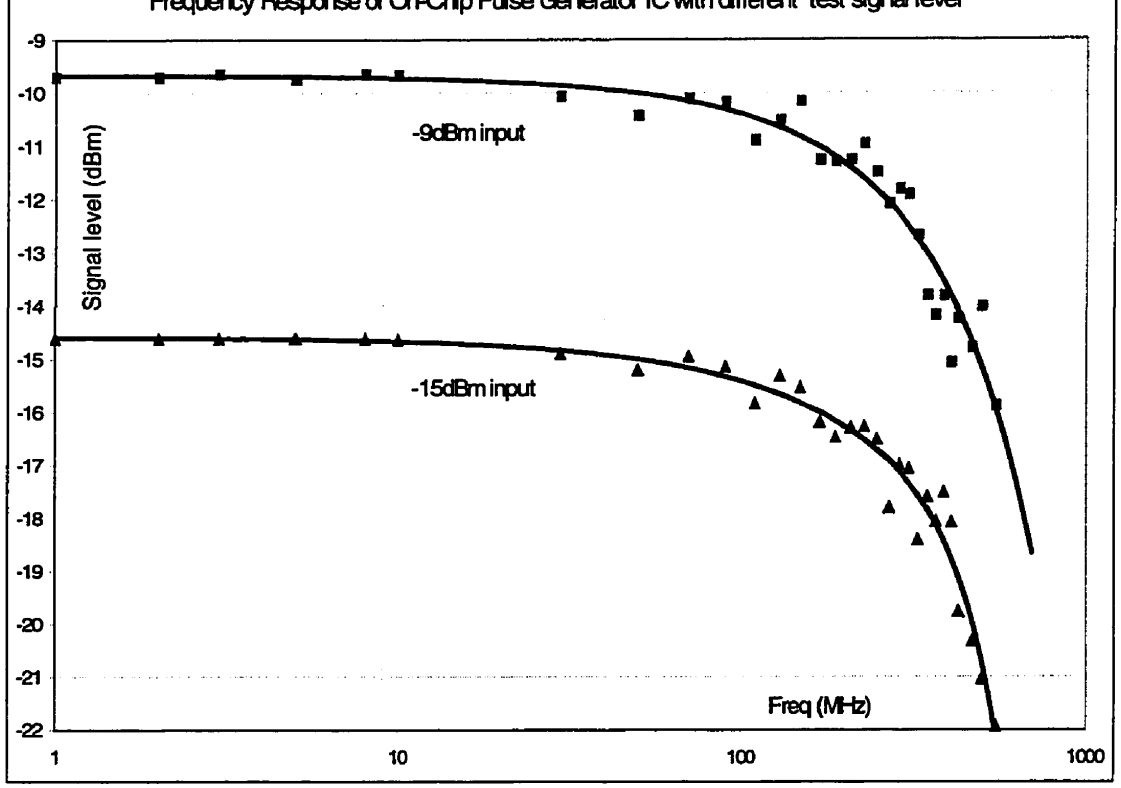

Figure 4.15 Frequency response of the On-Chip Pulse Generator IC with -9dBm and 15dBm input.

Table 4.7 Comparison of test results of the OpAmp DUT IC and Probe-Pad IC

Parameter:	Open-Front End IC	On-Chip Pulse Generator IC
3dB bandwidth	1.1GHz (in DAICO test fixture)	340MHz (–15.0dBm input)
Slew rates	484.9V/μs; -666.9V/μs (in DIP and τ of 1ns)	444.4V/μs; -76.2V/μs

compared to the Open-Front End IC was largely due to the low quality pulses generated on-chip. The measured slew rates were also significantly lower compared to the Open-Front End IC. The test results showed that the RC network and inverter was unable to generate high quality narrow pulses and was not suitable for high speed testing.

4.2.5 Multi-Node Analog DFT IC

Due to a power rail short in the prototype ICs, prototype testings was not possible. To verify the operation of the Multi-Node DFT IC, simulations were conducted by using Hspice simulation software to examine the frequency response of an analog macro. Recall from section 3.2.5 that there were two DUTs incorporated on the prototype IC; a unity gain OpAmp and an inverter. In addition to the two DUTs, there were two direct input lines connected to the IC input ports. The frequency response of the OpAmp was examined and compared to simulation results.

For simulations, the two direct input ports were set to signal ground (V_{ss}) potential and the input of the inverter DUT was set to V_{dd} power rail potential. A –20dBm sinusoid stimuli at various frequencies was applied to the input of the unity gain OpAmp. The frequency response of the OpAmp DUT is shown in figure 4.16. The 3dB bandwidth of the OpAmp DUT was found to be 71MHz (see table 4.8).

To examine the OpAmp DUT embedded as one of the analog macros, the test mode of the one-of-four decoder was configured to control the analog switch which was connected to the OpAmp DUT. A –15dBm sinusoid stimuli at various frequencies was applied to the input of the unity gain OpAmp, and a 1MHz narrow negative pulses with a

undersampling algorithm to the simulations, the resulting frequency response of the OpAmp DUT is shown in figure 4.17. From figure 4.17, the 3dB bandwidth of the OpAmp DUT was found to be 55MHz (see table 4.8). The reduced 3dB bandwidth is believed to be due to the increased input level. Further simulations were not possible as the license for the Hspice simulation software was expired.

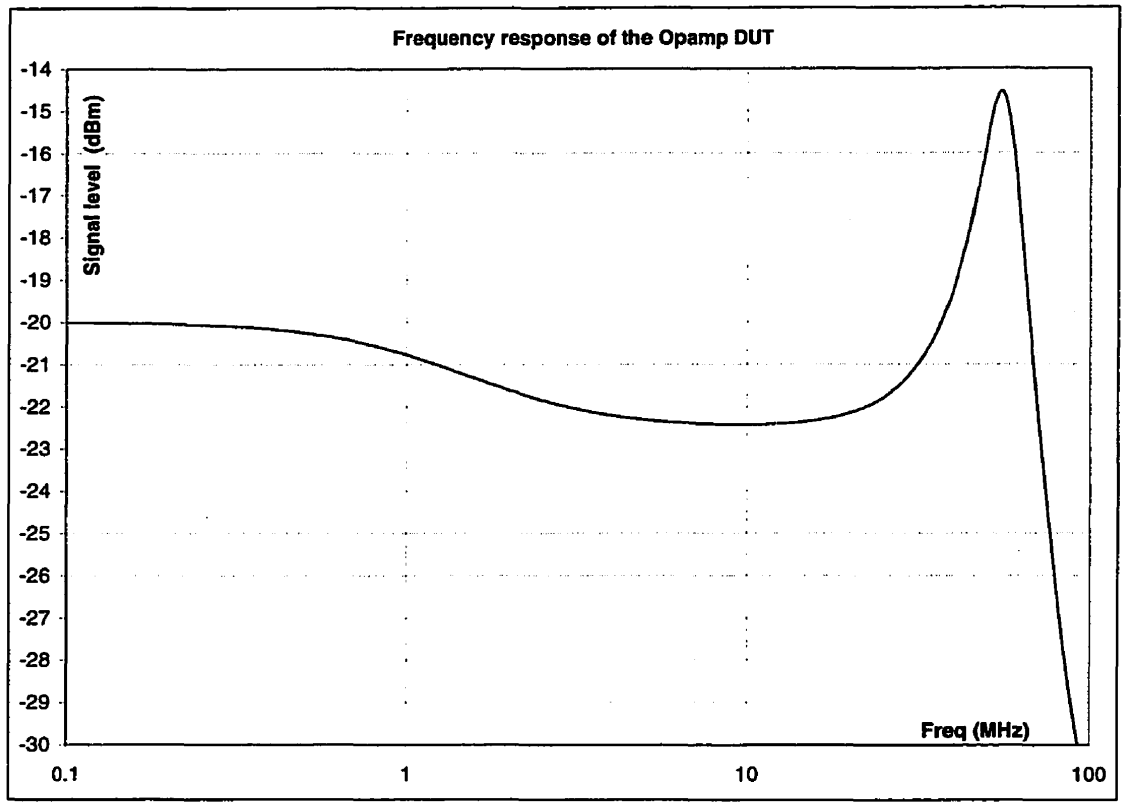

Figure 4.16 Simulated frequency response of the OpAmp DUT with –20dBm input.

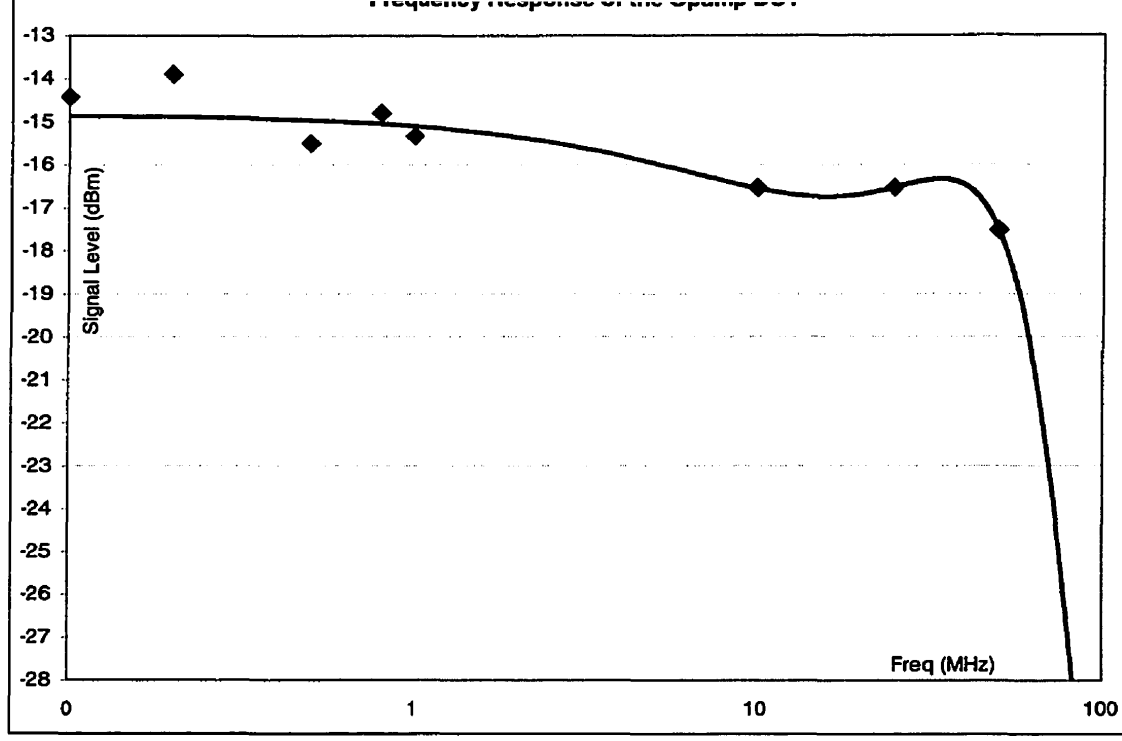

Figure 4.17 Simulated frequency response of the OpAmp DUT on the Multi-Node DFT IC with –15dBm input.

Table 4.8 Simulated frequency response of an OpAmp DUT and its Frequency response on the Multi-Node Analog DFT IC

DUT:	**Sinusoid input level (dBm):**	**-3dB BW (MHz):**
OpAmp DUT	-20	71.0
Trickle-charged OpAmp DUT	-15	55.0

Table 4.9 through 4.11 show the summary on prototype IC testing and simulation results.

Table 4.9 Test results for OpAmp DUT IC and Probe-Pad IC

Prototype IC:	**Parameter:**	**Measure/simulated value:**
OpAmp DUT IC	3dB bandwidth	180.0MHz
	Slew rates	133.3V/μs; -116.0V/μs
	1dB compression point	-16.5dBm
	Added distorion	-74.0dB
Probe-Pad IC	3dB bandwidth	110MHz (τ=2ns, measured at DIP pin)
		120MHz (τ=1ns, measured at DIP pin)
		120MHz (measured at probe pad)
	Slew rates	133.3V/μs; -102.6V/μs
	1dB compression	-16.5dBm
	Added distorion	-68.2dB

Prototype IC:	Parameter:	Measure/simulated value:
Open-Front End IC	3dB bandwidth:	250MHz (τ=2ns, in DIP package)
		560MHz (τ=1ns, in DIP package)
		950MHz (τ=0.5ns, in DIP package)
		620MHz (τ=1ns, in DAICO test fixture)
		1.1GHz (τ=0.5ns, in DAICO test fixture)
	Slew rates:	484.9V/μs; -533.4V/μs (for τ of 2ns)
		484.9V/μs; -666.8V/μs (for τ of 1ns)
		296.3V/μs; -444.5V/μs (for τ of 0.5ns)
	Added distortion:	-62.7dB (for τ of 2ns)
		-51.0dB (for τ of 1ns)
		-38.9dB (for τ of 0.5ns)
On-Chip Pulse Generator IC	3dB bandwidth:	330MHz (for input signal of –9dBm)
		330MHz (for input signal of –15dBm)
	Slew rates:	444.4V/μs; -76.2V/μs

Table 4.11 Simulation results for the Multi-Node Analog DFT IC

DUT:	Sinusoid input level (dBm):	-3dB BW (MHz):
OpAmp DUT	-20	71.0
Trickle-charged OpAmp DUT	-15	55.0

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

This thesis can be viewed in two different perspectives; (1) to achieve high quality and high speed mixed-signal testing, and (2) to develop a DFT technique with relatively low cost equipment. The feasibility of trickle charge undersampling for high speed analog signals was shown in Simon et. al's HAST. The work included in this thesis is a continuation of Simon et.al's work.

The most common mixed-signal DFT schemes have been examined. The limitations of these schemes show the need for HAST like systems for multi-node high speed mixed-signal testing. The HAST technique has been explained in both the time domain and frequency domain. It was shown that using high quality sampling pulses, on-chip high frequency signals could be measured. The method requires a repetitive input stimuli which can be mixed with the sampling frequency or its harmonics [38, 53]. In order to apply the undersampling technique, the sampling frequency and its harmonics are required to have flat spectral power level in the frequency domain. In order to avoid the null points due to the $\sin x/x$ attenuation factor, the sampling signals must consist of fast rising and falling edge pulses with pulse widths of 2ns or less.

The results obtained from the OpAmp DUT IC and the Probe Pad IC were compared. The inclusion of the probe pad increased the parasitic loading on the node under test. The performance of the Probe Pad IC was found to be reduced compared to

compared to probing further demonstrated the utility of the technique.

An Open Front End IC was used to examined the response of the sampling switch in isolation. With no DUT attached to the sampling switch, the maximum performance of the sampling circuits were measured. It was shown that using a high frequency test fixture, on-chip signals above 1GHz could be measured.

An On-Chip Pulse Generator IC was design to investigate the possibility of generating narrow control pulses on-chip. Due to the slow rising and falling edges of the pulses generated on-chip, these pulses reduced performance compared to high quality external signals. It did however demonstrated the feasibility of the approach. Using high quality pulses generated on-chip, testing costs can be reduced as a relatively low cost device can drive the on-chip pulses generator.

For production testing, it is more economical to apply DFT techniques to access many internal nodes. Simulations were conducted on a Multi-Node Analog DFT IC to demonstrate the feasibility of the approach. A prototype IC was designed in which only four additional I/O pins were required to test an unlimited number of internal nodes. For each additional test nodes, only one additional sampling switch is required. For actual production line implementation, only three additional pins are needed.

5.2 Future Work

Test costs can be further reduced if the sampling pulses or test stimuli can be generated on-chip. For testing high speed on-chip signals, on-chip circuitry must be able to generate high quality signals. One approach which could be investigated for

lines.

The undersampling technique could also be potentially used to generate multi-tone input signals on-chip. With a stable external repetitive signal source and a clean pulses generator, the product of the mixing process will also be a repetitive signal. The frequency of this signal can be varied by either changing the sampling frequency or the signal source frequency.

Multi-tone signals are useful in analog ICs. Multi-tone signals are important for isolation, distortion and frequency response measurements. When multi-tone signals can be generated on-chip, measurements like the 3rd order intermodulation point can be measured more accurately. An approach for generating multi-tone signals using undersampling technique is shown in figure 5.1.

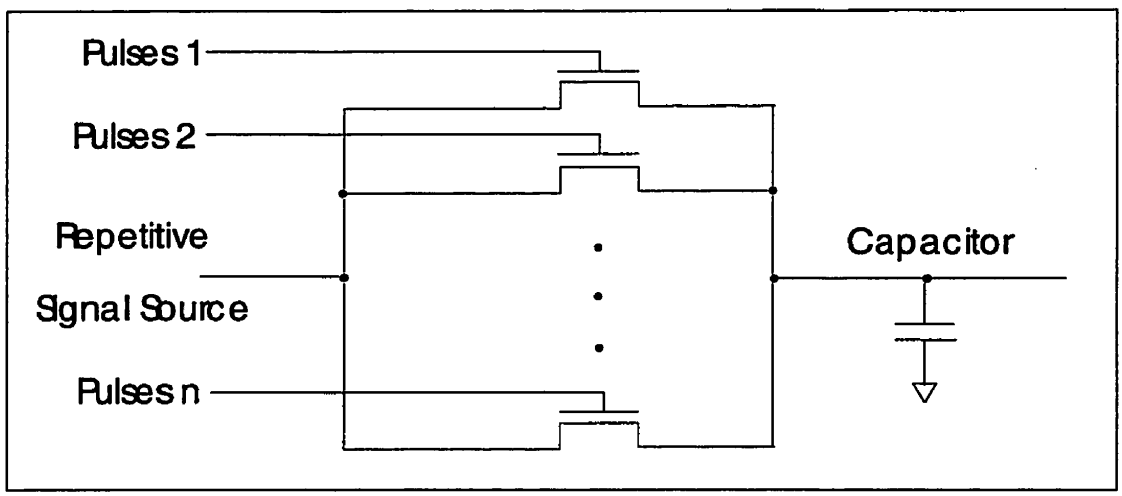

Figure 5.1 Schematic for multi-tone signal generation circuit

pulse sources and the repetitive signal source can either be internal or external sources. Only one hold capacitor is needed for an IC.

An IC was design and fabricated to test the isolation between the DFT circuitry and other non-connected circuits during normal operation. The IC was design using Nortel's 1.2μm CMOS technology. Two circuits were included in the design. The first circuit was an OpAmp which serves as an observation circuit to investigate the effect of additional test circuits near the area of the OpAmp. The performance of this OpAmp should be examined under normal operation with the test circuit in non-active mode and compared with the performance when the test circuit is operating.

Jitter is an important consideration on how accurate a test can be conducted, especially for high frequency measurements. Jitter can be classified into two categories: (1) residual jitter of the signal sources, and (2) jitter between test equipment/signal sources. To reduce these jitter effects, all test equipment and signal sources could be synchronized with a very high accuracy system clock/trigger. Technique could also be investigated for reducing any on-chip jitter.

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CMOS Transmission Gate and Inverter

A1.1 CMOS Transmission Gate and Inverter Layout Cellview

The transmission gate and inverter used in the prototype ICs extracted from a standard cell in CMC's Analog Cell Library. Layout design was extracted from Nortel's 1.2μm standard cell library (see figure A1.1). The transmission gate and inverter were used as an analog switch. The switch will close when there is a low control signal at the input port.

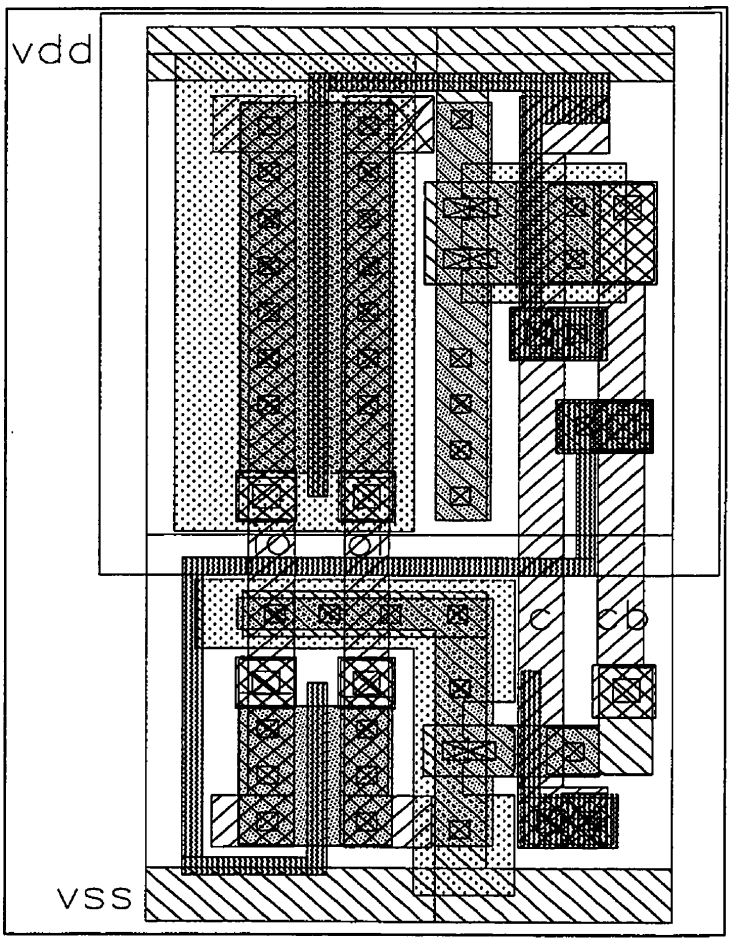


Figure A1.1 The layout cellview of a CMOS transmission gate and inverter

A1.2 CMOS Transmission Gate and Inverter Block Diagram

The schematic of the transmission gate and inverter is shown in figure A1.2.

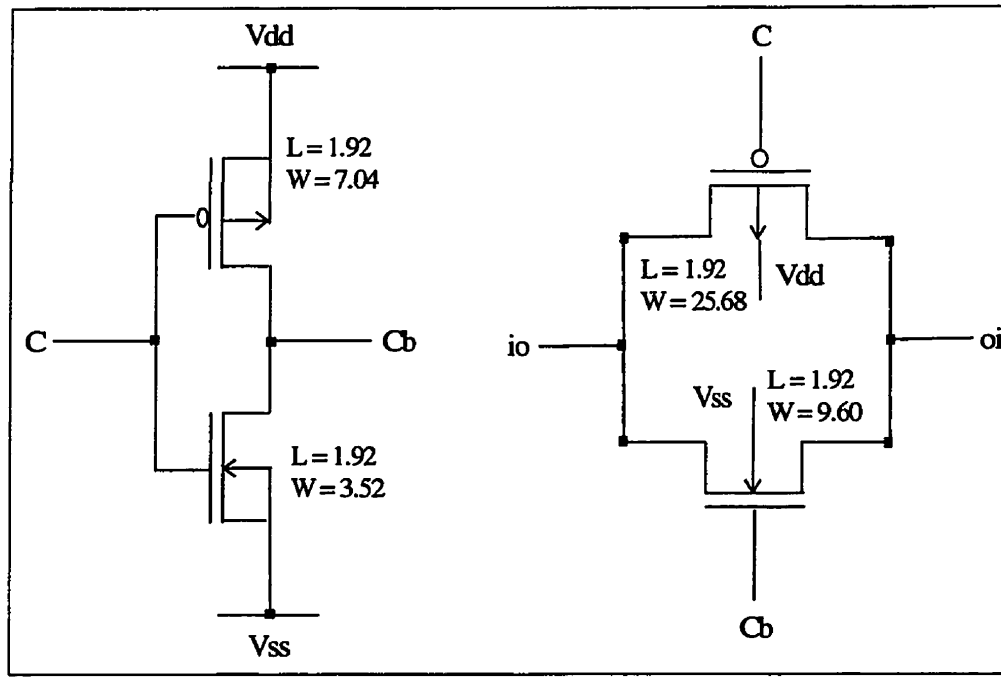


Figure A1.2 Schematic for a CMOS transmission gate and inverter

Layout Design of CMOS OpAmp and OpAmp DUT IC

A2.1 CMOS Analog OpAmp Layout Cellview

The unity gain OpAmp DUT and output buffer used in the OpAmp DUT IC was designed using a CMOS analog OpAmp extracted from Nortel's 1.2μm standard cell library. Figure A2.1 shows the layout cellview of the OpAmp.

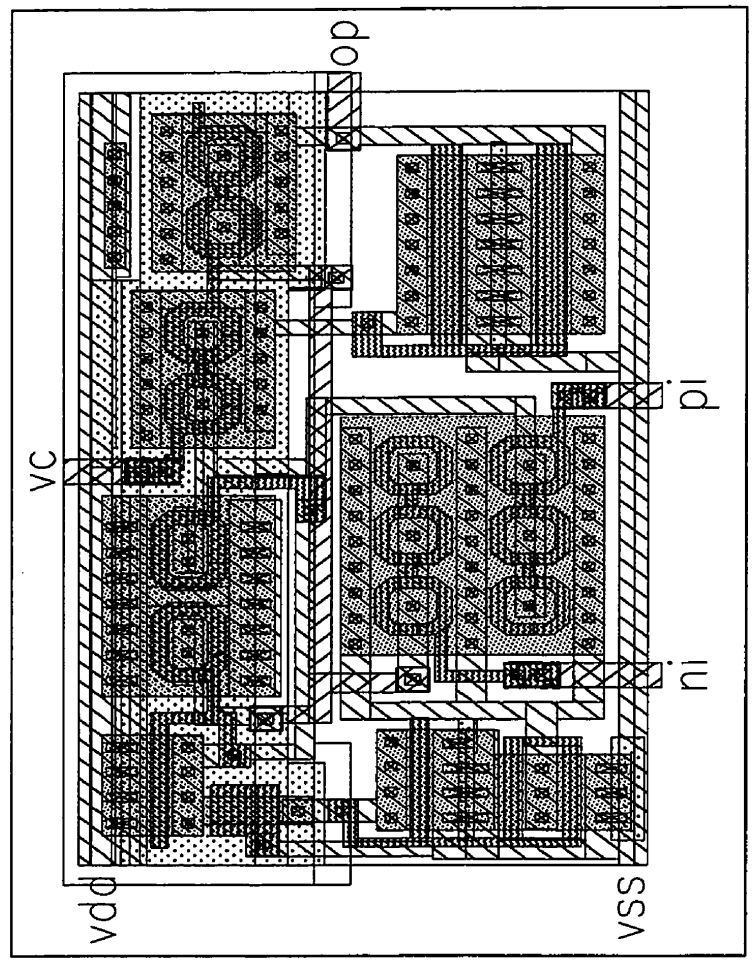


Figure A2.1 Layout cellview for the CMOS analog OpAmp

The unity gain OpAmp and output buffer was designed by connecting the negative input to the output terminal.

Figure A2.2 shows the schematic of a CMOS OpAmp.

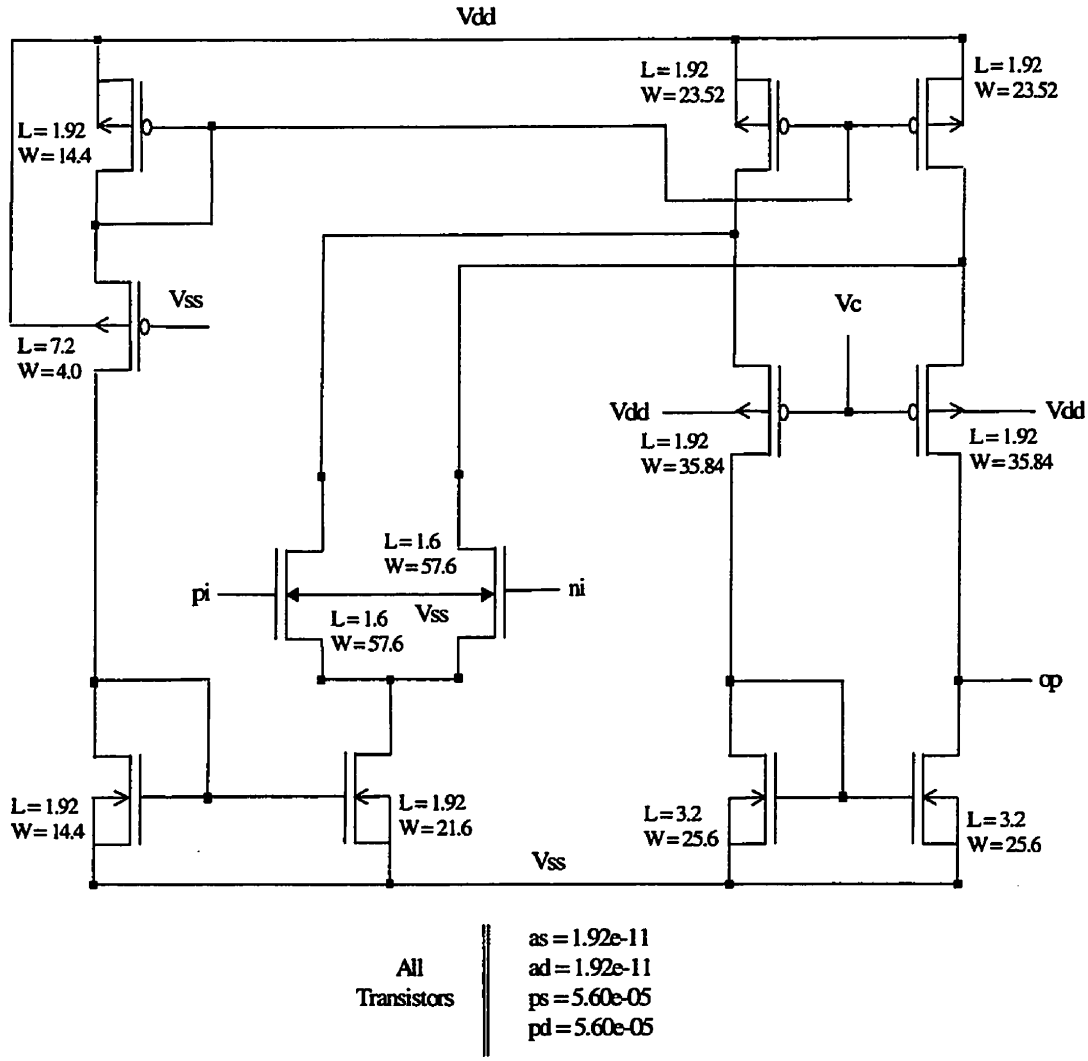


Figure A2.2 Schematic for the CMOS analog OpAmp

Figure 2.3 shows the layout design of the OpAmp DUT.

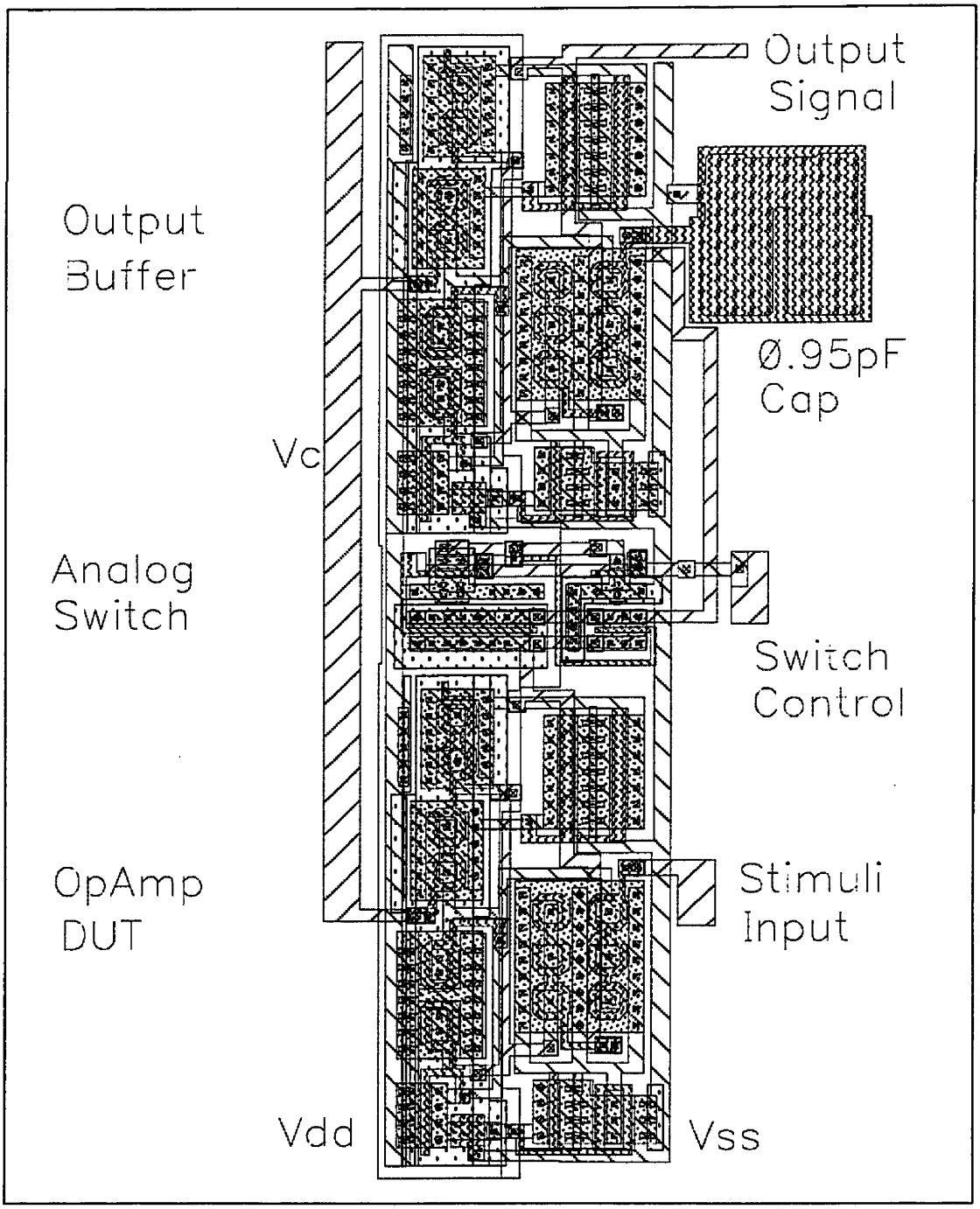


Figure A2.3 Layout of the OpAmp DUT design

Layout Design of the Probe-Pad IC

The layout design of the Probe-Pad IC is shown in figure A3.1. The layout includes the OpAmp DUT and a 40μm x 40μm probe pad.

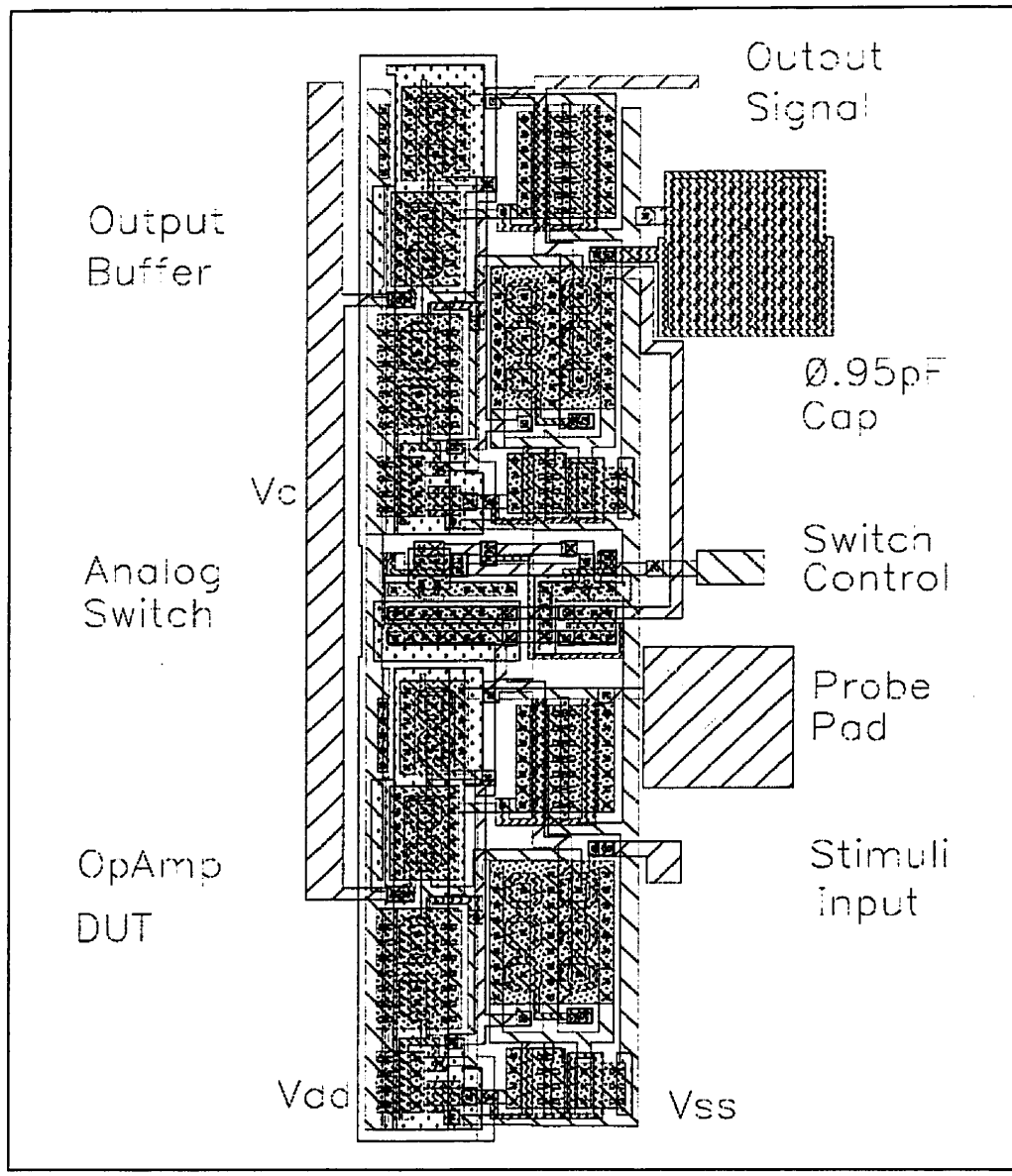


Figure A3.1 Layout of the Probe-Pad IC

A4.1 Layout of the Open-Front End IC

The layout design of the Open-Front End IC is shown in figure A4.1. Note that there was no DUT connected to the minimum dimension n-type transistor. The n-type transistor was a modification of the transmission gate and inverter used as the analog switch in the OpAmp DUT IC.

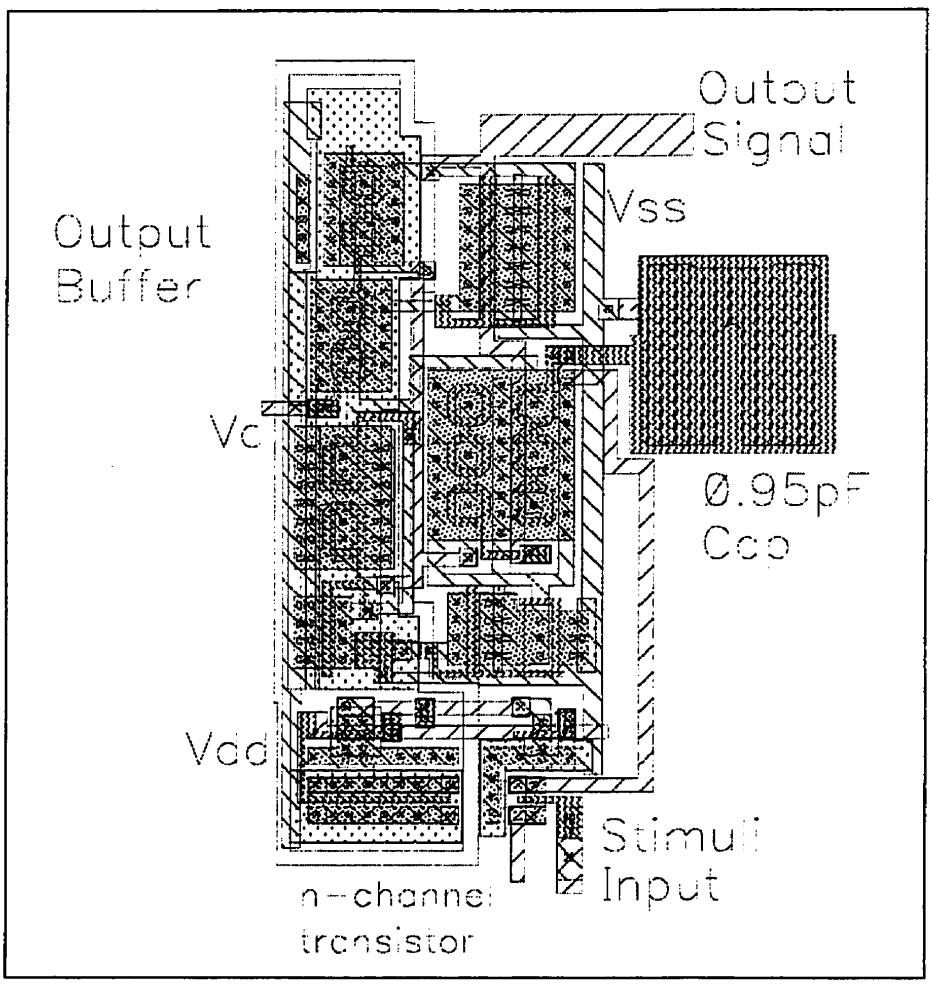


Figure A4.1 Layout of the Open-Front End IC

Figure A4.2 shows the minimum dimension n-type transistor used as the analog switch. The transistor was also used as the analog switch in the On-Chip Pulse Generator IC.

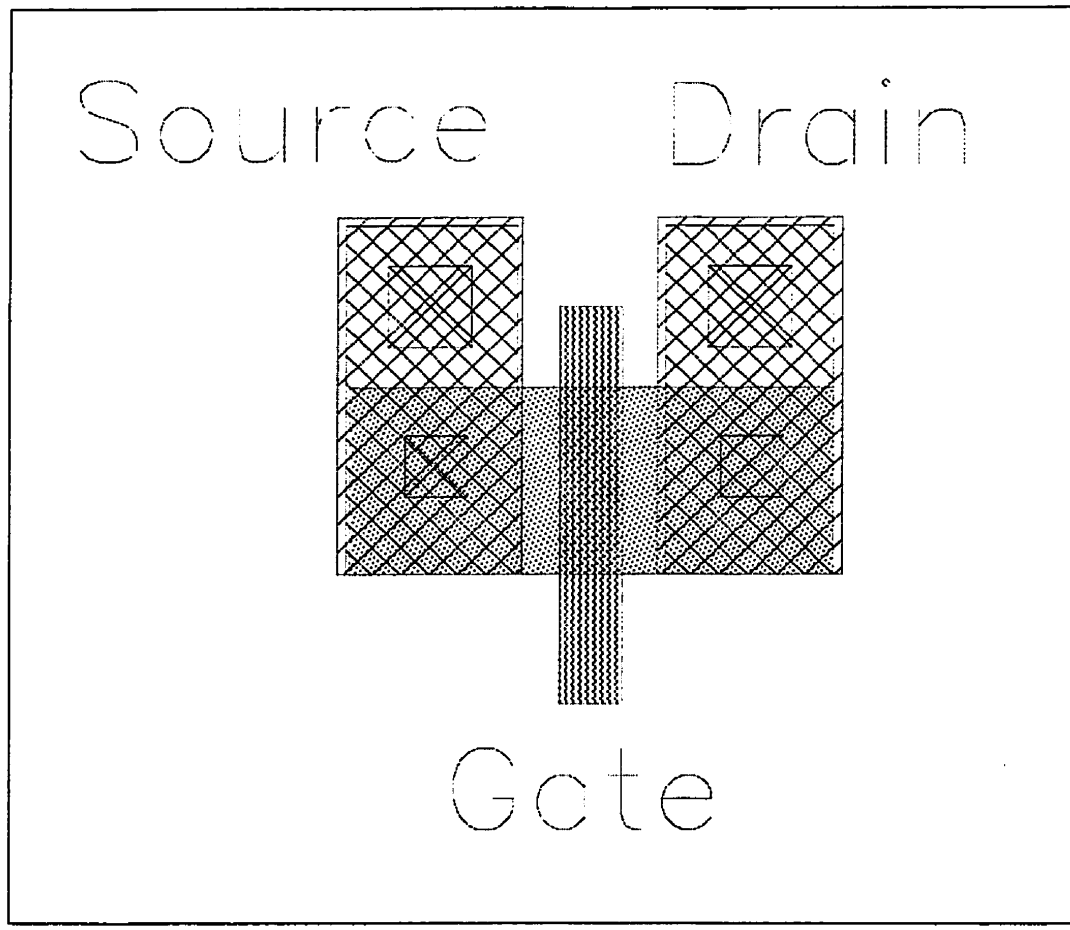


Figure A4.2 Layout of a minimum dimension n-type pass gate

Layout Design of the On-Chip Pulse Generator IC

The layout design of the On-Chip Pulse Generator IC is shown in figure A5.1. Note that the layout design was a modification of the layout design of the Open-Front End IC with the inclusion of a 1KΩ resistor, a 0.95pF capacitor, an inverter and a protection diode. A minimum dimension n-type pass gate was used as an analog switch.

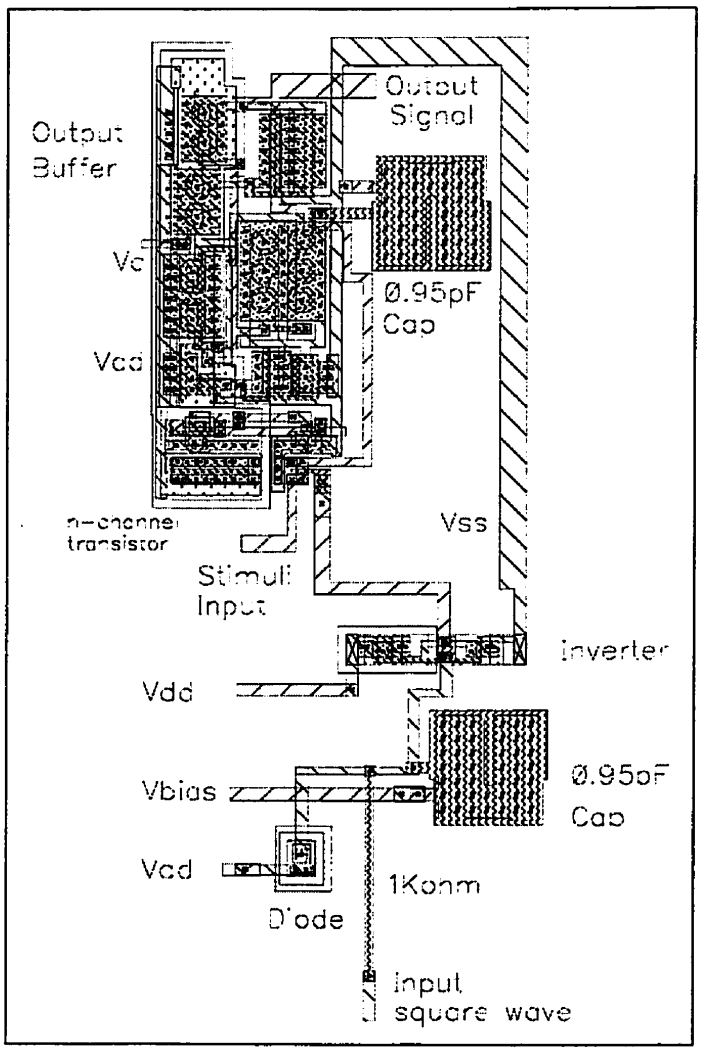


Figure A5.1 Layout of the On-Chip Pulse Generator IC

Layout Design of the Multi-Node Analog DFT IC

A6.1 Layout of minimum dimension n-type pass gate

A minimum dimension n-type pass gate was designed using Mitel 1.5μm process. The pass gate was used as analog switches in the Multi-Node Analog DFT IC. Figure A6.1 shows the layout design of the n-type pass gate.

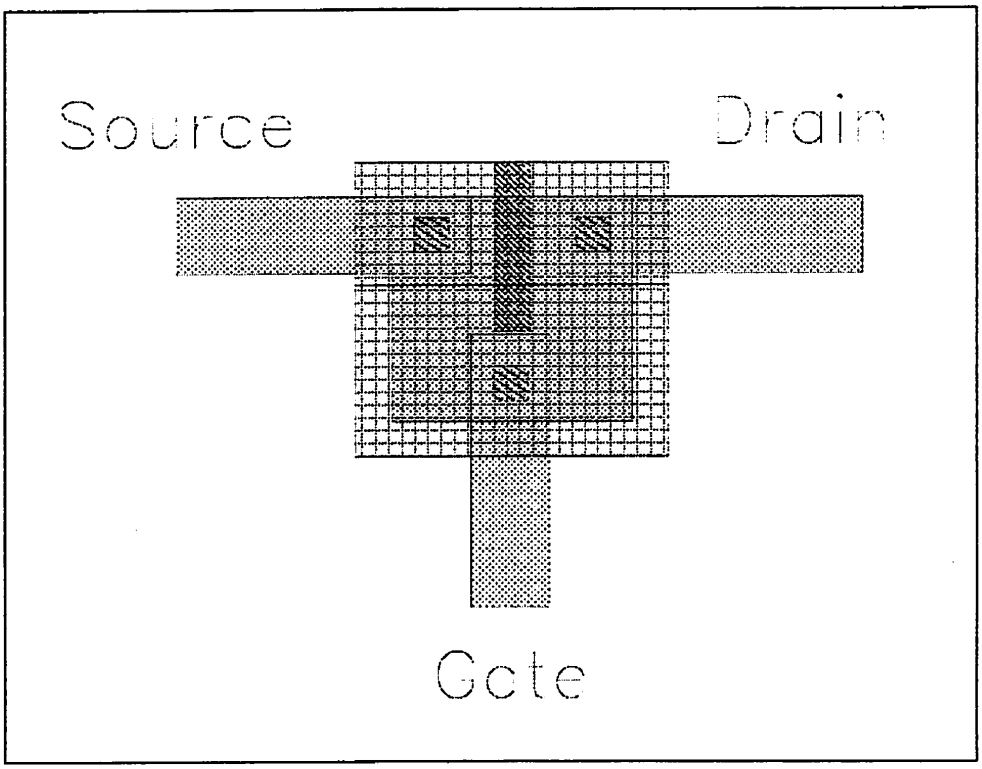


Figure A6.1 Layout of a minimum dimension n-type pass gate

A6.2 Layout and schematic of the analog OpAmp

The unity gain OpAmp DUT and output buffer used in the Multi-Node Analog DFT IC was designed using an analog OpAmp extracted from Mitel's 1.5μm analog cell library. Unity gain OpAmp and buffer was obtained by connecting the negative input

schematic of the analog OpAmp respectively.

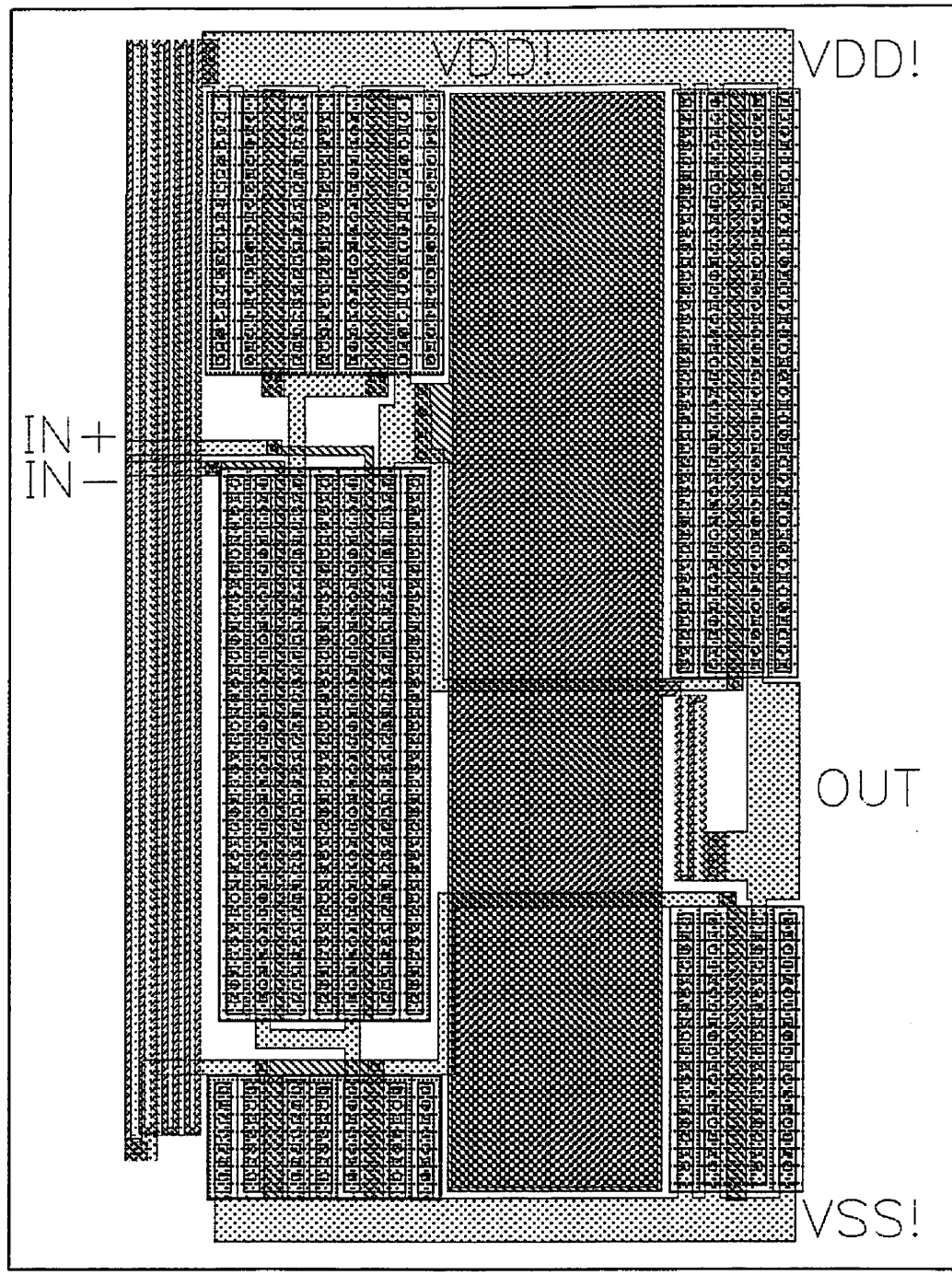


Figure A6.2 Layout of an analog OpAmp

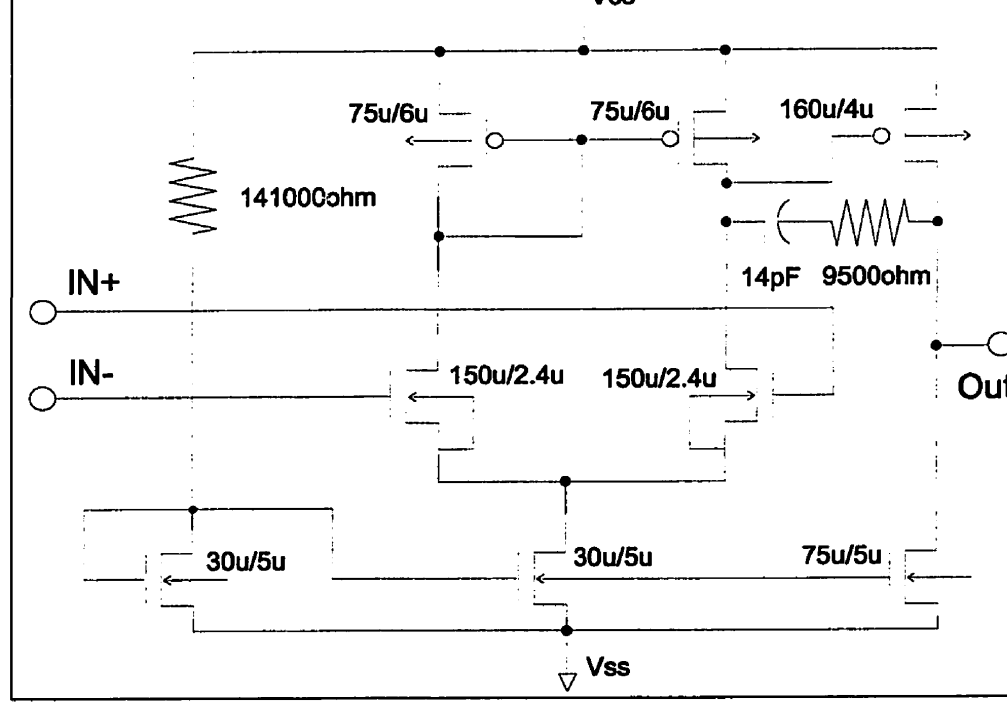


Figure A6.3 Schematic for an analog OpAmp

A6.3 Layout of the Multi-Node Analog DFT IC

The layout design of the Multi-Node Analog DFT IC is shown in figure A6.4. Note that there were two DUTs, an analog OpAmp and an inverter, and two direct input from the package pins. Minimum dimension n-type transistors were used as analog switches.

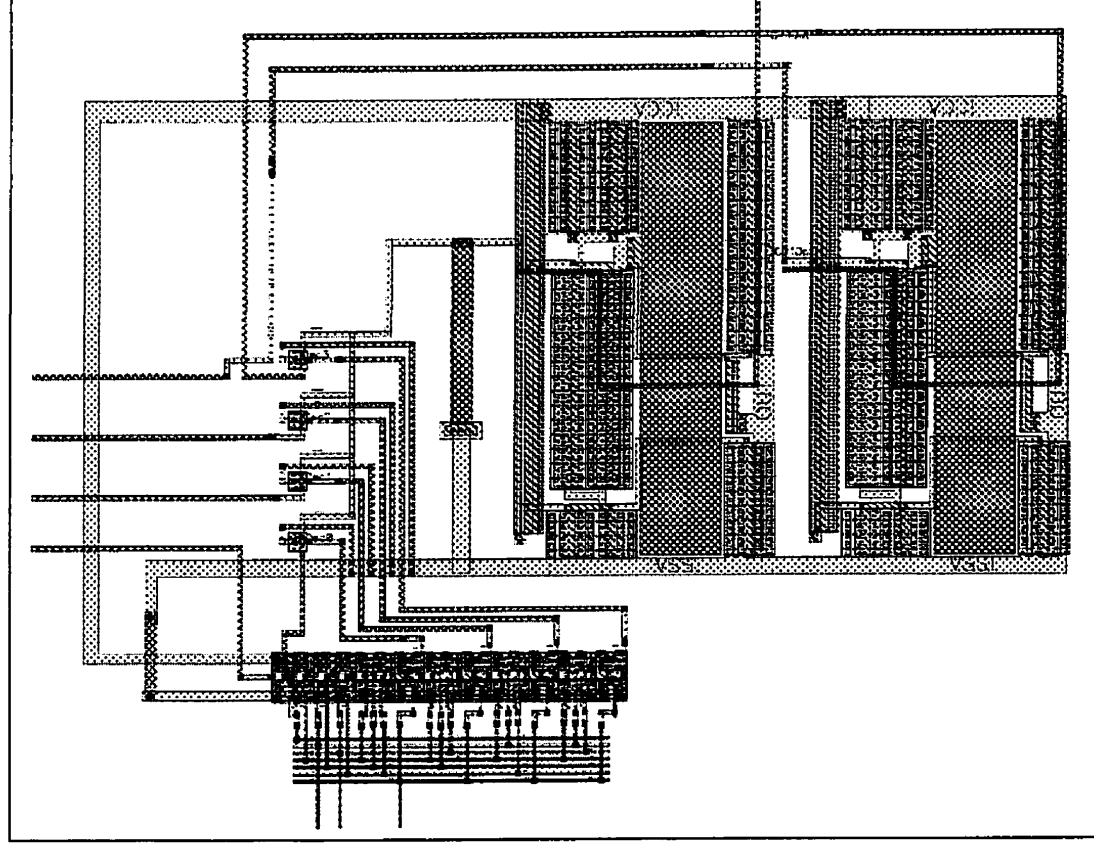


Figure A6.4 Layout for the Multi-Node Analog DFT IC

THD data tables and calculations

A7.1 THD of the sinusoid test signal

The sinusoid test signals generated by HP 8464A RF generator were tested for the most suitable signal to be used for prototype IC THD measurements. Total harmonics distortion of a 9.991MHz sinusoid test signal at various signal levels are listed in table A7.1.

Table A7.1 THD of a sinusoid test signal source at various amplitudes:

Sinusoid signal level (dBm):	THD measured:
-15	0.153%
-14	0.144%
-13	0.137%
-12	0.123%
-11	0.119%
-10	0.113%
-9	0.112%
-8	0.113%
-7	0.119%
-5	0.122%

The THD was calculated by using formula 4-3. From the table, it was found that sinusoid signals of-5dBm to –12dBm were most stable in term of their THD. Sinusoid signals within this signal level range were used for prototype ICs testing.

To measure the added distortion of the output signal of the OpAmp DUT IC, a 9.991MHz –11dBm sinusoid test signal was fed into the input port and being sampled at 10MHz. The power level of the input test signal and its harmonics, and the output signal of the OpAmp DUT IC and its harmonics were measured for THD calculations. The power level of the signals are listed in table A7.2. The first column represents the spectral of the output signal and its harmonics (up to 7th harmonic). The second column represents the signal level of the input signal and its harmonics while the third column represents the output signal level and its harmonics.

Table A7.2 THD of the input test signal and the output of the OpAmp DUT IC

Output frequency (KHz):	Sinusoid input Test signal	Output Of the OpAmp DUT IC
9	-10.39	-12.09
18	-76.84	-79.54
27	-72.37	-71.00
36	-75.85	-78.35
45	-78.21	-80.44
54	-81.95	-84.37
63	-85.14	-87.23
THD (%)	0.119 %	0.139%
ΔTHD (%)	0.020 %	
ΔTHD (dB)	-74.0 dB	

The measurement and calculations showed that the added distortion at the output of the OpAmp DUT was –74.0dB.

To measure the added distortion to the output signal of the Probe-Pad IC, the same procedure stated in section A7.2 were followed. The power level of the signals are listed in table A7.3.

Table A7.3 Calculation of added harmonics distortion of the output signal at various amplitude test signal for Probe-Pad IC

Output spectrum (KHz):	Output signal level (-11.0dBm input)
9	-11.71
18	-75.55
27	-69.68
36	-77.16
45	-80.66
54	-84.53
63	-88.46
THD (%)	0.158 %
ΔTHD (%)	0.039 %
ΔTHD (dB)	-68.2 dB

The measurement and calculation showed that the added distortion of the output of the Probe-Pad IC –68.2dB for input signal level of –11dBm.

To measure the added distortion to the output signal of the Open-Front End IC, control pulses with pulse widths of 500ps, 1ns and 2ns were used for prototype testing. The power level the output signals of the Probe-Pad IC and their harmonics were measured for THD calculations. The power level of the signals are listed in table A7.4.

Table A7.4 Calculation of added harmonics distortion of the output signal with various pulse widths for the Open-Front End IC

Output spectrum (KHz)	Output signal level (500ps pulses)	Output signal level (1ns pulses)	Output signal level (2ns pulses)
9	-12.47	-11.28	-11.14
18	-50.43	-59.68	-69.74
27	-72.24	-70.13	-68.58
36	-87.44	-79.12	-77.16
45	-89.80	-82.60	-78.60
54	-90.07	-85.56	-84.88
63	noise floor level	-89.52	-86.02
THD (%)	1.26%	0.401%	0.192%
ΔTHD (%)	1.141%	0.282%	0.073%
ΔTHD (dB)	-38.9 dB	-51.0 dB	-62.7 dB

The measurement and calculation showed that the added distortion at the output of the Open-Front End IC was –38.9dB for control pulse widths (τ) of 500ps, -51.0dB for τ of 1ns, and –62.7dB for τ of 2ns.

Schematic of a Mini-Circuits GaAs Switch

The square wave test stimuli used for transient analysis was generated by using a Mini-Circuits ZYSWA-2-50DR GaAs switch. The switch is able to generate fast rising and falling edges with slew rates of 833.3V/μs and –1000.0V/μs. The switch has an RF input, a TTL signal input and two outputs (output #1 and Output #2). Both Output #1 and Output #2 require 50Ω termination (see figure A8.1). The switch is powered by +5V and –5V power supplies. There are a total of four transistors on-chip (M1, M2, M3, and M4), and a TTL Driver.

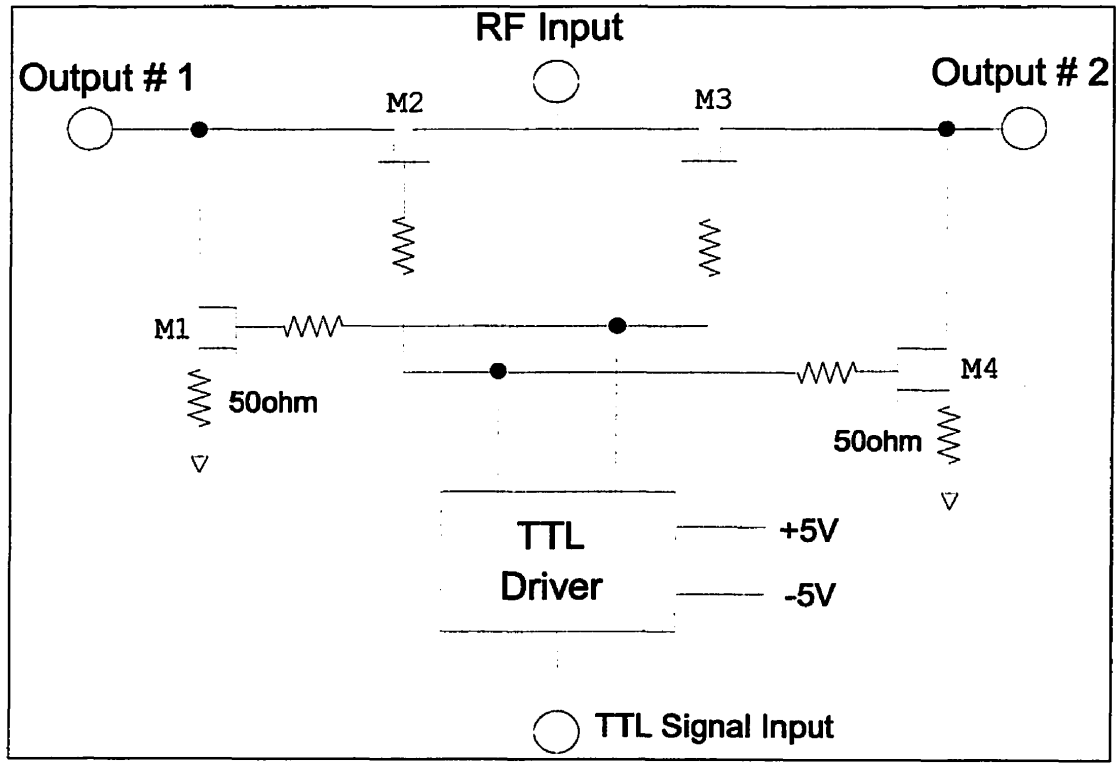
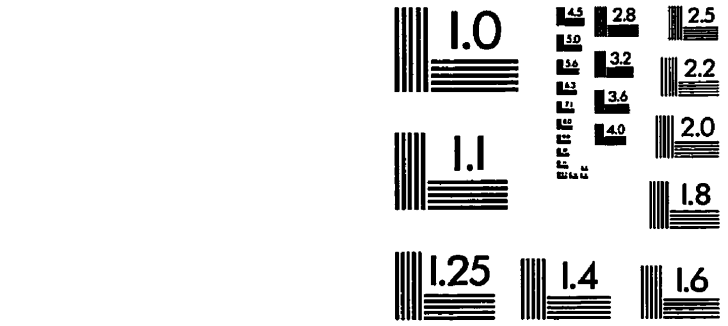
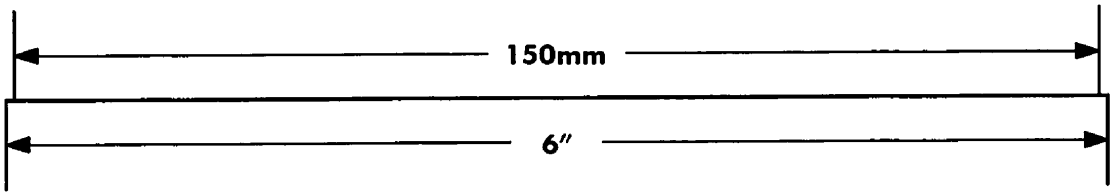


Figure A8.1 Schematic for a Mini-Circuits ZYSWA-2-50-DR GaAs switch [104]

drives the four transistors. Referring to figure A8.1, only one pair of transistors, either M1 and M3 or M2 and M4, is on at any instant. When transistors M1 and M3 are turned on, Output #1 will be driven to signal ground while the RF signal is passed through to Output #2. When transistors M2 and M4 are turned on, the opposite is true.

In order to generate a 1MHz square wave with fast rising and falling edges, the RF Input was connected to $2.0V_{dc}$ and a 1MHz TTL signals was fed into the TTL Input port. Since only one square wave signal was required for testing purposes, and to minimize impedance mismatch of the switch, a 50Ω termination resistor was connected at the Output #2. A 1MHz 1.2Vp-p square wave was generated on Output #1.





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