Monolithic Silicon Receiver Front-Ends for Portable Radio

by

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Abstract

This thesis is an effort to further the integration level of superheterodyne receiver front ends for portable radio using state-of-the-art submicron silicon bipolar technology. A key contribution is the development of a viable monolithic image reject filter. Using this filter, monolithic inductors and transformers are exploited to realize a low power superheterodyne receiver front-end. LC resonators are used to advantage to realize the required passband and reject responses.

Superheterodyne receivers for portable radio applications require substantial image rejection (80 to 100dB) routinely provided by off-chip passive filters. These filters are costly and therefore it is useful to develop integrated solutions. The original monolithic image reject filter developed in this thesis was a notch filter realized using an LC series resonator which was Q enhanced by means of a negative resistance circuit. The circuit was demonstrated to be stable even with very high Qs. A first version fabricated in 0.8micron BiCMOS showed more than 50dB image rejection at 2.5GHz. This filter was then made tunable and integrated with an LNA and a mixer.

A 1.9GHz fully monolithic silicon superheterodyne receiver front-end was demonstrated consisting of an LNA, a tunable image reject filter and a Gilbert cell mixer integrated in one silicon die. The receiver was designed to operate with a 2.2GHz LO for a 300MHz IF. Various chip versions were fabricated on a 0.5micron, 25GHz f_T bipolar technology. Measured performance for the packaged receiver with its input matched to 50 ohms was: Conversion Gain 26.3dB, Noise Figure 4.6dB, Input IP3 -19dBm, Image Rejection 65dB, and current consumption 15.9mA at +3V (48mW). The image rejection was tunable from 2.34 to 2.55GHz by means of an on-chip varactor. Another version used a transformer coupled mixer instead of a Gilbert cell. This chip worked well with a 2.5V DC supply, consuming only 21.5mW with performance suitable for DECT operation. A comparison with state-of-the-art monolithic image reject mixers shows that our receivers outperform the image reject mixer in terms of image rejection and power consumption.

The image reject filter requires on-chip tuning. Various approaches for this are discussed at the end of the thesis.

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Chapter 1 Introduction

Since its invention in 1918 the superheterodyne receiver has become the most popular receiver architecture. Today superheterodyne receivers are state-of-the-art in mobile communications. A superheterodyne receiver front-end consists of a Low Noise Amplifier (LNA), an image filter and a mixer with a local oscillator. The LNA is required to ensure good sensitivity, that is, to enable the receiver to detect very weak signals. Current cellular standards require receivers with high sensitivity, hence an LNA with very low noise figure is required. Additionally the LNA must provide sufficient gain to suppress the noise generated by the stages that follow. The image filter is required to suppress the unwanted image frequency located two Intermediate Frequencies (IFs) away from the desired radio frequency (RF). Finally the mixer allows the translation of the desired signal from the RF frequency to the Intermediate Frequency (IF), usually a lower frequency, for further processing by the receiver backend.

Currently off-chip passive filters, such as ceramic filters and surface acoustic wave (SAW) filters are routinely used for image rejection. These off-chip filters add complexity to the circuit, increase the number of pins required in the package, cause chip interface problems as typically 50 ohm matching networks are required, and increase the production cost. These filters represent the major impediment to raising the level of integration of wireless radios, since they cannot be easily implemented monolithically [1]. Hence, it would be highly desirable to develop monolithic image rejection filters with low power consumption.

The required image-rejection for cellular application varies from 80 to 100dB depending on the standard and the selected IF (ideally, infinite rejection is desirable). A ceramic bandpass filter is typically installed before the LNA providing 30 to 40dB of image rejection. Therefore on-chip rejection of 50dB or higher would be desirable to meet cellular requirements. To date monolithic rejection has only been achieved using the classical image reject mixer. This is a somewhat complicated circuit with significant power consumption and the best reported rejection has typically been in the order of 30dB although very recently Philips has introduced an improved part with 38dB rejection. However, additional rejection is still required to meet existing cellular standards. Hence it

would be highly beneficial to realize a monolithic image reject filter which would then be integrated between the LNA and the mixer. It is important to note that such an image reject filter need not be exclusive but could be complementary to the image reject mixer approach. Thus by combining an on-chip image reject filter with an integrated image reject mixer a very high on-chip image rejection could be obtained.

In this thesis it is demonstrated that a low power monolithic silicon superheterodyne receiver front-end with on-chip image reject filter can be realized using tuned circuits. This is made possible with the recent availability of on-chip inductors and/or on-chip transformers as well as state-of-the-art sub-micron silicon technology. This would further the level of integration presently available. It is hoped that the results of this work will generate valuable information such as design trade-offs, technology limitations, problems due to substrate coupling and modelling and simulation limitations. The proposed image filter is a notch filter tuned to suppress the image. This work will show that by using a notch filter instead of a bandpass filter, monolithic realization of a tunable image reject filter with performance suitable for portable radio is possible. Concentration is on adequacy of performance rather than on actual tuning circuits. This is because it is not very useful to demonstrate on-chip tuning if the filters being tuned are not capable of being actually used due to poor noise and linearity as has been the case with previous monolithic filters.

First the low power monolithic image reject filter developed as part of this work will be introduced. The image reject filter principle of operation will be presented and its transfer function derived. The design methodology will be explained, including design guidelines to ensure circuit stability. This filter will then be integrated with an LNA and a mixer to realize a monolithic superheterodyne receiver front-end in a 0.5micron bipolar process. This will demonstrate the validity of using a notch filter to suppress the image. Two approaches will be studied, one using a Gilbert cell mixer and the other a balun mixer previously developed at Carleton University. The advantages and disadvantages of each approach will be discussed.

This thesis is divided in the following chapters:

Chapter 1: Introductory concepts. Explanation of the superheterodyne principle, fundamental concepts and figures of merit used in radio, and key performance requirements of existing cellular standards. Concludes with a review of front-end receiver architectures.

Chapter 2: Overview of image rejection methods. Review of the state-of the art in integrated image reject receiver front-ends. Review of state-of-the-art transceivers with off-chip image filtering.

Chapter 3: Theory, design, fabrication and testing of a monolithic image reject filter. In this chapter the principles of operation of a proposed low power monolithic filter for image rejection will be described. Simulated and measured results on a 0.8 micron BiCMOS implementation are presented as proof of concept.

Chapter 4: An integrated LNA and image reject filter. In this chapter the design issues concerning the integration of an LNA with the above image reject filter are shown. Simulated results on NORTEL's 0.5 micron bipolar technology will be presented.

Chapter 5: RF Mixer design. Two monolithic balanced mixers are introduced. The conventional Gilbert cell and the more recent transformer coupled mixer are reviewed. Key performance issues are discussed and simulation and measurement results presented.

Chapter 6: A monolithic silicon receiver front-end architecture. This chapter describes an integrated superheterodyne receiver front-end consisting of an LNA, image reject filter and Gilbert cell mixer in one silicon die.

Chapter 7: Various improved receiver versions investigated in this work are described here. Simulation results on NORTEL's 0.5 micron bipolar technology are presented. Measurements are presented as well and compared with the simulations. Finally, the receiver front-ends developed in this work are compared with the state-of-the-art.

Chapter 8 Discussion and conclusions, including a review of the obtained results, claims and future work.

1.1 The superheterodyne principle

Early in the 20th century a scientist by the name of Fessenden proposed to improve the wireless receiver of the day by the method that he called "heterodyning". He coined the new word from the Greek word "heteros", meaning different, and "dynamis", meaning power. His scheme involved the non-linear mixing of the incoming Morse-code signals with a locally generated, sinusoidal signal, so that the newly created output signal was at the difference frequency between the two original input signals [2]. The difference frequency was audible, and this allowed the receiver operator to recognize the dot and dash tones representing the Morse codes of the various characters. His proposal was doomed to failure in those days because there was no good way to generate the local oscillator signal.

Later, during the First World War, Edwin Armstrong, a Major in the U.S. Army Signal Corps stationed in France, wanted to amplify radio signals in the several megahertz frequency range but the vacuum tubes of the time were only able to amplify signals with frequencies up to 100KHz. He got around this difficulty by using its own version of heterodyning. Instead of mixing to produce an audible output frequency, he chose to produce a frequency considerably above the audio range, an above-sonic intermediate frequency of about 50KHz. He named his new creation the superheterodyne [2].

The basic concept of the superheterodyne radio receiver is illustrated in Fig.1-1. The incoming radio frequency (RF) signal is amplified and combined with the sinusoidal input of a local oscillator in a mixer. This mixer is sometimes called the first detector. The mixer output contains the difference between the frequencies of the local oscillator and the incoming signal. The sum frequency is also present as well as other intermodulation products due to nonlinearities. The design of the receiver is such that when it is tuned to the frequency of another incoming signal the frequency of the local oscillator is automatically changed (tuned) so as to maintain the same difference frequency as before; this process is called tracking. The difference frequency is called the intermediate frequency (IF) and the circuits that amplify these signals are called IF amplifiers. A key advantage of a superheterodyne receiver is that the IF is at a fixed frequency.

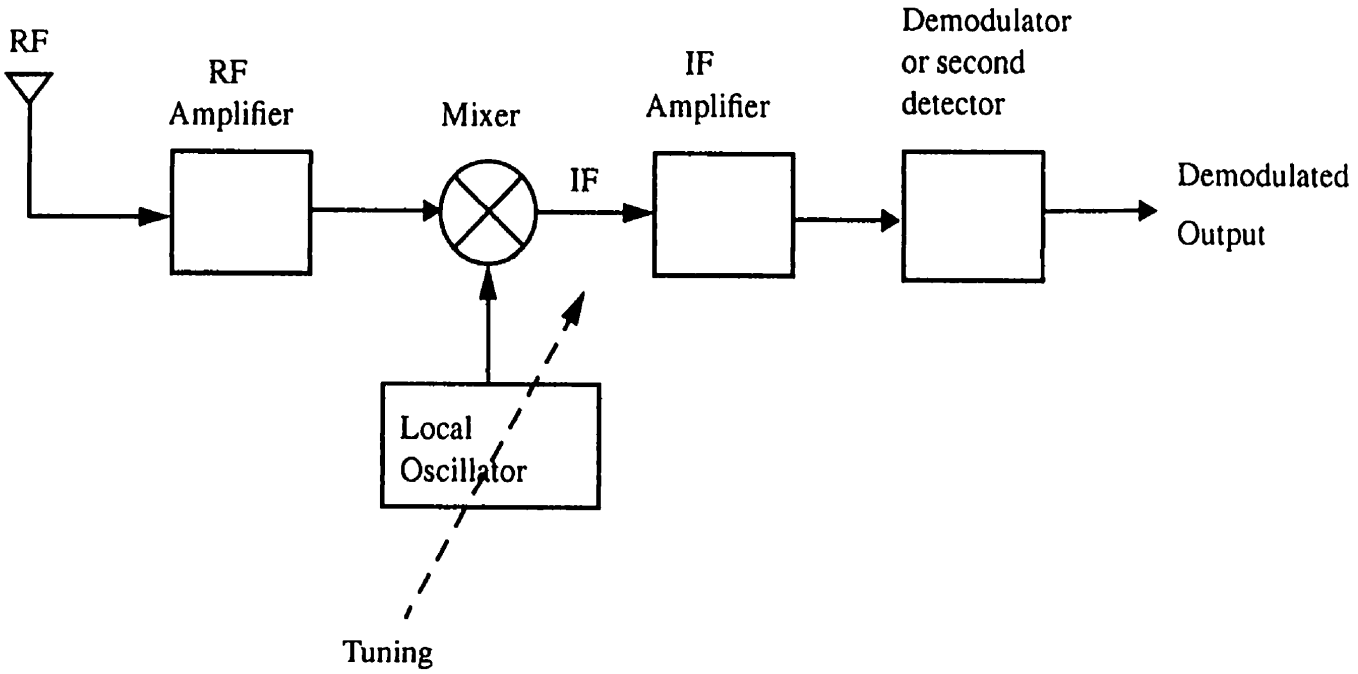

Figure 1-1: Simplified block diagram of a superheterodyne receiver

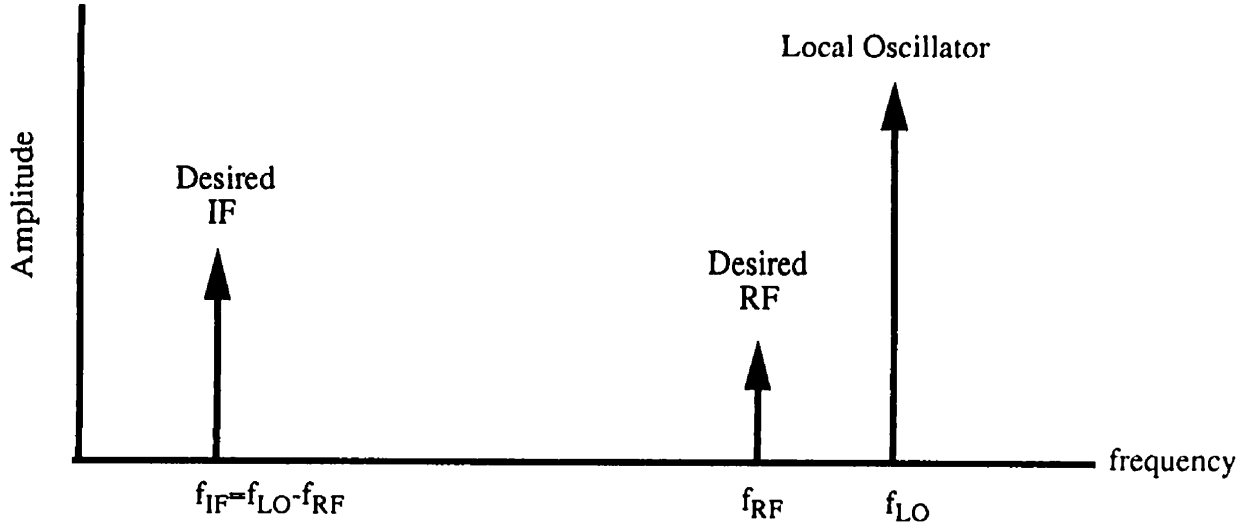

Figure 1-2: Difference mixing with high-side injection, downconversion

Figure 1-2 shows an ideal spectrum of a superheterodyne receiver with a so-called high side injection (HSI) local oscillator, and with the LO located one IF above the desired RF. As shown, the IF is the difference between the local oscillator and the desired RF frequencies. Hence, the desired RF has been downconverted or translated to an IF frequency. The same IF frequency could result from a low side injection (LSI) local oscillator if the LO was located one IF below the desired RF frequency.

Note that Figure 1-2 is an ideal case, in the real situation all these components have harmonics and there are intermodulation products between them.

1.2 Fundamental radio concepts

In this section some fundamental radio receiver concepts will be very briefly reviewed.

1.2.1 Sensitivity

Sensitivity is a measure of the ability of a receiver to respond to weak RF signals.

Receiver sensitivity is normally defined as the signal strength needed to produce a certain signal to noise ratio, or, for digital systems, the level needed to produce a certain Bit Error Rate (BER). Current portable radio applications require highly sensitive receivers as will be illustrated in section 1.3.

The sensitivity is determined by the receiver noise figure which is briefly explained in the next subsection.

1.2.2 Noise factor and noise figure

The noise factor (F) compares the output noise power of the actual noisy system to the output noise power that would be delivered by the system if the only source of noise were the thermal noise in the source resistance at the standard temperature of 290°K [2]. The noise factor of an ideal noiseless system is unity because the system would not add any noise of its own, that is in a noiseless system the output SNR is equal to the input SNR.

Thus, for a specified frequency:

$$F = \frac{N_{out}}{N_{in} \cdot Gain} = \frac{SNR_{input}}{SNR_{output}} \tag{1.1}$$

where N_{out} = output available noise power of the actual noisy system,

N_{in} = available thermal noise power from the source

$Gain$ = available signal power gain

SNR = signal to noise ratio

The noise figure (NF) is obtained by expressing the noise factor in dB as follows.

$$NF = 10 \cdot \log F \Rightarrow dB \tag{1.2}$$

Practical systems always have F>1 and consequently NF > 0dB. A high quality receiver will exhibit low noise figure.

As was shown in Figure 1-1 a typical superheterodyne receiver consists of several stages. It is therefore important to express the overall receiver noise factor in terms of the noise factors and power gains of the individual stages.

In the case of n cascaded stages the overall noise factor can be obtained using the well known Friis formula

$$F = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 \cdot G_2} + \ldots + \frac{(F_n - 1)}{(G_1 \cdot G_2) \ldots G_{n-1}} \tag{1.3}$$

where F_1, G_1 are the noise factor and the power gain of the first stage, F_2, G_2 are the noise factor and the power gain of the second stage and so on. This formula shows that the relative noise contribution of each stage diminishes as the power gain of all the preceding stages increases. Note also that the first stage contributes the most as there is no gain preceding it. That is why in a receiver with good sensitivity an LNA with low noise figure and substantial gain is required. The LNA gain is needed to reduce the noise contribution of the stages that follow, particularly the mixer which is typically noisy.

The required noise figure for receivers for portable radio applications will be introduced in section 1.3.

1.2.3 Selectivity

Selectivity is a measure of how well a receiver can select a desired station to the exclusion of all others. The superheterodyne receiver improves selectivity but it also introduces undesirable image responses which are explained below.

1.2.4 Image response

Suppose we use a superheterodyne receiver to receive a 1.9GHz RF signal and downconvert it to a 300MHz intermediate frequency by using a high side injection (HSI) 2.2GHz local oscillator. It turns out that a 2.5GHz RF signal will also generate a 300MHz intermediate frequency simply because the difference between 2.5GHz and the 2.2GHz LO is also 300MHz, the desired intermediate frequency. That is, the 2.2GHz signal is low side injection (LSI) for the RF signal which happens to exist at 2.5GHz. Two RF signal bands are mixing down to the same IF frequency as illustrated in Figure 1-3.

The undesired 2.5GHz RF signal is referred to as the image signal and 2.5GHz is called the image frequency of 1.9GHz. The IF output that is obtained from an input signal at the image frequency is called the image response.

In general when HSI downconversion is used the image frequency is given by:

$$f_{image} = f_{RF} + 2 \cdot IF \tag{1.4}$$

where f_{RF} is the desired frequency to which the receiver is tuned. Clearly, the IF frequency defines where the undesired image will be. A higher IF places the undesired image further away from the desired RF frequency thus relaxing the task of the image filter. For good image rejection, it is recommended to make the IF as high as possible. Also, when the LO is above the desired RF band, the image frequency is above the RF and easier to deal with. That is, HSI is preferable to LSI, except in that it makes it necessary to generate a higher LO frequency.

The image response of a receiver is said to be improved when the output produced by a signal at the image frequency is made to be less than what it was before, in other words there is now greater image rejection.

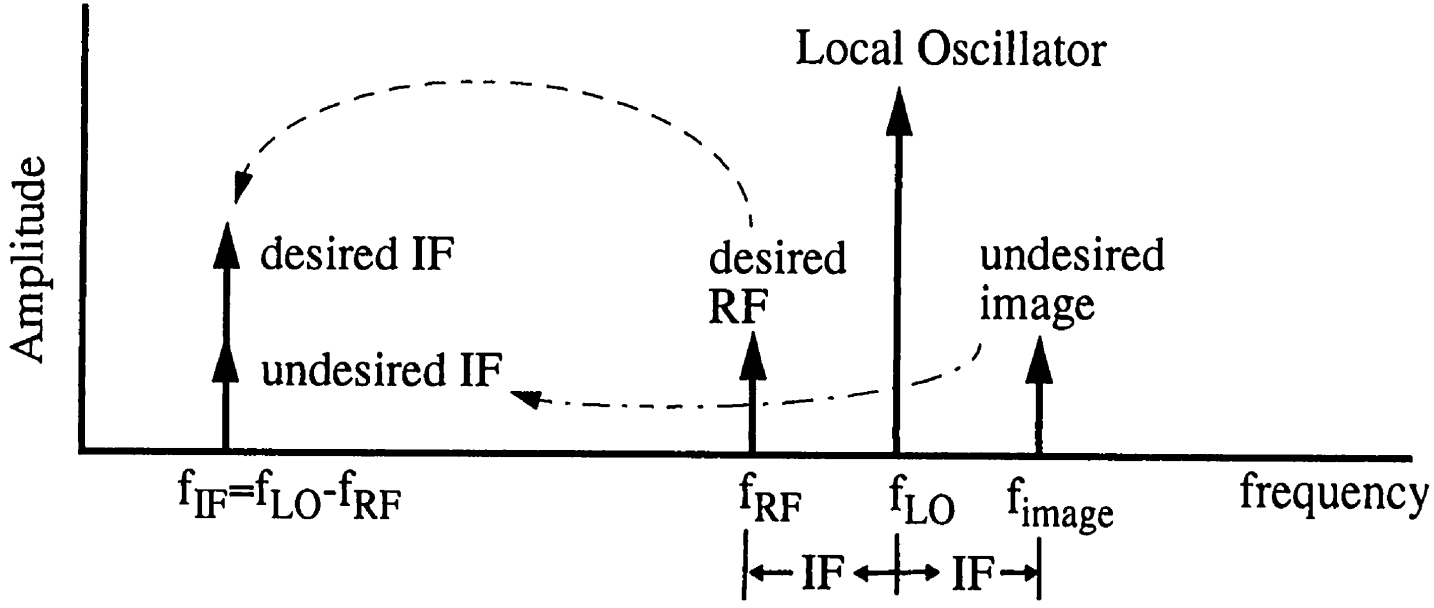

Figure 1-3: Difference mixing with high-side injection, downconversion showing image response

1.2.5 Third-order intercept point

When the sum of two sinusoids is applied to the input of a nonlinear device, the output contains harmonics of the original frequencies and various intermodulation products (IM products). It is usual to allow the amplitude of the two input sinusoidals to be equal when using them together to test an amplifier or a radio receiver for its linearity [2]. If the two frequencies are sufficiently close and centered on the symmetric response characteristic, the outputs at these two frequencies will have the same amplitude.

To illustrate, let the two equal amplitude input sinusoids have frequencies f_1 and f_2, and let f_2-f_1=Δf. Then, assuming that the input amplitudes are sufficient to drive the system into nonlinearity, the third-order IM products are:

$$2f_2 - f_1 = f_2 + \Delta f \qquad 2f_1 - f_2 = f_1 - \Delta f \tag{1.5}$$

Typically Δf is small and these intermodulation products are in the desired passband, which is why they are particularly harmful. Hence, the system output now contains the fundamentals at f_1 and f_2 and two additional IM products at f1-Δf and f2+Δf. The lower the amplitude of these IM products the more linear the circuit. A plot of the input power versus the output power for both the fundamental and the third order IM products would be as shown in Figure 1-4.

The intercept point cannot be measured directly because compression destroys the linearity of the lines at the higher power levels required [2]. The intercept point is the point at which the extrapolated fundamental response and the extrapolated third-order spurious response lines intersect. Its location can be specified by its projection onto the input axis (input referred third order intercept point or IIP3) or onto the output axis (output referred third order intercept point or OIP3). IIP3 and OIP3 are related by the first order (linear) gain. The third-order input intercept point, in dBm, can be calculated from [3]:

$$IIP3 = \frac{R_s}{2} + P_1 \tag{1.6}$$

where R_s equals the suppression in dB of third order products and P_1 equals the input signal power level in dBm at which the relative suppression is measured. In Fig. 1-4 the

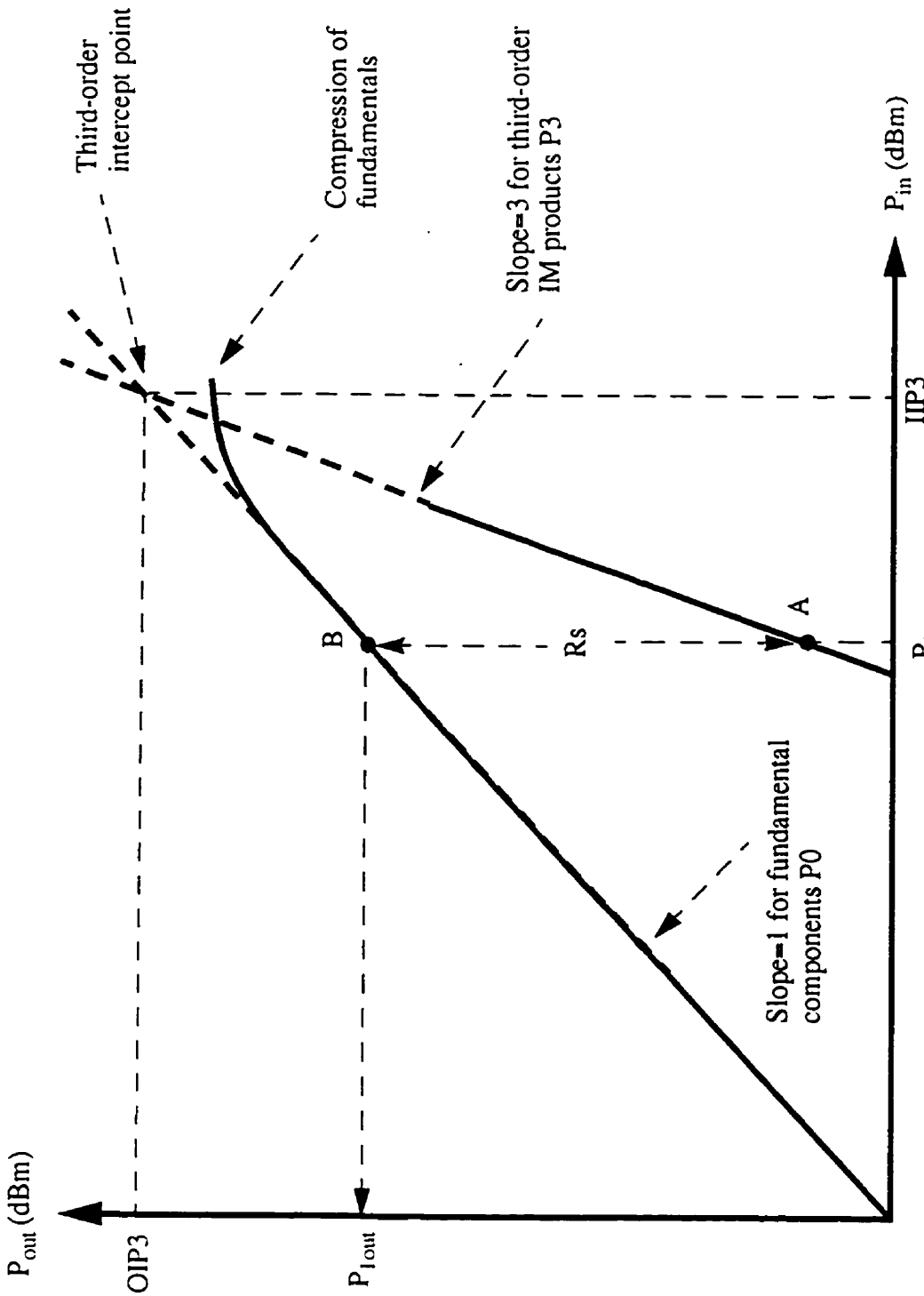

Figure 1-4: The third order intercept point

suppression corresponding to input power P_1 is indicated by the dashed line between points A and B (R_s).

The third order intercept point (IP3) is a popular figure of merit for the linearity of a circuit. It indicates the theoretical power level which when applied to the circuit would generate third order intermodulation products as large as the main harmonic as illustrated in Figure 1-4. Obviously the higher the IP3 the more linear the circuit at a given input level.

1.3 Receiver performance requirements for portable radio

The receiver explored in this thesis is not designed to comply with any particular specification. However, it will be important to compare the performance of the proposed receiver with the requirements of existing cellular communication systems. These requirements are briefly described below.

The required noise figure can be derived from the sensitivity specification and the channel bandwidth. This noise figure results from the contributions of all the components of the receiver front-end which typically include a diplexer (or switch which allows the antenna to be operated in receive or transmit mode), a passive bandpass filter, the LNA, an image reject filter and the mixer. Usually, there is also a small contribution due to the IF amplifiers and the rest of the backend circuit, but due to the large gain of the front-end, the IF amplifier noise usually adds little to the overall noise figure.

1.3.1 Digital European Cordless Telecommunications (DECT)

DECT is a digital cordless telephone standard. The frequency band allocated for DECT is from 1881MHz to 1897MHz [4].

The required sensitivity for all DECT equipment is -83dBm and for equipment meant for public access use, the requirement is -86dBm. It can be shown that these sensitivities are equivalent to a maximum noise figure of 16.8dB for all DECT equipment and 13.8dB for equipment meant for Public Access [4].

A DECT receiver is required to meet an intermodulation performance test. In this test the desired signal is specified at -73dBm and two undesired signals are located in adjacent

channels in such a manner that their intermodulation product falls into the desired frequency band. The level of the two undesired signals is defined at -46dBm and they should produce a third order intermodulation product no larger than -83dBm so as to maintain a co-channel rejection ratio of 10dB (i.e. the intermodulation product is 10dB below the desired -73dBm signal). It can be shown that to meet this requirement a -27.5dBm IIP3 is required in the receiver front-end.

Additionally, for a DECT superheterodyne receiver an image rejection in the order of 80 to 100dB is required [5].

1.3.2 Global System for Mobile Communications (GSM)

GSM is a digital cellular mobile radio system. The frequencies allocated for GSM are 890-915MHz for the uplink (portable hand-held to base station) and 935-960MHz for the downlink.

GSM receivers have more stringent requirements than DECT in both noise figure and linearity. Among the specifications in the GSM standard is a requirement that the receiver operate properly with input signals ranging from -102dBm to -15dBm [6].

For GSM, a sensitivity of -102dBm [7] is required which translates into a minimum noise figure of approximately 8dB for the overall receiver front-end. The linearity requirement is also high; a minimum IIP3 of -18dBm is required [8]. Hence, one of the challenges of a monolithic low power receiver front-end would be to exhibit performance suitable to meet the GSM specification.

GSM has also migrated into different and higher frequencies. Except for the frequencies used, all the features of the various GSM implementations (DCS-1800, PCS-1900) are similar to the more common 900MHz GSM system [9]. In this thesis when GSM is mentioned it refers to either the DCS-1800 or PCS-1900 standard.

A GSM receiver would require substantial image rejection. For example a DCS 1800 GSM receiver is required to operate in the 1805-1880MHz band. The receiver must be able to work well when receiving a useful signal frequency with -99dBm signal level, in the presence of out of band interferers with 0dBm power level located below 1705MHz or

above 1980MHz up to 12,750MHz. Hence, if a 300MHz IF was used, the image frequency would be located in the 2405-2480MHz band for a high side LO, or in the 1205-1260MHz for a low side LO. In either case, according to the specification, the interfering image could be as large as 0dBm while the desired signal is at -99dBm. This would indicate that to ensure a minimum SNR of say 10dB, the image should be rejected by 109dB.

1.4 Conventional superheterodyne receiver implementations

The purpose of this section is to familiarize the reader with existing receiver implementations. The most fundamental choice for a receiver architecture is between a superheterodyne or a direct conversion topology. Heterodyne transceivers are the most popular choice amongst manufacturers and are the state-of-the-art in mobile communications [10][11]. Direct conversion architectures which transfer the signal from RF to baseband in one step are theoretically simpler, and image frequencies do not occur [11] (thus saving the image filter), however direct conversion has not generally been successful due to implementation problems [10]. Hence in this thesis a superheterodyne receiver architecture is explored.

A typical superheterodyne receiver front-end would be as shown in Figure 1-5. A diplexer is usually installed after the antenna. The diplexer allows the sharing of the antenna by the receiver and the transmitter, which is not shown for simplicity. A ceramic bandpass filter is installed after the diplexer and before the LNA. This filter passes the desired RF signal and rejects out-of-band interferers including the image. Usually, 30 to 40dB image rejection is provided by this filter, depending on whether the interferer is below or above the passband. Typically, better rejection is obtained below the passband frequency. The ceramic filter usually presents 3dB insertion loss and its noise figure is also 3dB. The LNA must have low noise figure and sufficient gain to ensure an overall low noise figure of the whole receiver. The LNA is normally input and output matched to 50 ohms usually by using external components such as inductors and capacitors.

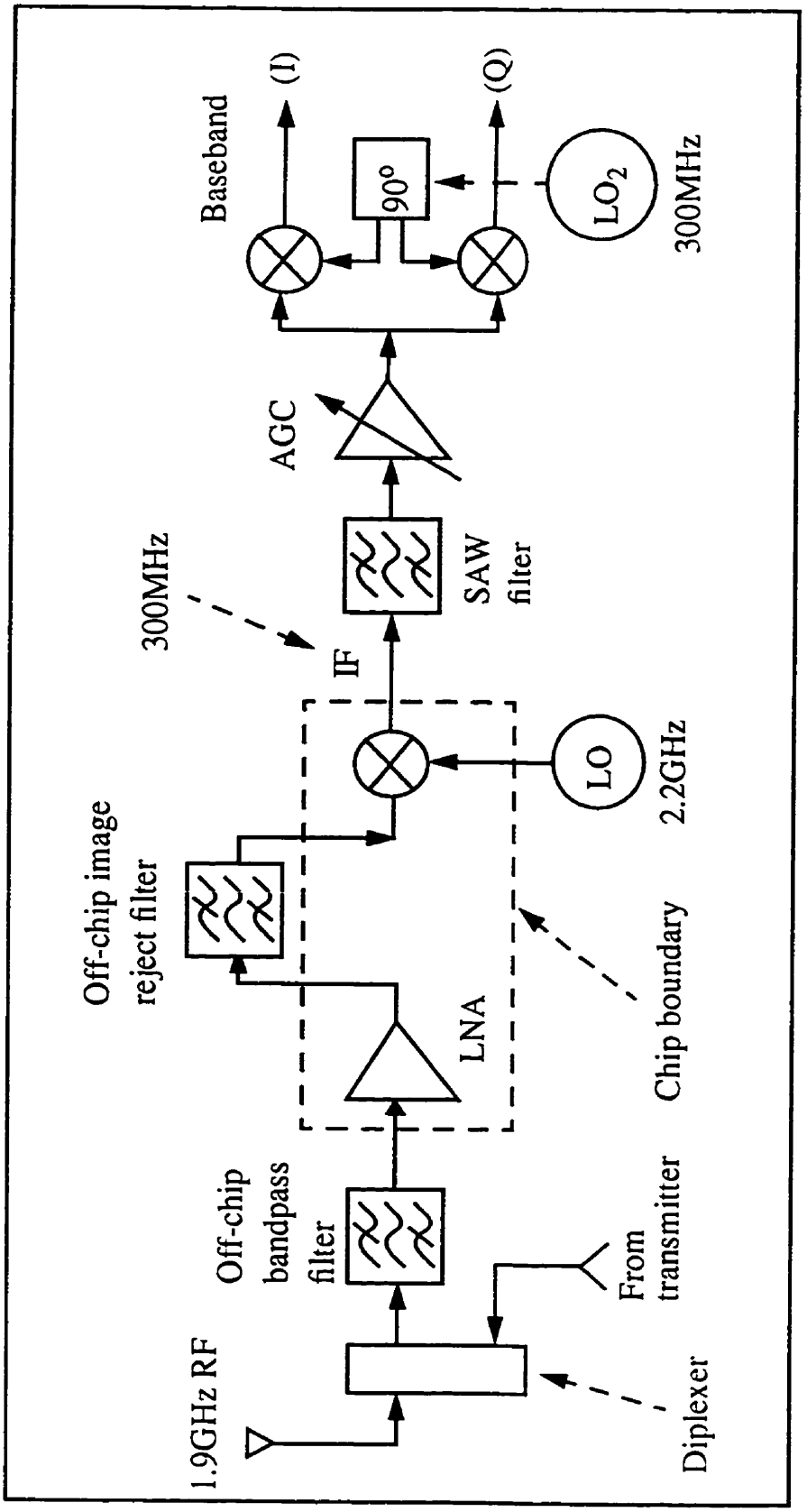

Figure 1-5: Typical superheterodyne receiver front-end

Following the LNA is a second passive bandpass filter, typically a SAW filter with approximately 4dB insertion loss. This second filter provides additional image rejection from 20 to 30dB depending on the location of the interferer. Observe that the LNA must have sufficient gain to compensate for the losses in the two passive filters and still maintain substantial gain before the mixer. The second filter output feeds into the mixer for downconversion to the selected IF frequency. At the mixer output, a SAW bandpass filter is normally used for channel selection and to reject spurious high frequency components such as RF and LO leakages. The IF SAW filter output feeds into an AGC amplifier whose output feeds two mixers, for downconversion into in-phase and quadrature baseband signals.

A survey of existing LNA implementations will be presented in section 2.4 to illustrate the existing state-of-the-art. Some receiver front-end implementations are briefly reviewed next, to show current trends in superheterodyne receiver design.

Volker [12] presents a 2GHz superheterodyne receiver for cordless phone applications. In his design the mixer downconverts the RF to a 110MHz IF, which is connected to a SAW filter by means of an off-chip transformer. However more recent designs are shifting to higher IFs. For example, Marshall [13] presents a 2.7V GSM transceiver IC. The receiver circuit uses a single superhet architecture with a 400MHz IF which is filtered with an external SAW filter. Veit [14] presents an 800MHz-2.1GHz transceiver chip set in which the receiver portion contains an LNA and a mixer. The mixer downconverts the received RF into a 246MHz IF signal which is then fed into a SAW filter for channel selection.

These higher IFs are made possible with advancements in SAW filter technology. Fenk [8] indicates that due to advances in SAW filter technology the IF-frequency range can now be shifted from 40-80MHz to around 250MHz. Such higher IFs result in smaller IF SAW filters and also relax the requirements on the image reject filters as the image moves away from the desired RF.

Carson [2] recommends to make the IF as high as possible for good image rejection. For these reasons a 300MHz IF was selected for the receiver front-end developed in this work, as shown in Section 1.5.

1.5 Proposed monolithic receiver architectures

Radio receiver architectures which appear promising for monolithic integration are briefly presented here.

Figure 1-6 shows the block diagram of a linear receiver, usually referred to as "single IF receiver" or "single conversion receiver" because there is only one downconversion stage before the baseband downconverter. A single IF approach is attractive for integration due to its simplicity, since using only one mixer there is a reduction in the amount of spurious signals [15] as well as the power consumption. Naturally, if desired, this first stage can be followed with a second IF stage which is then followed by the baseband downconverter. This would then be referred to as a dual conversion receiver.

The receiver front-end of Figure 1-6 consists of a passive bandpass filter, an LNA, an image reject filter and a mixer which translates the incoming 1.9GHz RF signal down to a 300MHz IF (this is the "single IF"). This IF is then fed to a SAW filter which is followed by a second mixing stage for downconversion to the in-phase and quadrature (I/Q) baseband signals. Note that the diplexer after the antenna is not included for simplicity.

In this thesis it is attempted to integrate the portion surrounded by dashed lines in Fig.1-6, consisting of the LNA, the image reject filter and the mixer, in one die. Comparing this with the conventional receiver of Figure 1-5 it can be seen that the second off-chip filter between the LNA and the mixer has been eliminated. The image filtering is now done on-chip. Since the LNA output does not go off-chip, the associated wire bonds, package pin and printed circuit board trace are eliminated, greatly simplifying the circuit modelling. Also the required matching networks which usually include inductors and capacitors at the filter input and output are eliminated. This reduces the parts count as well as manufacturing costs. Furthermore, the LNA does not have to drive a 50 ohm load any longer. The LNA-to-filter-input and the filter-output-to-mixer-input interfaces are now on-chip and can be done at higher impedance levels, thus improving the voltage gain.

Once such a monolithic front-end is achieved it could then be integrated with the VCO and the IF backend to realize a fully monolithic receiver.

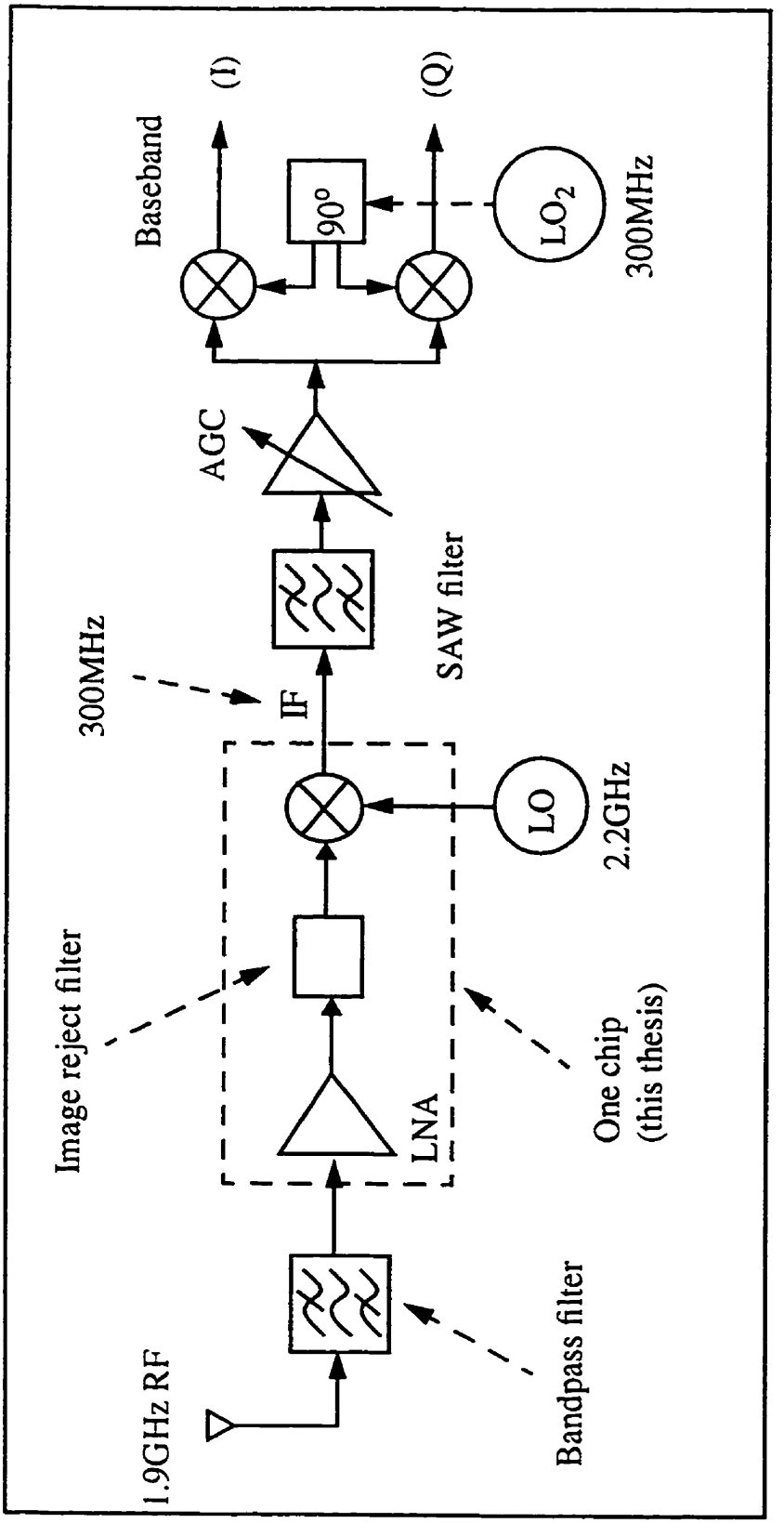

Figure 1-6: Single conversion and IF conversion to I/Q baseband

Another possible architecture is shown in Figure 1-7. This is still a single conversion receiver, in which two high frequency mixers are now used to generate in-phase and quadrature IFs, referred to as IF(I) and IF(Q). These IFs could then be sampled and processed with a processor to demodulate the signal. Here an analog-to-digital converter (A/D) capable of digitizing 300MHz signals would be required. Observe also that having the in-phase and quadrature IFs available, further image rejection is possible by appropriately processing these IF signals.

Thus the monolithic receiver front-end developed in this thesis could easily be augmented by adding one more mixer to realize the front-end shown with dashed lines in Figure 1-7. In this case the image reject filter would provide, say, 50dB image rejection and another 20/ to 30dB could be obtained by processing the quadrature IFs, for example using complex sigma-delta as proposed by Swaminathan [16]. In this manner a very high on-chip image rejection could be obtained. Adding to this the rejection provided by the passive filter before the LNA would result in over 100dB of image rejection for the complete receiver front-end. Observe that in Figure 1-7 no IF SAW filters are included, however in practice they may be required to alleviate the task of the A/D converter and avoid aliasing. If the IF SAW filters can be avoided then the complete receiver front-end could be integrated in one chip.

Observe also that with the recent realization of monolithic VCOs [17][18][19][20][21], it would be possible to integrate the local oscillator and its 90° phase shifting network with the receiver front-end. However, to realize a GSM receiver with integrated VCO, improvements in the phase noise performance of the monolithic VCOs are required. Only one research group [20] claims to have achieved an integrated VCO which meets the GSM requirement.

In conclusion, by having a monolithic image reject filter combined with an image reject mixer and a fast A/D converter could result in a fully integrated receiver front-end.

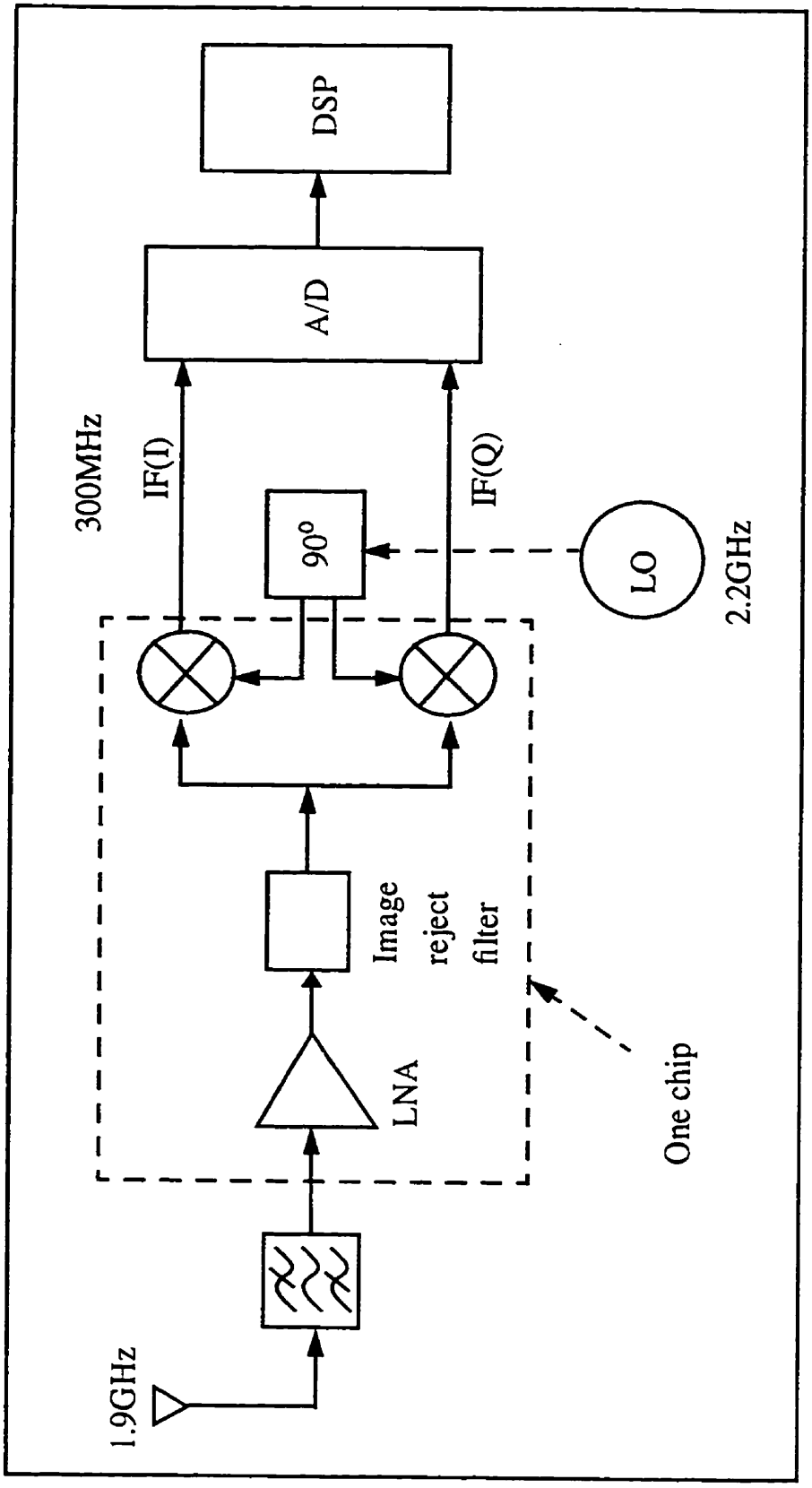

Figure 1-7: Single conversion with quadrature IF outputs and I/Q IF sampling

1.6 Thesis Objectives

This thesis explores the use of monolithic inductors and transformers to realize low power monolithic silicon receiver front-ends suitable for personal communication applications. This research shows that using on-chip inductors, high-performance submicron processes and innovative RF design techniques it is possible to advance the integration level of superheterodyne receiver front-ends.

A first objective was to develop a monolithic filter for image rejection suitable for low power operation. A stable filter with very high Q was desirable. This was achieved with a monolithic LC series resonator. This original circuit is described in detail in chapter 3. The transfer function and the design methodology of the filter were developed as part of this work.

A second major objective was to demonstrate a first functional 1.9GHz integrated superheterodyne receiver front-end consisting of LNA, tunable image filter and mixer in one silicon die as discussed in section 1.5. Key objectives were to verify that the circuit was stable and that the proposed image filter provided substantial rejection. Furthermore, our efforts were aimed at the realization of a high quality receiver front-end with performance suitable to meet the GSM requirements. Thus, important goals became to obtain low noise figure and acceptable linearity.

For portable radios it is crucial to reduce power consumption. To this effect two additional receiver front-end versions were fabricated and fully characterized. This yielded useful knowledge on power consumption versus performance trade-offs.

Another important objective was to validate the transistor and inductor models and provide information on modelling and simulation limitations. To this effect, significant simulation and experimental work was conducted. The experimental work is also useful to uncover potential problems due to substrate coupling and packaging.

As part of the study a comparison of monolithic image rejecting front-ends was done. This shows the advantages of using tuned circuits implemented with monolithic LC resonators. At the end guidelines for the electronic tuning of the image filter are discussed.

Chapter 2 Image Rejection Methods

There are various methods to achieve image rejection using monolithic circuits. The most popular method is the image reject mixer which is reviewed in section 2.1 below. It is also possible to use a monolithic bandpass filter but performance limitations make this approach not very attractive as explained in section 2.2. Finally section 2.3 proposes the use of a notch filter which has advantages for low power monolithic implementation.

2.1 Image reject mixer

This is a well known method [22][23] which relies on phase cancellation. A block diagram of an image reject downconversion architecture is shown in Figure 2-1. To achieve the image rejection two mixers are required (usually Gilbert cells). Precise high frequency phase shifters for the local oscillator (at say 2.2GHz) are needed as well as phase shifters at the IF frequency (say, 300MHz) and an adder circuit, all of which increase the power consumption and the die area of this circuit.

In this approach the difficulty lies in realizing networks with accurate phase shifts as well as flat amplitude response. The advantage of the approach is that in principle the image reject filter is eliminated. In practice however, as will be shown in section 2.1.1, the obtained image rejection is not sufficient to meet the requirements of existing cellular standards and additional off-chip image rejection is still required. For example, a DECT receiver would require 80dB image rejection [5]. Assuming that a passive bandpass filter is installed before the LNA, providing 20 to 30dB image rejection, then approximately 50dB of on-chip image rejection would be required. Typically the best monolithic image reject downconverters have been offering rejections in the order of 30dB as will be shown in the following section. However a more recent image reject mixer part from Philips, designed for GSM operation, exhibits 38dB image rejection and is briefly described in the survey of the following section. This image reject mixer will be compared with the results of this work in Chapter 7.

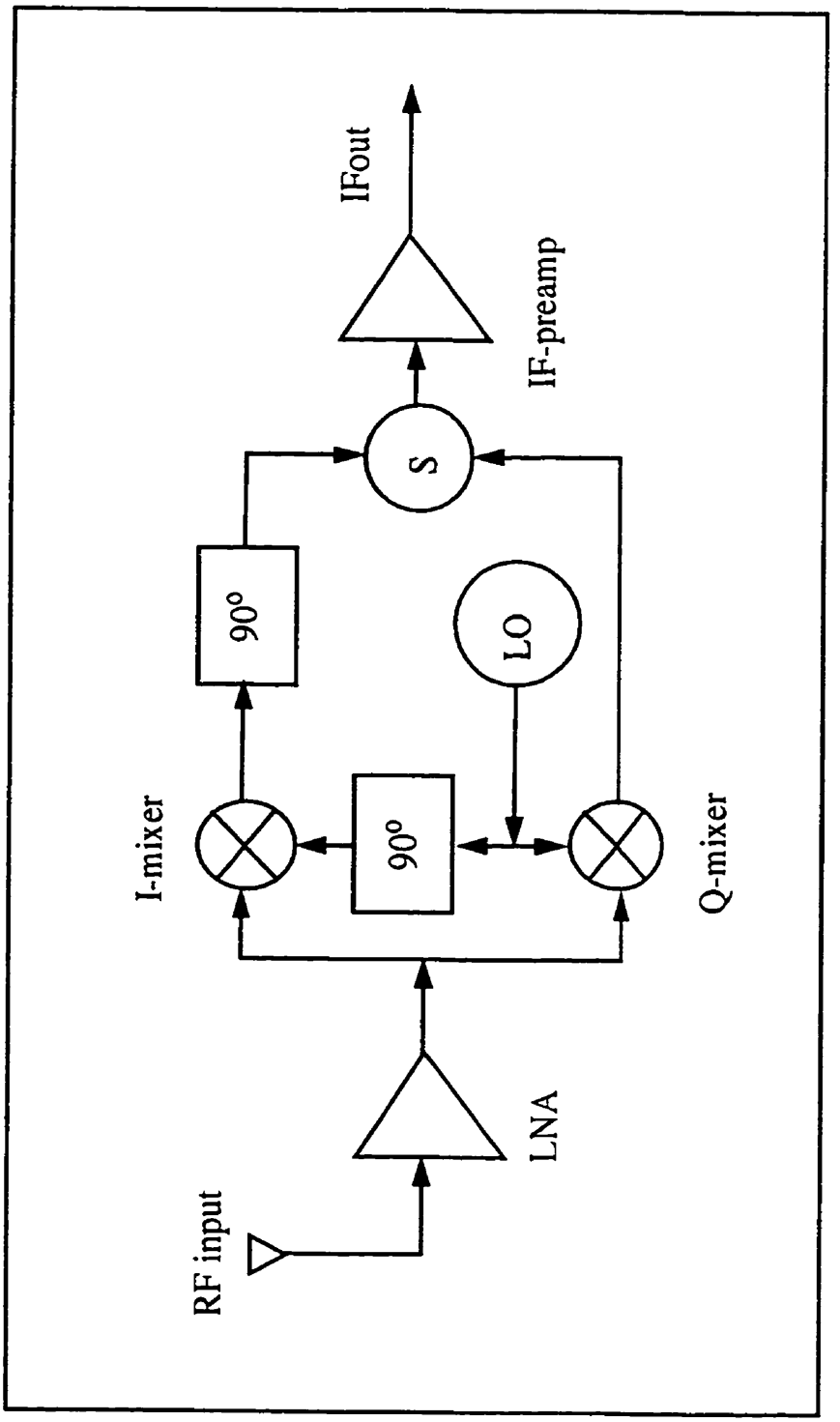

Figure 2-1: Image reject downconversion architecture

2.1.1 Survey of monolithic image reject downconverters

The integrated circuit implementations presented in Table 2-1 are image reject downconverters selected from the literature to illustrate the performance level of the state-of-the-art. They all use the conventional image-reject mixer approach with minor variations.

McDonald [24] developed a 2.5GHz BiCMOS Image Reject Front-End consisting of a low noise amplifier (LNA), an image-reject mixer, three phase-shifters (one for the LO and the other two for the IFs), and output, bias and power-down circuits. The LNA output directly drives the image-reject mixers. Phase-shift circuits are connected to the LO and to both mixer IF outputs. These +/-45° phase-shift circuits are implemented using RC/CR bridges for low-power consumption. The circuit was measured at DECT frequencies.

McDonald's BiCMOS chip clearly illustrates the complexity of the image reject mixer approach. The obtained 18dB noise figure is insufficient to meet the DECT specification. Perhaps this is due to lack of gain on the LNA, specially given the fact that the LNA is driving two Gilbert cell mixers which doubles the amount of noise that the LNA is supposed to suppress. The third order intercept point is -11.6dBm which is acceptable for DECT. However if the LNA gain was increased to improve the noise figure, then this would decrease the IP3 by approximately the amount of gain increase. Additionally the 14.1dB image rejection is rather poor, thus substantial off-chip filtering would be required to obtain acceptable image rejection on the receiver front-end.

Pache [25] presents a 2GHz BiCMOS image reject mixer integrated circuit. He points out that the cumulated amplitude errors due to the phase shifters make the image rejection greatly dependent on the LO frequency variation in the RF bandwidth, the IF adjustments and the process variation. To compensate for these errors Pache uses a gain control system in order to obtain higher image rejection, i.e. about 30dB rejection.

Pache's paper clearly describes how the phase shifters are the Achiles'heel of the image reject mixer. His work demonstrates that in order to obtain substantial image rejection an

Table 2-1: Comparison of existing image reject front-ends

Parameter	McDonald [24]]	Baumberger [26][27] (α)= unmatched	Pache [25]	Philips UAA2077 BM[28]
Supply Voltage	3V?	5V	3V	4V
RF frequency	2.5GHz	2.44GHz	2 GHz	2.0GHz
IF frequency	111MHz	130-260MHz	100-300MHz	118MHz
Conv.Gain (front-end)	7.6dB	34dB matched 21dB (α)	17 dB	20dB
Noise Figure	18dB	6.5dB matched 18dB (α)	N/A	4.3dBtyp (5dB max)
Input IP3 (front-end)	-11.6dBm	N/A matched -23dBm (α)	-15dBm	-17dBm
Image Rejection (mixer)	14.1dB	33dB	25-35dB	32dB
LO-RF isolation (front-end)	30dB	n/a	27dB	40dB
LO-IF isolation (front-end)	47dB	n/a	34dB	N/A
Current (front-end)	19.8mA	43mA	20 mA	27mA
Power consumption	59.4mW?	215mW	60mW	108mW
Chip Area	n/a	1.4x2.1mm^2	2x1mm^2	n/a
Technology	BiCMOS	GaAs	BiCMOS	BiCMOS
Presented at	ISSCC93	GaAs Symp 1993	CICC95	See Handbook [28]

additional control voltage (VCG) is required to tune out the errors due to LO, IF and process variation. He does not mention temperature variation effects.

Thanks to this tuning approach, Pache's chip exhibits a much better rejection than that of McDonald's who does not use any tuning (Pache's has 26dB rejection while MacDonald exhibits 14.1dB for the same IF of 111MHz). Surprisingly, Pache's paper does not state the noise figure of his integrated front-end receiver. Hence one could infer that Pache's noise figure is probably not very impressive.

Baumberger [26][27] presents a GaAs single chip image reject downconverter for the 2.44GHz band for licenseless operation. His chip comprises an RF preamplifier, a phasing type image reject mixer, an IF preamplifier, a two-stage ring-oscillator type VCO and a prescaler. He achieves a 33dB image rejection over a 130 to 260MHz IF bandwidth. The signal path consists of a single stage differential RF preamplifier, the two mixing channels followed by the RC allpass networks (IF Phase shifters) and their drivers.

Baumberger's circuit is also interesting in that he uses a differential LNA. He measures his circuit in two manners: first without input matching and second with a transformer at the input to symmetrize the single ended antenna signal and a symmetrical matching network. The noise figure of the broadband setup (single ended input, the other input terminated in 50 ohms) was 18dB (poor) with an input IP3 of -23dBm. However, in the tuned (matched) circuit the gain has been improved from 21dB to 34dB and the noise figure has been improved from 18dB to 6.5dB in a 100MHz bandwidth constrained only by the input matching network. Clearly, this 13dB increase in gain will also generate a degradation of the receiver IIP3 as the gain of the LNA has now been increased and the mixer receives signals which are 13dB larger. Unfortunately the IIP3 of the input matched circuit is not given. However since the input matching increases the gain by 13dB then it is to expect that the IIP3 will decrease by the same amount, i.e. from -23dBm to -36dBm. Thus it appears that Baumberger's matched circuit does not have sufficient linearity to be used either for DECT nor GSM.

A high performance part from Philips is the UAA2077BM which is a commercially available image rejecting front-end for DCS-1800 hand portable equipment or PCS

application [28]. This circuit contains a low noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert cell type whose internal architecture is fully differential. The local oscillator, shifted in phase to 45° and 135° mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and recombined internally to realize the image rejection.

This review indicates that with the image reject mixer approach an image rejection in the order of 30dB is typical. The best noise figure is 4.3dB (Philips) followed by 6.5dB from Baumberger's part which however has a much poorer IIP3 (-36dBm estimated by the author). As shown in Table 2-1 the Philips part UAA2077BM exhibits the best performance.

However, very recently Philips has added a new part UAA2077CM which exhibits a typical noise figure of 4dB, a -17dBm input IP3 with a 38dB image rejection which would then be the best in the market. Later, in chapter 7, the UAA2077CM part will be compared with the results of the present thesis.

Hence, it would be highly desirable that the monolithic receiver front-end explored in this thesis achieved a noise figure below 5dB, with an input IP3 of -17dBm or better, and an image rejection better than 50dB and with low power consumption consistent with portable radio applications. The realization of such a one-chip front-end is the topic of the present thesis.

2.2 Monolithic bandpass filter

Off-chip bandpass filters are routinely used for bandlimiting and image rejection. Typically, ceramic or SAW filters are connected before the LNA as well as between the LNA output and the mixer input. These filters provide excellent rejection but unfortunately are off-chip parts and usually require a 50 ohm matching network for optimum performance. Hence, a natural progression towards an integrated receiver would be to have monolithic bandpass filters.

Typically, monolithic bandpass filters are implemented using positive feedback so as to enhance the desired signal (at the center frequency) so in reality they are high Q tuned amplifiers. Since high Q is desired (for high selectivity) then strong positive feedback is needed and stability rapidly degrades. Hence only a moderate Q would be realizable. Also, as the positive feedback is increased (to enhance the Q) the linearity is automatically degraded. Finally the noise figure is also excessive.

For example a recently reported 1.8GHz monolithic bandpass filter [29] exhibits a noise floor of -138dBm/Hz (input referred) which corresponds to a 32dB NF. This noise figure is unacceptably high to use such a filter for image rejection in a front-end receiver. The measured input IP3 was -16dBm but with a Q of only 35. Again this linearity is not sufficient for a front-end because the filter would be preceded with an LNA with, say, at least 10dB gain, thus now the IP3 at the LNA input would be approximately -26dBm and this would be rather poor.

In another effort, Duncan [30] shows that there is an inverse relation between Q and linearity which is a major limitation in the performance of a monolithic bandpass filter.

Thus, at this time an on-chip bandpass filter with adequate performance to be used on a receiver front-end for cellular application has not been demonstrated.

2.3 Notch filter

An alternative to the ubiquitous bandpass filter approach is to instead use a bandreject or notch filter to suppress the undesired image [31]. This approach is promising for monolithic integration as will be shown in this work because very high Qs can be obtained without stability problems while achieving low power operation.

As will be shown in Chapter 3 the proposed notch filter is simple, making it attractive for low power operation. It uses a monolithic inductor to implement an LC series resonator whose Q is enhanced with negative resistance. The obtained rejection is very high. As will be shown, the circuit requires Q tuning as well as frequency tuning. The frequency tuning is required to center the filter and to compensate for process variations. The Q

tuning is required to provide sufficient negative resistance to obtain a deep notch. The circuit will be explained at length in Chapter 3.

2.4 Monolithic transceivers with off-chip image filtering

This section presents a brief review of existing transceiver ICs in GaAs and BiCMOS technologies. The performance of these transceivers is an indication of the state-of-the-art in current receiver technology. In these chips the receiver front-end consists of an LNA and a mixer, with an intervening off-chip image filter; thus these transceivers are not fully monolithic. The off-chip filter is usually a passive surface acoustic wave (SAW) or ceramic filter and usually exhibits 3dB loss (its noise figure is therefore 3dB). Hence the image filter degrades the receiver noise figure and decreases the gain.

Table 2-2 compiles data on the LNAs which form part of the transceiver ICs reviewed in this section. The overall noise figure of the receiver front-end can be easily obtained with the well known Friis formula for cascaded stages [2]. Similarly the linearity for the cascaded devices can be obtained by appropriately combining the linearity of the various stages [2].

This review is also useful to observe the topologies currently in use for high performance transceivers. As Table 2-2 shows GaAs designs exhibit the best results (lowest noise figure), however Long's BiCMOS LNA has a noise figure comparable to Devlin's design while consuming much less power. Similarly Long's LNA consumes less power than Kazuya's LNA. This clearly indicates that, at least for 1.9GHz operation, silicon is becoming very competitive.

A true comparison is difficult because all these LNAs use different technologies and different current and supply voltages.

However, in the following sections we will discuss these LNAs individually.

Table 2-2: LNAs used on transceiver ICs

Author:	Kazuya[32]	Titus[33]	Devlin[34]	Long [35]
Application	1.9GHz PHS	1.9GHz	2.4GHz ISM	1.9GHz
Supply voltage	3.4V	5V	5V	1.9V
Supply current	6.1mA	32mA	6mA	2mA
Supply power	20.7mW	160mW	30mW	3.8mW
Gain	7.4dB (LNA)	15.5dB	17.5dB	9.5dB
Noise Figure	1.7dB	5.0dB (diplexer +LNA)	2.5dB	2.8dB
IP3 (input)				-3dBm
Technology	GaAs	BiCMOS	GaAs	BiCMOS
Presented at	ISSCC96	1996 Mwave Sympo-sium	1993 Mwave-Symposium	JSSC, Dec.95

2.4.2 The Kazuya GaAs transceiver IC

Kazuya et al. [32] designed a 3.4V single power supply GaAs single chip RF transceiver IC for 1.9GHz digital mobile communications such as the Japanese Personal Handy Phone System (PHS). The analog circuits contain a power amplifier, an SPDT switch, two attenuators for transmitting and receiving modes, and a low-noise amplifier. The chip does not contain a mixer and no mention is made to the image rejection strategy, hence one assumes that an off-chip filter would be used.

Kazuya's LNA is illustrative of the state-of-the art; his 1.7dB noise figure is the best one found in this survey. Unfortunately, no details of the LNA topology are provided in the

paper. However, observing the micrograph one can see that the LNA contains an on-chip inductor.

2.4.3 The Titus BiCMOS transceiver front-end

Titus [33] designed a silicon BiCMOS transceiver front-end. This process has NPN devices with 12GHz f_T. Titus's LNA has a single ended input and a differential output to drive a balanced mixer. Titus omits to say what kind of image reject filter he would use in his receiver. A series feedback inductor is used to transform the input impedance close to the noise match. He does not state whether this inductor is on-chip, but one assumes so.

The LNA current consumption is high, probably to obtain high gain (two LNA stages are used) and high linearity. Unfortunately the LNA input IP3 is not given. His work is interesting in that he integrates an SPDT switch in front of the LNA. His measurements include the diplexer switch and the LNA together. He obtains 15dB gain and 5dB noise figure at 1.9GHz.

To complete the receiver front-end, the LNA output would normally be connected to an off-chip image filter whose output would then be connected back to a silicon mixer. Thus, one must add the noise contribution of the image filter and the mixer. For example, if a filter with 3dB loss and a mixer with 10dB noise figure are assumed, then the noise figure would increase to 5.75dB (from antenna to first IF).

However in this work the bandpass filter which is usually placed between the diplexer switch and the LNA is missing, thus this receiver will probably have insufficient image rejection for a cellular application. If such a filter (with 3dB loss) was added then the noise figure of the overall receiver front-end would increase to 8.75dB.

An important piece of information from Titus's work is the measured insertion loss of his BiCMOS SPDT. It is 1.3dB at 1GHz and degrades to approximately 1.8dB at 1.9GHz. Hence, at 1.9GHz the switch is contributing with 1.8dB noise figure and therefore the LNA is contributing with the remaining 3.2dB noise figure (calculated by the author using Friis formula) for a total of 5dB measured noise figure. This shows that the BiCMOS switches need improvement to achieve very low noise receivers.

2.4.4 The Devlin 2.4GHz single chip transceiver

Devlin [34] presents a single chip GaAs transceiver. His paper describes a transmit/receive front-end for a 2.4GHz wireless communications transceiver. In receive mode the RF input signals are downconverted to differential IF signals. Typical power requirement on receive mode is 30mA from the +5V supply.

The LNA is a two stage design implemented with FETs with series inductive feedback. The LNA gain is 17.5dB+/- 0.5dB from 2-3GHz and its measured noise figure is 2.5dB at 2.5GHz. An external bandpass filter located before the LNA is used for image rejection and the LNA output is directly connected to the mixer input (no filter between LNA and mixer). Since in this architecture all the image rejection is provided by the filter placed before the LNA, the image rejection will be insufficient for a cellular application.

Devlin presents a plot which shows the measured receiver gain and DSB noise figure versus IF frequency. For a 300MHz IF the receiver gain is 13.6dB and the noise figure 4.2dB DSB. Devlin does not indicate whether he included the external image reject filter to do this measurement. However, since his receiver contains a Diversity switch and a T/R switch in front of the LNA for a total of 1.4dB loss due to both switches (0.7dB each switch) and the LNA has 2.5dB noise figure at 2.4GHz and is directly connected to the mixer it is obvious that the external filter was not included.

Thus it appears that 4.2dB represents the DSB noise figure of the receiver front-end with no image rejection and if an image reject filter (with 3dB loss) was included, then the overall receiver measured NF would have been approximately 7.2dB with a limited amount of image rejection (probably 30 to 40dB) probably insufficient for a cellular application.

2.4.5 The Long 1.9GHz narrowband radio receiver front-end

Long [5][35] presents a silicon LNA which uses a transformer to obtain very good linearity while preserving low noise. This is a very interesting design which could be used in a more advanced version of the monolithic receiver front-end proposed in this thesis. Careful redesign would be required to tailor Long's design to the monolithic receiver application. For example Long's LNA was designed for a 50 Ohm load, however for an integrated

version with on-chip image filtering the LNA does not have to drive an external 50 Ohm load, instead it would drive a higher impedance load, in the order of 300 Ohms.

It is informative to calculate the budget for a receiver front-end using Long's design results [5]. In this case the receiver front-end would consist of a monolithic LNA followed by an off-chip image reject filter which is then connected to Long's monolithic transformer coupled balanced mixer. The results are shown in Table 2-3. These results indicate the performance achievable using a conventional off-chip filter for image rejection. Note that the image filter linearity is typically very high, which is advantageous.

Table 2-3: 0.8 micron BiCMOS receiver front-end with off-chip image filter following Long's results

Parameter	LNA	Image filter (passive)	Mixer	Total
Gain	9.5dB	-3dB	6.1dB	12.6dB
NF	2.8dB	3dB	10.9dB (SSB)	4.3dB
IP3 (input)	-3dBm	>>0dBm	+2.3dBm	-4.2dBm
Supply voltage	1.9V	n/a	1.9V	1.9V
Supply current	2.0mA	n/a	2.5mA	4.5mA
Power	3.8mW	n/a	4.75mW	8.55mW

In Table 2-3 the total NF for a receiver following Long's results was calculated using Friis formula (1.3), and the input IP3 was estimated assuming that the off chip image reject filter has ideal linearity; hence this is an slightly optimistic estimate. Observe that due to the 3dB filter loss the total gain in front of the mixer is only 6.5dB and for this reason the overall 4.3dB noise figure is 1.5dB higher than the LNA noise figure. On the other hand,

due to the low gain the signals in front of the mixer are not too large and the overall linearity is very good

To obtain the performance of a completed receiver front-end one would have to add the contribution of a diplexer (which is placed right after the antenna and can be assumed to have 1dB loss) and a bandpass filter before the LNA (typically a ceramic filter with 3dB loss). In this case the overall noise figure for Long's receiver front-end (from the antenna to the first IF) would be 8.3dB. The noise introduced by the IF processing stage would degrade this noise figure a little more, in the order of 0.5dB or so. Clearly this performance is sufficient to meet DECT specification and comes very close to meeting the GSM requirements.

The performance shown in Table 2-3 would be desirable in a monolithic receiver front-end consisting of LNA, image filter and mixer in one chip. To answer whether this is achievable or not is one purpose of the present investigation.

Chapter 3 Theory and design of a notch filter

In this section we begin by introducing the principle of operation of the notch filter used in this work and then follow up with the realization of a basic notch filter. The filter transfer function for the basic notch filter is then derived. Finally, the basic notch filter is combined with a bandpass amplifier to obtain a completed design suitable for image rejection in a superheterodyne receiver front-end for portable radio.

3.1 Notch filter principle of operation

Consider the block diagram shown in Fig.3-1 below. The forward loop gain is 1 while the closed loop gain is *B(s)*. In this case the closed loop transfer function is given by:

$$\frac{Vout}{Vin} = \frac{1}{1 + B(s)} \tag{3.1}$$

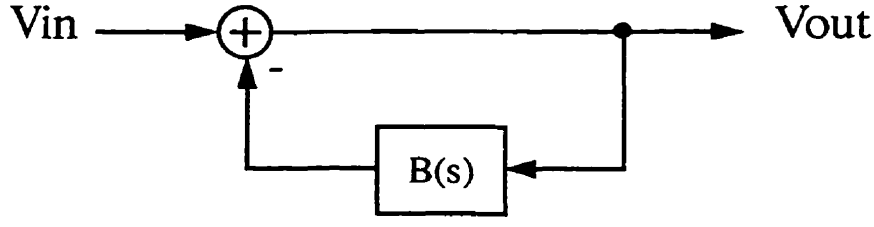

Figure 3-1: Closed loop block diagram

Clearly the frequency response of *B*(s) defines the closed loop behaviour. Assume now that *B*(s) has a second order bandpass characteristic, as follows:

$$B(s) = \frac{G_{BP} \cdot \frac{\omega_0}{Q} \cdot s}{s^2 + s \cdot \frac{\omega_0}{Q} + \omega_0^2} \tag{3.2}$$

Replacing this expression in equation (3.1) yields:

$$H(s) = \frac{Vout}{Vin} = \frac{s^2 + s \cdot \frac{\omega_0}{Q} + \omega_0^2}{s^2 + s \cdot \frac{\omega_0}{Q} \cdot (1 + G_{BP}) + \omega_0^2} \tag{3.3}$$

This expression exhibits a pair of complex zeros located at a frequency of ω_0 and with a quality factor given by Q. These zeros create a notch (at ω_0) in the frequency response and thus a notch filter has been obtained. This shows that by inserting a bandpass response (B(s)) in the feedback path of the closed loop shown in Fig.3-1 a pair of complex zeros has been realized. Note that these zeros originate from the poles of the resonator B(s), thus the zeros of H(s) will resonate at the same frequency (ω_0) as the poles of B(s), and have the same Q. This demonstrates that it is sufficient (barring stability issues) to have a second order resonator, be it bandpass, lowpass or all pass, in the feedback loop to synthesize a pair of complex zeroes in the closed loop response. The denominator of (3.3) shows a pair of poles also at frequency ω_0, in this case however the pole quality factor has been reduced by $(1+G_{BP})$. Thus the higher the gain of the bandpass filter B(s) on the feedback loop the lower the Q of the poles and the more stable the closed loop circuit.

Note that the starting Q of the poles of the bandpass filter B(s) could even be negative, i.e. B(s) could be an oscillator (open loop). Closing the loop removes the stability problem associated with operating B(s) near the onset of oscillation.

At resonance (ω_0) the above expression (3.3) reduces simply to the following:

$$H(s)_{\omega = \omega_o} = \frac{Vout}{Vin} = \frac{s \cdot \frac{\omega_0}{Q}}{s \cdot \frac{\omega_0}{Q} \cdot (1 + G_{BP})} = \frac{1}{1 + G_{BP}} \tag{3.4}$$

It is important to observe that if G_{BP} is much larger than 1 the above expression will yield a very small value, thus deeply notching the input signal. Hence it is useful to have a resonator B(s) with high gain. Observe also that in expression (3.4) the Q term does not appear, hence, even with a relatively low Q bandpass filter on the feedback loop it is possible to realize a very deep notch (i.e. a notch with very high Q), provided the bandpass

filter has large passband gain. However, a relatively low Q would translate to a relatively wide notch and hence difficulty in achieving high gain away from the notch, i.e. at the desired RF frequency.

In this work a 1.9GHz superheterodyne radio receiver is being addressed, with 2.2GHz local oscillator and 300MHz IF, hence the undesired image frequency is located at 2.5GHz and to suppress this image a 2.5GHz notch filter is proposed. Based on the above theory a 2.5GHz notch filter can be realized with the block diagram shown in Fig 3-2 below. Clearly by having a bandpass filter tuned to 2.5GHz in the feedback path a 2.5GHz notch filter is realized. In this case the notch filter function is to pass the desired RF (1.9GHz) while suppressing the undesired image (2.5GHz).

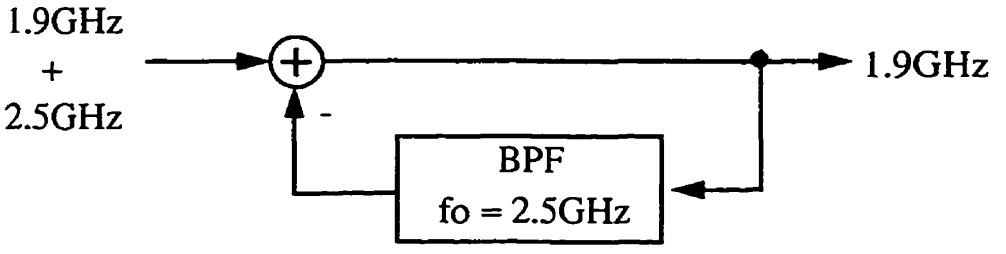

Figure 3-2: A 2.5GHz notch filter block diagram

To implement the notch filter shown in Fig.3-2 a summer node and a resonator circuit (tuned for 2.5GHz) in the feedback loop are needed. These circuits are described in the next section.

3.2 Design of an LC notch filter for image rejection

A circuit to demonstrate the notch filter technique proposed in the previous section is presented here. A superheterodyne receiver with 1.9GHz RF frequency, 2.2GHz L.O. and 300MHz IF is assumed. The unwanted image would then be located at 2.5GHz. As shown in section 3.1, to implement the notch filter a resonator is needed. A monolithic series LC resonator was found to be useful for this purpose and is described in section 3.2.1 below. Then this resonator is used in a closed loop to complete the desired notch filter.

3.2.1 A monolithic LC resonator

Consider the series resonator shown in Figure 3-3. It consists of an on-chip inductor (L) in series with the base of an emitter follower (Q_{ef}) whose emitter is loaded with a capacitor (C_{load}). The transistor is biased by means of the ideal DC current source I_1. The monolithic inductor is represented by an ideal inductor (L) in series with a resistor (R_{ind}) to account for the finite inductor Q, which typically is in the order of 6 for silicon inductors in a sub-micron bipolar process.

The emitter follower loaded with a capacitor behaves as a negative resistance generator and if a resonant circuit can be formed by parasitics or other elements, in this case the on-chip inductor, then the amplifier becomes an oscillator [36]. Thus, this series LC resonator can be seen as a version of a common collector Colpitts oscillator, that is a feedback oscillator using a capacitive voltage divider. However, for the notch filter application intended here, the oscillation will be quenched, that is the circuit will be connected so as to prevent oscillation as will be shown.

The series resonator small-signal equivalent circuit is shown in Fig. 3-4 using the transistor hybrid-π model [37]. A load resistor R_o is assumed for completeness and the Miller capacitance is not included for simplicity (this is a reasonable simplification since, as will be seen later, the collector of Q_{ef} will be connected to the emitter of a cascode transistor).

From Figure 3-4 the input voltage is given by:

$$v_{in} = i_b \cdot (R_{ind} + j\omega \cdot L + r_{bb'} + Z_\pi) + v_e \tag{3.5}$$

where R_{ind} represents the inductor losses, $r_{bb'}$ is the base resistance of transistor Q_{ef} which depends on the transistor size and technology and Z_π is given by:

$$Z_\pi = \frac{r_\pi \cdot \frac{1}{j\omega \cdot C_\pi}}{r_\pi + \frac{1}{j\omega \cdot C_\pi}} = \frac{r_\pi}{j\omega \cdot C_\pi \cdot r_\pi + 1} \tag{3.6}$$

where C_π is the emitter-base capacitance of transistor Q_{ef}.

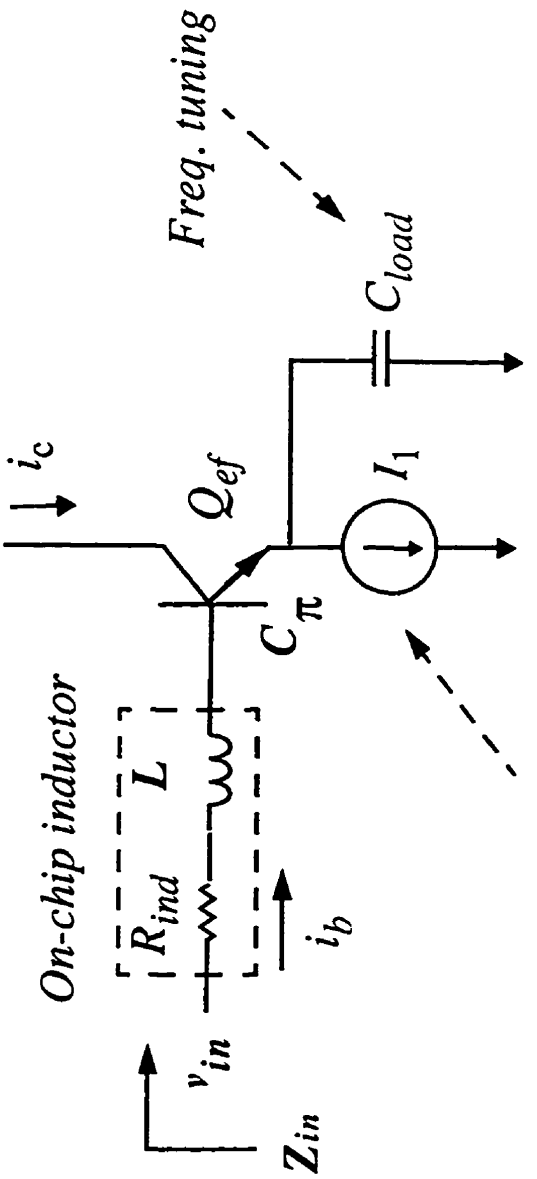

Figure 3-3: A series LC resonator

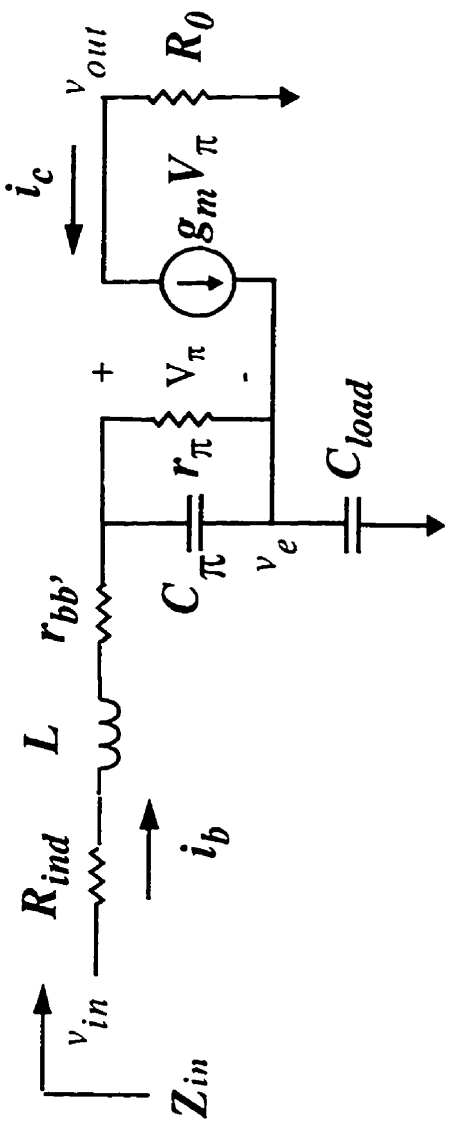

Figure 3-4: Small-signal equivalent circuit for the series LC resonator

In Figure 3-4 the emitter voltage (v_e) can be expressed as:

$$v_e = (i_b + i_c) \cdot \frac{1}{j\omega \cdot C_{load}} = (i_b + g_m \cdot v_\pi) \cdot \frac{1}{j\omega \cdot C_{load}} \tag{3.7}$$

where g_m is the transconductance of Q_{ef} which depends on the DC bias current (I_1) of the transistor. Expressing now v_π as the product of i_b and Z_π yields:

$$v_e = (i_b + g_m \cdot i_b \cdot Z_\pi) \cdot \frac{1}{j\omega \cdot C_{load}} = i_b \cdot (1 + g_m \cdot Z_\pi) \cdot \frac{1}{j\omega \cdot C_{load}} \tag{3.8}$$

Before continuing, let us look at the transistor high frequency small-signal current gain (β) which can be expressed as follows [37]:

$$\beta(j\omega) = \frac{\beta_0}{1 + j\frac{\omega}{\omega_T} \cdot \beta_0} = \frac{\beta_0}{1 + j\frac{\omega}{\omega_\beta}} \tag{3.9}$$

where β_o is the low frequency current gain and the -3dB point cut-off frequency (ω_β) is defined as:

$$\omega_\beta = \frac{\omega_T}{\beta_0} \tag{3.10}$$

Based on the above equation (3.9) Figure 3-5 below shows the magnitude of the current gain as a function of frequency. It can be seen that beyond the cut-off frequency (ω_β) the current gain (β) reduces with a slope of -6dB/octave.

Equation (3.6) is directly related to the above current gain as follows:

$$Z_\pi = \frac{\beta_0 / g_m}{1 + j\omega \cdot C_\pi \cdot \frac{\beta_0}{g_m}} = \frac{\beta_0 / g_m}{1 + j\frac{\omega}{\omega_\beta}} = \frac{r_\pi}{1 + j\frac{\omega}{\omega_\beta}} \tag{3.11}$$

Equation (3.11) shows that at frequencies well below the cut-off frequency (ω_β) Z_π is simply equal to r_π. At moderate frequencies (not much higher than the cutoff frequency), Z_π would have both a resistive and a capacitive component. On the other hand at very high

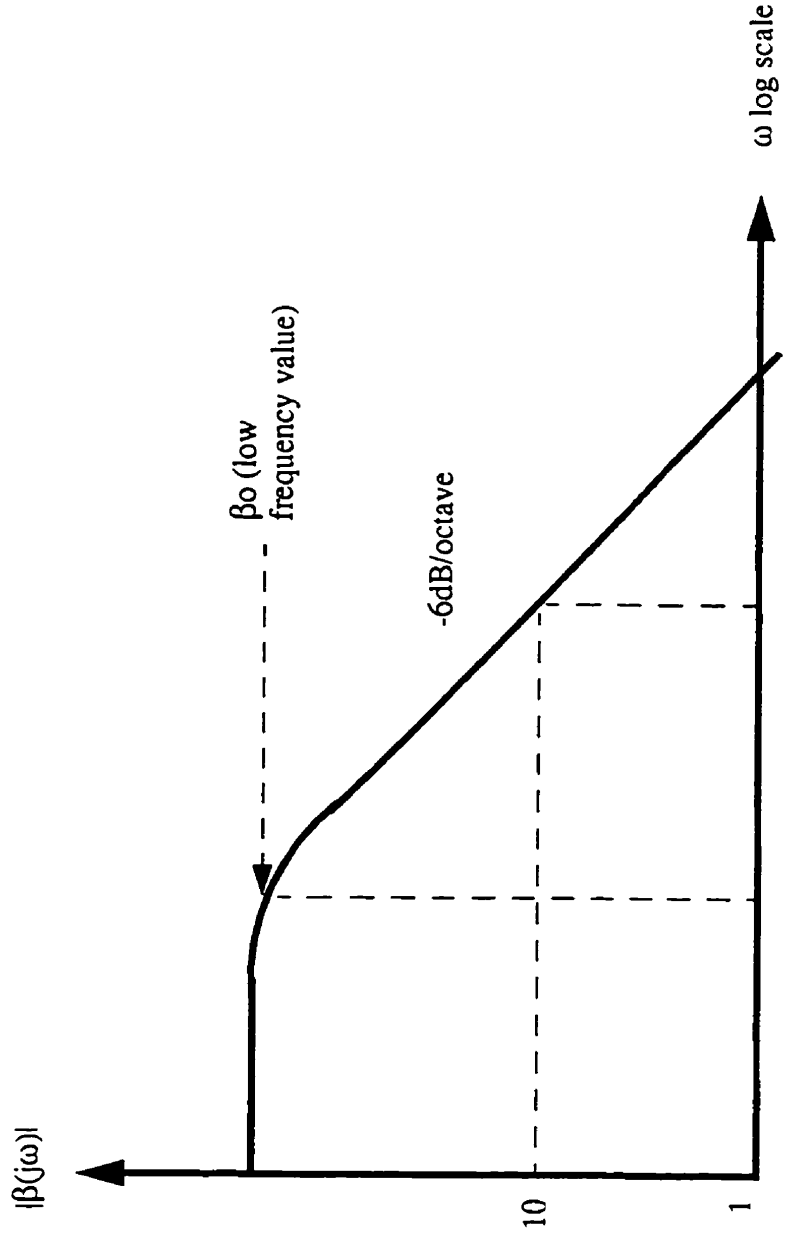

Figure 3-5: Small-signal AC current gain

frequencies (say at least 10 times higher than the cutoff frequency) the imaginary part of the denominator of equation (3.11) is dominant and Z_π can be approximated as follows:

$$Z_\pi = \frac{r_\pi}{j\frac{\omega}{\omega_\beta}} = \frac{r_\pi}{j\omega} \cdot \frac{\omega_T}{\beta_0} = \frac{1}{j\omega \cdot C_\pi} \tag{3.12}$$

This equation indicates that when operating the resonator well beyond the transistor cut-off frequency r_π is negligible and Z_π becomes a pure capacitance which is useful to generate negative resistance as will be shown below.

For the 0.5 micron bipolar process used in this work, the transit frequency will typically be in the order of 10 to 20GHz (depending on the transistor DC bias current) while β_o is in the order of 70 to 80. Hence according to (3.10) the cut-off frequency (ω_β) will be on the order of a couple of hundred MHz. For the present work, the desired frequency of operation for the series resonator is 2.5GHz (the image frequency). This frequency of operation is therefore approximately 10 times the cut-off frequency ω_β and equation (3.12) applies.

Observe that if the frequency of operation was higher than 2.5GHz or the transit frequency was reduced (say by reducing the bias current or by adding an external capacitor connected in parallel with the base emitter junction as will be done in chapter 4) equation (3.12) would still be valid because in both cases the frequency of operation would then be larger than 10 times the cutoff frequency ω_β. For example, if the transit frequency was reduced to 2.5GHz then the current gain cutoff frequency would be approximately 31MHz (as per equation (3.10)), and therefore the frequency of operation (2.5GHz) is now much larger than the cutoff frequency (31MHz) and equation (3.12) still applies.

To continue the analysis, replace expression (3.12) in equation (3.8) above to obtain:

$$v_e = i_b \cdot \left(1 + g_m \cdot \frac{1}{j\omega \cdot C_\pi}\right) \cdot \frac{1}{j\omega \cdot C_{load}} = i_b \cdot \left(\frac{1}{j\omega \cdot C_{load}} + g_m \cdot \frac{1}{(j\omega)^2 \cdot C_\pi \cdot C_{load}}\right) \tag{3.13}$$

Now inserting the above expression in equation (3.5) yields the complete expression for the input voltage:

$$v_{in} = i_b \cdot \left(R_{ind} + j\omega \cdot L + r_{bb'} + Z_\pi + \frac{1}{j\omega \cdot C_{load}} + g_m \cdot \frac{1}{(j\omega)^2 \cdot C_\pi \cdot C_{load}} \right) \quad (3.14)$$

The complete input impedance Z_{in} of the series resonator is then given by:

$$Z_{in} = \frac{v_{in}}{i_b} = R_{ind} + j\omega \cdot L + r_{bb'} + Z_\pi + \frac{1}{j\omega \cdot C_{load}} + g_m \cdot \frac{1}{(j\omega)^2 \cdot C_\pi \cdot C_{load}} \quad (3.15)$$

Observe in the right-hand side of this equation the term which has $(j\omega)^2$ on its denominator, this term represents a negative resistance which is useful for this work as it allows to cancel the on-chip inductor losses. This term is negative because both Z_π (as in equation (3.12)) and the load (C_{load}) are capacitive. Observe that this term does not directly depend on ω_T and therefore it is possible to generate negative resistance at operating frequencies equal or beyond the transit frequency.

Hence, in the series resonator circuit the capacitive load is multiplied by $-j$ or "rotated" by -90° to become a negative resistance when looking into the base of transistor Q_{ef}. A resistive load would have become capacitive while an inductive load would have become resistive. Thus the circuit is acting as a -90° gyrator, as illustrated in Figure 3-6, which is valid only for operation well beyond ω_β.

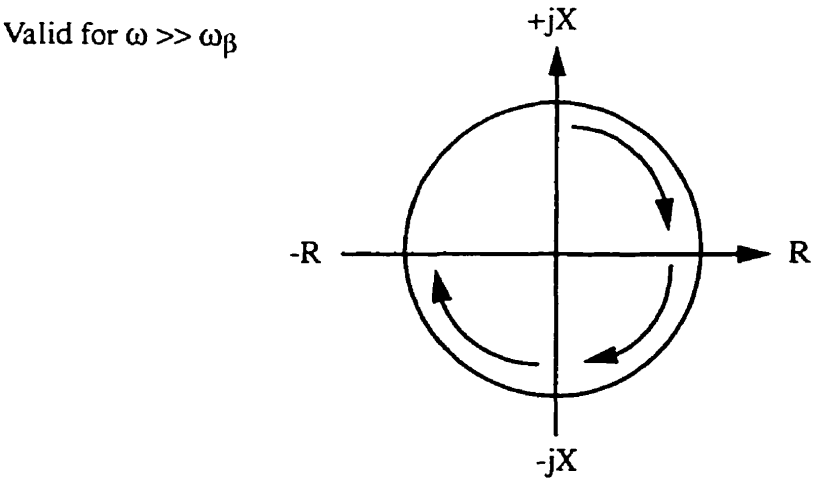

Figure 3-6: Emitter load impedance transformation for the emitter follower of the series resonator. The beginning of the arrow indicates the emitter load impedance and the end of the arrow indicates the corresponding input impedance seen at the base of Q_{ef}.

Now replacing j^2 with -1, replacing Z_π with expression (3.12) and rearranging equation (3.15) yields the final expression for the input impedance:

$$Z_{in} = j\omega \cdot L + \frac{1}{j\omega \cdot C_\pi} + \frac{1}{j\omega \cdot C_{load}} + R_{ind} + r_{bb'} - \frac{g_m}{\omega^2 \cdot C_\pi \cdot C_{load}} \qquad (3.16)$$

The negative resistance component in the right hand side of equation (3.16) is confirmed by Vendelin [36]. This negative resistance varies inversely with the square of the frequency and is proportional to g_m. Thus by adjusting g_m by means of the DC bias current I_1 (see figure 3-3), sufficient negative resistance can be generated to cancel the losses of the monolithic inductor (R_{ind}) and the intrinsic base resistance of Q_{ef} ($r_{bb'}$). This results in a dramatic increase in the effective inductor quality factor Q to very high values. For example for the 0.5micron bipolar process used in this work, the monolithic inductor by itself has a Q of approximately 6 at 2GHz; the exact value will depend on the geometry of the inductor. The effective Q, on the other hand, can approach infinity, depending on the precision of tuning.

Clearly, there is an LC series resonator formed by L, C_π and C_{load} with resonant frequency (ω_o) given by the following formula:

$$\omega_o = \frac{1}{\sqrt{L \cdot C_s}} \tag{3.17}$$

where C_s represents the series combination of C_π and C_{load} and is calculated as follows:

$$C_s = \frac{C_\pi \cdot C_{load}}{C_\pi + C_{load}} \tag{3.18}$$

Observe that by varying C_{load} or C_π the frequency of resonance (ω_0) can be adjusted (in a monolithic context the inductor is of fixed value and cannot be adjusted to tune the frequency).

For simplicity let us now express the input impedance in the Laplace domain:

$$Z_{in} = s \cdot L + \frac{1}{s \cdot C_s} + R + \frac{g_m}{s^2 \cdot C_\pi \cdot C_{load}} \tag{3.19}$$

where R represents the total losses due to the inductor series resistance and the transistor Q_{ef} base resistance and is given by:

$$R = R_{ind} + r_{bb'} \tag{3.20}$$

From equation (3.19) the corresponding admittance is given by:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{s \cdot C_s}{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \frac{g_m}{s^2 \cdot C_\pi \cdot C_{load}} \right) + 1} \tag{3.21}$$

Clearly, this admittance exhibits a bandpass frequency response with a pair of complex poles at the frequency ω_0 which was defined in equation (3.17) above. Observe that depending on the value of g_m in the denominator of the above expression the pair of complex poles can be placed in the right or left side of the s-domain plane. Thus the series resonator can oscillate if sufficient negative resistance is generated by the transistor.

3.2.2 Realization of a basic notch filter

The series resonator of Figure 3-3 is now used in a current adder circuit to obtain the basic notch circuit shown in Fig.3-7, in which the resonator transistor is now Q_2. The input voltage is converted into a current (i_{c1}) by the input stage (Q_1) and current i_{c1} can be treated as the input current. Node A acts as a current summing node and current i_3 can be considered as the circuit output variable. Current i_{s2} is the series resonator input current which is generated by the voltage v_3 in Fig. 3-7.

Applying Kirchoff's current law to the summing node A with the currents in the directions shown in Figure 3-7 we have:

$$i_3 = i_{c1} - i_{s2} \tag{3.22}$$

Assuming that Z_3 is resistive, then i_{c1} as drawn in the schematic is in phase with v_3, that is when i_{c1} increases so does v_3. Also at resonance, the series resonator input impedance is resistive and small, hence i_{s2} is large and in phase with v_3. Thus at resonance, i_{c1} and i_{s2} are in phase, that is while i_{c1} is entering node A, i_{s2} is leaving the same node. Now, if Q_2 is tuned to minimize the series resonator input impedance, then i_{s2} can be made almost identical to i_{c1} and according to equation (3.22) i_3 would then be very small. Thus there is no output current (i_3) and the notching action has occurred.

To analyze the circuit, Figure 3-8 shows a block diagram representation of node A based on the previous nodal equation (3.22). This representation is artificial in that the loop of Fig. 3-8 is not evident in a circuit sense in Fig. 3-7. However, it is mathematically correct and it allows association with the block diagram of Fig. 3-2. It also allows to easily derive the circuit transfer function as will be shown.

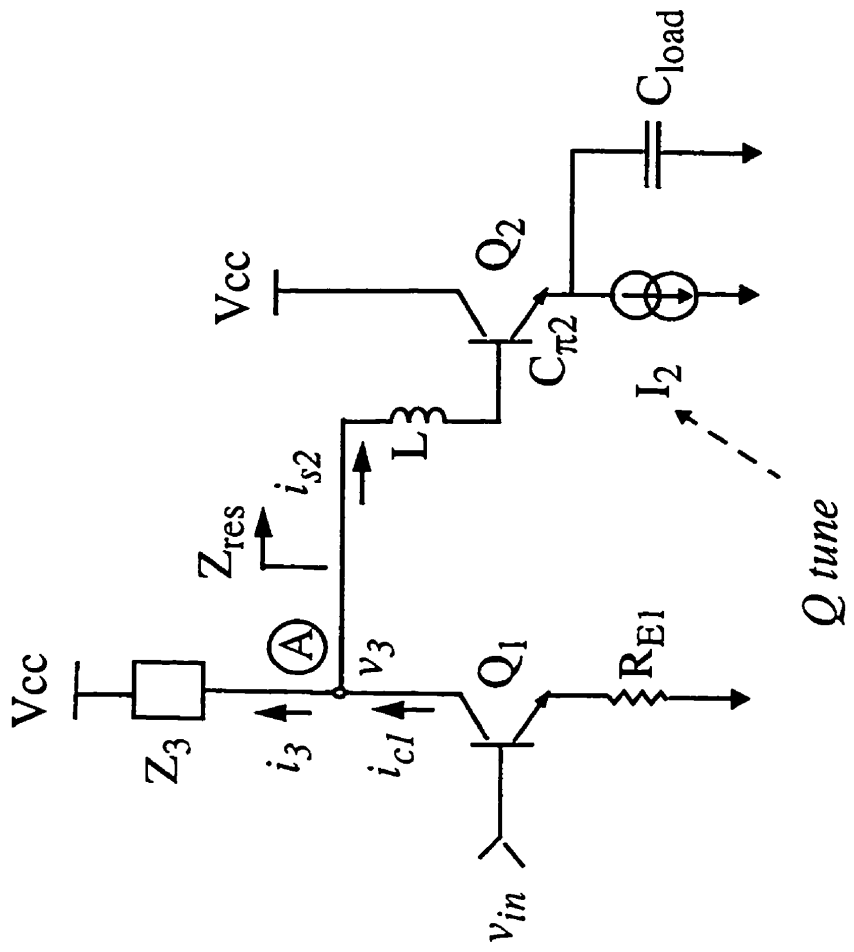

Figure 3-7: A basic notch filter

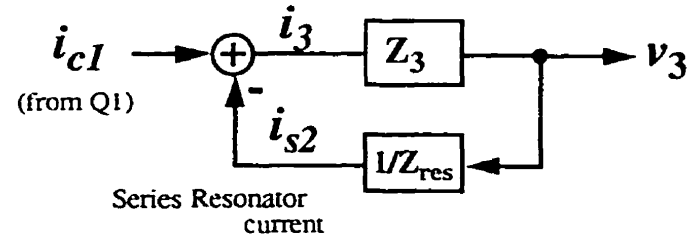

Figure 3-8: Block diagram of basic notch filter

In this diagram Z_{res} is the series resonator input impedance (formula (3.19)) as indicated in Figure 3-7 and v_3 is the voltage at node A. For simplicity the previous diagram can be redrawn as shown below where the output variable is i_3.

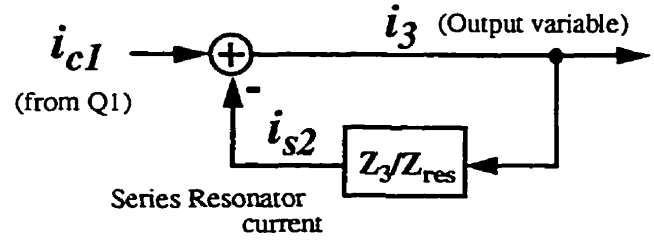

Figure 3-9: Compact block diagram of basic notch filter

Observe that this block diagram is precisely the desired one to realize the notch filter (compare with Fig.3-2 in section 3.1). The feedback transfer function (Z_3/Z_{res}) has precisely a bandpass characteristic (see equation (3.21)) which resonates at frequency ω_o, which we can now refer to as the notch frequency. In this diagram the loop gain is given by Z_3/Z_{res}. The relative phases and magnitudes of Z_3 and Z_{res} then become important for stability. From the block diagram of Figure 3-9 the following transfer function is readily obtained:

$$\frac{i_3}{i_{c1}} = \frac{1}{1 + \frac{Z_3}{Z_{res}}} \tag{3.23}$$

This expression clearly shows that away from the series resonant frequency (or when the notch circuit is turned off by turning Q_2 off) Z_{res} is very large and the right hand side of equation (3.23) reduces to 1 and i_3 is simply equal to i_{cl} as expected (bandpass action). On the other hand when transistor Q_2 is turned on and the resonator enabled, Z_{res} will be very small at the resonance frequency (ω_o) and the right hand side of equation (3.23) approaches zero, hence i_3 becomes very small and there is no output (the notch action).

Replacing the expression for the series resonator admittance (equation (3.21)) in (3.23) above yields the basic notch filter transfer function:

$$\frac{i_3}{i_{c1}} = \frac{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \dfrac{g_{m2}}{s^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \dfrac{g_{m2}}{s^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + Z_3 \cdot s \cdot C_s + 1} \tag{3.24}$$

Now back to the frequency domain for an explicit view of the negative resistance terms:

$$\frac{i_3}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + Z_3 \cdot j\omega \cdot C_s + 1} \tag{3.25}$$

This formula clearly shows a pair of complex zeroes in the numerator with resonant frequency (ω_z) given by:

$$\omega_z = \frac{1}{\sqrt{L \cdot C_s}} \tag{3.26}$$

The Q of the numerator can be made infinite by adjusting the negative resistance term to completely cancel the resistive term R and obtain a very deep notch in the frequency response. Hence, during normal operation the filter is tuned by adjusting I_2 in the circuit of Figure 3-7 in order to adjust g_{m2} so that at the zero frequency of resonance (ω_z) the term in brackets in the numerator of equation (3.25) cancels. Hence, g_{m2} is adjusted to comply with the following equation:

$$R = \frac{g_{m2}}{\omega_z^2 \cdot C_{\pi 2} \cdot C_{load}} \tag{3.27}$$

Observe now the denominator of equation (3.25) which exhibits a pair of complex poles which we will refer to as spurious poles to differentiate them from desired poles at the RF passband (1.9GHz) which will be added later. The term Z_3 will influence the spurious pole resonant frequency and their Q and the circuit stability. In the following two sections the transfer function is now analyzed for two cases, when Z_3 is resistive and when Z_3 is capacitive.

3.2.2.1 Basic notch filter with resistive load

Assuming that Z_3 is an ideal resistor R_3, the basic notch filter transfer function (3.25) now becomes:

$$\frac{i_3}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + R_3 \cdot j\omega \cdot C_s + 1} \tag{3.28}$$

and rearranging:

$$\frac{i_3}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R_3 + R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1} \tag{3.29}$$

This formula shows a spurious pole resonant frequency (ω_p) equal to the zero resonant frequency (ω_z), thus leading to potential zero-pole cancellation, which is not desirable since the notch depth will tend to be degraded by the presence of the poles, especially if they are poles with high Q (as would happen if R_3 is small). An enhanced resonator will be presented later which helps to correct this problem by moving the poles away from the zeroes.

As was mentioned before, during normal operation g_{m2} will be adjusted to comply with equation (3.27). In that situation, at the pole frequency (ω_p), the term in brackets on the denominator of equation (3.29), becomes simply:

$$\left(R_3 + R - \frac{g_{m2}}{\omega_p^{\,2} \cdot C_{\pi 2} \cdot C_{load}} \right) = \left(R_3 + R - R \cdot \frac{\omega_z^2}{\omega_p^2} \right) = R_3 \qquad (3.30)$$

Since R_3 is always positive, the system is therefore guaranteed to be stable.

Observe also that the Q of the poles has been decreased due to the additional positive resistance component (R_3) in the denominator of equation (3.29). This would suggest to use a large R_3 to promote stability. Clearly, a large R_3 improves the notch because it reduces the error current i_3 at the notch frequency. Unfortunately, there is always going to be a parasitic capacitance at node A which will shunt R_3 and may become the dominant load, especially at very high frequencies. A capacitive load would be bad for stability as will be shown further; hence R_3 would have to be sufficiently small to ensure stability by shunting the capacitive component to ensure that the total load is mostly resistive. Additionally an excessively large R_3 would generate a large voltage drop due to the DC bias current, thus limiting the ability of the circuit to operate at low supply voltages. Also a very large R_3 would increase the voltage gain of transistor Q_1, particularly at low frequencies, thus endangering stability at low frequencies. For these reasons, the size of R_3 would have to be moderate to low.

Observe also that the series resonator is in parallel with the load Z_3. The series resonator input impedance is very low at the 2.5GHz image frequency and can be made zero by properly tuning the current source I_2. On the other hand, at the 1.9GHz passband frequency (that is below the series resonant frequency) the series resonator input impedance is not zero, but is still relatively small and capacitive. For example, for this implementation L is in the order of 4nH in series with a total capacitance of 1pF for series resonance at 2.5GHz. With these values the series resonator input impedance at 1.9GHz is approximately -j36 ohms, which is then in parallel with the load Z_3. Thus if the load is

large (say a few hundred ohms) then the resonator input impedance will dominate the total load.

This can be illustrated by developing a simplified expression for the voltage gain from the input to node A as follows (where use has been made of equation (3.23) and Q_1 is considered to be operating at high frequency):

$$\frac{v_3}{v_{in}} = \frac{i_3 \cdot Z_3}{i_{c1} \cdot \left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}} \right) \right)} = \frac{Z_3}{\left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}} \right) \right)} \cdot \frac{1}{\left(1 + \frac{Z_3}{Z_{res}} \right)} \quad (3.31)$$

In this expression r_{e1} is the dynamic emitter resistance of transistor Q_1. For the case when Z_3 is much larger than Z_{res}, at the passband frequency, the above equation becomes:

$$\frac{v_3}{v_{in}} = \frac{Z_{res}}{\left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}} \right) \right)}; \text{ for...} Z_3 > Z_{res} \quad (3.32)$$

This formula shows that, for this circuit the voltage gain at the passband would be directly proportional to the resonator input impedance and independent of Z_3 provided that Z_3 is larger than Z_{res} which is the case for our circuit at the passband frequency as previously explained. Additionally, in order to improve linearity, R_{E1} would typically be in the order of 50 ohms and therefore it would be larger than Z_{res} at the passband frequency. For these reasons the voltage gain from input to node A will be small at the passband frequency, regardless of how large R_3 is made.

In conclusion, the circuit of Figure 3-7 (with Z_3 large) has poor passband gain and is not yet suitable for our application. A means of providing substantial passband voltage gain while retaining the benefit of the notch is needed.

The previous analysis indicates that if Z_3 were purely resistive, the circuit would be guaranteed to be stable and the zeroes could be tuned for infinite Q without creating stability problems. However the pole-zero cancellation would tend to degrade the notch, specially if Z_3 was made small.

3.2.2.2 Basic notch filter with capacitive load

As mentioned above, a parasitic capacitance will usually be present at node A (for example, the collector to substrate capacitance and collector to base capacitance as well as parasitics due to the interconnections), which can be dangerous as will be shown in the following analysis.

We suppose now that Z_3 in Figure 3-7 was purely capacitive, as follows:

$$Z_3 = \frac{1}{s \cdot C_3} = \frac{1}{j\omega \cdot C_3} \tag{3.33}$$

substituting this term into (3.25) above yields:

$$\frac{i_3}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + \dfrac{1}{j\omega \cdot C_3} \cdot j\omega \cdot C_s + 1} \tag{3.34}$$

and simplifying we obtain:

$$\frac{i_3}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + 1}{-\omega^2 \cdot (L \cdot C_s) + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_{load}} \right) + \left(\dfrac{C_s}{C_3} + 1 \right)} \tag{3.35}$$

Equation (3.35) shows that due to the presence of C_3 the spurious pole frequency has been increased. Also, if now the zeros are tuned for infinite Q (by adjusting g_{m2} to cancel the term in brackets in the numerator), the poles would have large Q and therefore the system would tend to be unstable.

3.2.2.3 Conclusions for the basic notch filter

From the above analysis, it is concluded that for the basic notch filter circuit of Figure 3-7:

- impedance Z_3 must be made mostly resistive in order to ensure stability.

- a purely resistive Z_3 leads to zero-pole cancellation potentially degrading the notch depth.
- a purely capacitive Z_3 makes the circuit potentially unstable and must be avoided.
- The passband voltage gain from input to node A is poor.

Finally, it is obvious that the circuit presented in Figure 3-7 is not practical yet, as a way is needed to extract the output signal, in this case the error current i_3, while at the same time providing substantial passband gain. This is done later in section 3.2.4, but first an enhanced LC series resonator is introduced in the following section which is then used to realize a cascoded notch filter.

3.2.3 An enhanced LC series resonator

Let us now examine the collector current (i_c) of the resonator transistor Q_{ef} of Figure 3-3. As indicated in the small-signal model (Fig. 3-4) the collector current is given by:

$$i_c = g_m \cdot v_\pi = g_m \cdot i_b \cdot Z_\pi \tag{3.36}$$

and for operation well beyond the current gain cutoff frequency we can use equation (3.12) and obtain:

$$i_c = g_m \cdot i_b \cdot \frac{1}{j\omega \cdot C_\pi} = i_b \cdot \frac{g_m}{j\omega \cdot C_\pi} = i_b \cdot \left(-j\frac{\omega_T}{\omega}\right) \tag{3.37}$$

Thus the collector current i_c is simply an amplified (and phase shifted) version of i_b and can be used to advantage to increase the conductance given by (3.21) by the feedback connection of the collector of Q_1 as shown in Fig. 3-10 below. Now the total current entering the enhanced resonator (i_s in Fig. 3-10) is given by:

$$i_s = i_b + i_c = i_b \cdot \left(1 - j \cdot \frac{\omega_T}{\omega}\right) \tag{3.38}$$

and the new input impedance (Z_s) of the enhanced resonator of Figure 3-10 is given by:

$$Z_s = \frac{v_{in}}{i_s} = \frac{v_{in}}{i_b \cdot \left(1 - j \cdot \frac{\omega_T}{\omega}\right)} = \frac{Z_{in}}{1 - j \cdot \frac{\omega_T}{\omega}} \tag{3.39}$$

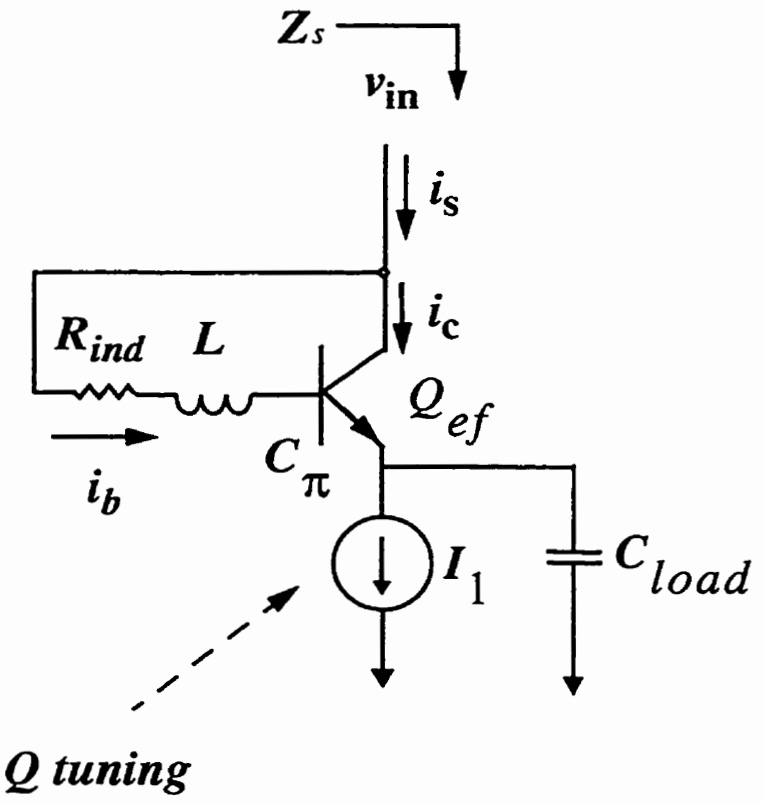

Figure 3-10: Enhanced series resonator

Thus, the effect of this connection is to reduce the impedance Z_{in} (equation (3.16) or (3.19)) by dividing it by the term $(1 - j\omega_T/\omega)$ where ω_T is the transit frequency in rad/sec of transistor Q_{ef} in Figure 3-10.

And the corresponding enhanced admittance (Y_s) is now given by:

$$Y_s = \frac{i_s}{V_{in}} = \frac{1}{Z_s} = \frac{s \cdot C_s \cdot \left(1 + \frac{g_m}{s \cdot C_\pi}\right)}{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \frac{g_m}{s^2 \cdot C_\pi \cdot C_{load}}\right) + 1} \tag{3.40}$$

This is now the sum of bandpass and lowpass second order responses. Thus, this admittance can be used as the feedback element in a loop to form a notch filter as will be shown in section 3.2.5. The advantage obtained by using this connection is that the gain of the bandpass response is increased substantially and a deeper notch can therefore be obtained, as was discussed when explaining equation (3.4) in section 3.1.

In the following section the enhanced resonator is used to implement a cascoded notch filter and the corresponding transfer function derived.

3.2.4 Realization of a cascoded notch filter

The enhanced series resonator of Figure 3-10 is now used in combination with a current adder circuit to obtain the cascoded notch filter shown in Fig.3-11 in which the resonator transistor is now Q_2.

This circuit is similar to the basic notch filter described in section 3.2.2 (see Figure 3-7) but with the load Z_3 replaced with a cascode (Q_3) in order to obtain good passband gain while preserving the notch. The emitter of cascode Q_3 acts now as the current summing node. In this circuit the cascode acts as a power gain element and it also isolates the series resonator from the output load which will be connected to the collector of the cascode as will be shown later in section 3.2.8. The base of cascode Q_3 is assumed to be perfectly AC grounded.

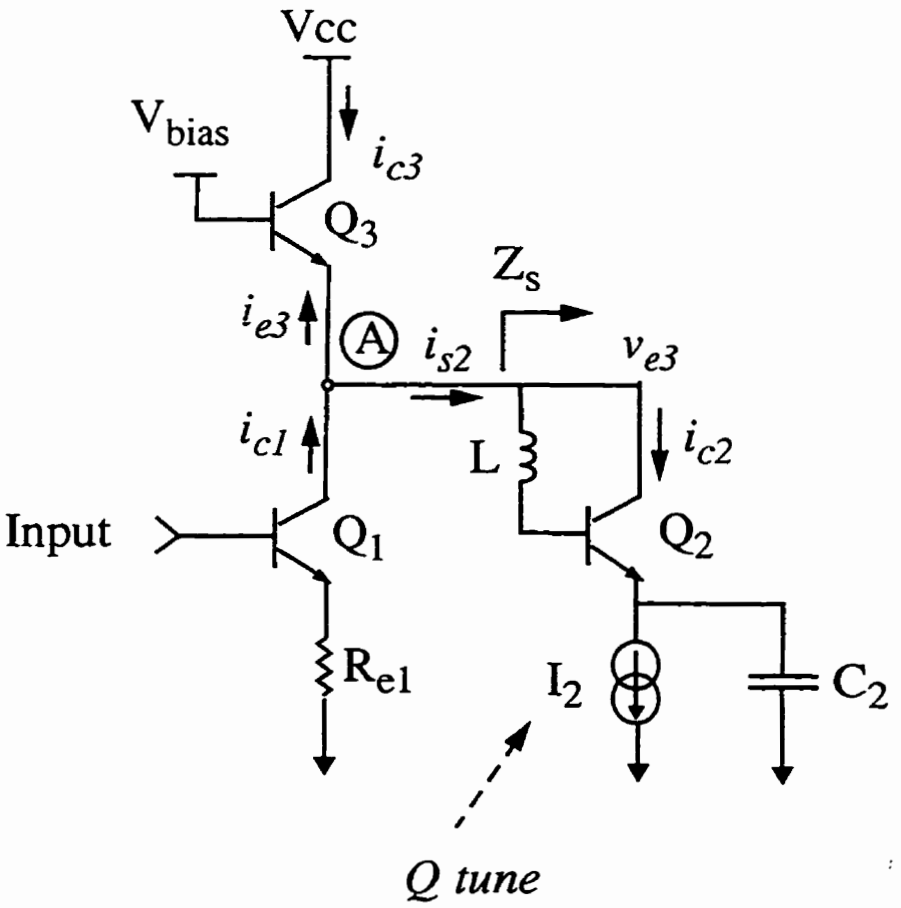

Figure 3-11: Cascoded notch filter

As previously, current i_{c1} can be treated as the input current and current i_{e3} as the output current. Current i_{s2} is the enhanced resonator input current which is generated by voltage v_{e3} present at the emitter of Q_3. Most importantly the impedance looking into the emitter of cascode Q_3 acts as a mostly resistive low impedance load. This will ensure stability of the circuit as will be shown in the following sections.

Applying Kirchoff's current law to the emitter of Q_3 with the currents in the directions shown in Figure 3-11 we have:

$$i_{e3} = i_{c1} - i_{s2} \tag{3.41}$$

and the explanation of the basic notching action is then the same as in section 3.2.2.

Away from resonance Z_s is very large and i_{e3} is simply equal to the input current i_{c1}. However at resonance Z_s is small and v_{e3} will generate a resonator current i_{s2}. The bias current I_2 can now be adjusted to reduce Z_s and make the amplitude of i_{s2} almost identical to that of i_{c1} so that the total current i_{e3} that enters the emitter of Q_3 is now very small.

For more clarity Figure 3-12 below shows a block diagram representation of node A at the emitter of Q_3. In this drawing the adder is based on nodal equation (3.41).

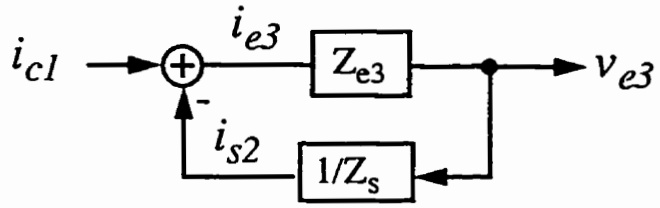

Figure 3-12: Block diagram of cascoded notch

For this diagram we have:

Z_{e3}: impedance looking into the emitter of the cascode Q_3 in Figure 3-11 above, assumed linear here.

$1/Z_s$: enhanced resonator input admittance (formula (3.40))

v_{e3}: emitter voltage of Q_3.

and simplifying the previous block diagram we have (where i_{e3} is the output variable):

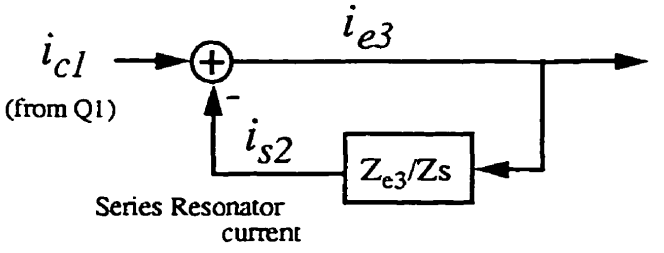

Figure 3-13: Compact block diagram of cascoded notch

In this diagram the loop gain is given by Z_{e3}/Z_s. The relative phases and magnitudes of Z_{e3} and Z_s then become important for stability. At the end of this section the circuit will be shown to be stable as long as Z_{e3} is mostly resistive. Thus the size and transit frequency (f_T) of cascode Q_3 must be carefully chosen.

From the block diagram of Figure 3-13 the following transfer function is readily obtained:

$$\frac{i_{e3}}{i_{c1}} = \frac{1}{1 + \frac{Ze_3}{Z_s}} \qquad (3.42)$$

Let us briefly examine this transfer function. At the resonance frequency (ω_o) Z_s is very small and the right hand side of equation (3.42) approaches zero, hence i_{e3} becomes very small and there is no output (the notch action). Away from resonance, Z_s is very large and the right hand side of equation (3.42) reduces to 1 and i_{e3} is simply equal to i_{c1} as expected (bandpass action).

Appropriately updating the equation for $1/Z_s$ (3.40) with the indices corresponding to the new schematic of Figure 3-11 and then replacing this in (3.42) above yields the complete transfer function for the filter frequency response:

$$\frac{i_{e3}}{i_{c1}} = \frac{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \frac{g_{m2}}{s^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{s^2 \cdot L \cdot C_s + s \cdot C_s \cdot \left(R + \frac{g_{m2}}{s^2 \cdot C_{\pi 2} \cdot C_2} \right) + Z_{e3} \cdot s \cdot C_s \cdot \left(1 + \frac{g_{m2}}{s \cdot C_{\pi 2}} \right) + 1} \tag{3.43}$$

where:

$$C_s = \frac{C_{\pi 2} \cdot C_2}{C_{\pi 2} + C_2} \tag{3.44}$$

Now back to the frequency domain for an explicit view of the negative resistance terms:

$$\frac{i_{e3}}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \frac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + Z_{e3} \cdot j\omega \cdot C_s \cdot \left(1 + \frac{g_{m2}}{j\omega \cdot C_{\pi 2}} \right) + 1} \tag{3.45}$$

We observe the same pair of complex zeroes in the numerator as before with resonant frequency (ω_z) given by:

$$\omega_z = \frac{1}{\sqrt{L \cdot C_s}} \tag{3.46}$$

During normal operation the filter is tuned by adjusting I_2 in the circuit of figure 3-11 in order to adjust g_{m2} so that at the zero frequency of resonance (ω_z) the term in brackets in the numerator of equation (3.45) cancels generating a very deep notch in the frequency response. Hence, to make the Q of the numerator infinite, g_{m2} is adjusted to comply with the following equation:

$$R = \frac{g_{m2}}{\omega_z^2 \cdot C_{\pi 2} \cdot C_2} \tag{3.47}$$

Observe now the denominator of equation (3.45) which exhibits a pair of spurious complex poles, but with added effect due to the connection of the collector of Q_2 as in Figure 3-11.

The term Z_{e3} will influence the spurious poles resonant frequency and its Q and circuit stability.

Let us assume that transistor Q_3 is a cascode with a perfectly AC grounded base and that for high frequency operation $Z_{\pi 3}$ is capacitive as in equation (3.12). A small signal analysis shows that the impedance looking into the emitter of the cascode is given by:

$$Z_{e3} = \left(\frac{1}{j \cdot \omega \cdot C_{\pi 3}} + r_{b3}\right) \cdot \frac{1}{\left(1 - j \cdot \frac{\omega_{T3}}{\omega}\right)} = \frac{1}{j \cdot \omega \cdot C_{\pi 3}} \cdot \frac{1}{\left(1 - j \cdot \frac{\omega_{T3}}{\omega}\right)} + \frac{r_{b3}}{\left(1 - j \cdot \frac{\omega_{T3}}{\omega}\right)} \quad (3.48)$$

which can be written as:

$$Z_{e3} = \frac{1}{g_{m3} + j\omega \cdot C_{\pi 3}} + \frac{r_{b3}}{\left(1 - j \cdot \frac{\omega_{T3}}{\omega}\right)} \quad (3.49)$$

For more clarity the previous equation can now be expressed as:

$$Z_{e3} = \frac{r_{e3}}{1 + \frac{j\omega}{\omega_{T3}}} + \frac{r_{b3}}{\left(1 - j \cdot \frac{\omega_{T3}}{\omega}\right)} \quad (3.50)$$

And when the operating frequency is significantly smaller than the transit frequency (say 10 times smaller) the previous formula can be approximated as (note that with this approximation we are only neglecting a very small resistive term due to r_{b3}):

$$Z_{e3} = \frac{r_{e3}}{1 + \frac{j\omega}{\omega_{T3}}} + r_{b3} \cdot \frac{j\omega}{\omega_{T3}} \qquad ;\left(\frac{\omega}{\omega_{T3}} \ll 1\right) \quad (3.51)$$

This formula shows that the magnitude of the inductive component depends on the cascode base resistance and the ratio of the operating frequency over the transit frequency.

For more insight we can express the previous formula as shown below:

$$Z_{e3} = r_{e3} - j \cdot r_{e3} \cdot \frac{\omega}{\omega_{T3}} + j \cdot r_{b3} \cdot \frac{\omega}{\omega_{T3}} \qquad ,\left(\frac{\omega}{\omega_{T3}} \ll 1\right) \quad (3.52)$$

This equation indicates that Z_{e3} consists of a resistive, a capacitive and an inductive component. The resistive component is the dynamic resistance r_{e3} which depends on the bias current through Q_3. The capacitive component is due to $C_{\pi 3}$, the base emitter junction capacitance of Q_3, which depends on the transistor transit frequency and the bias current and finally the inductive component is due to the gyration of the base resistance.

Formula (3.52) clearly shows that a cascode with high transit frequency results in a mostly resistive Z_{e3} which is desirable for stability as will be shown in the following sections. This formula also shows that Z_{e3} may be inductive or capacitive depending on the magnitudes of the emitter dynamic resistance and the base resistance. Both cases were encountered during the development of this work.

For example, for the 0.8 micron BiCMOS realization presented in section 3.2.5 the cascode is a transistor with a 60 x 0.8 micrometer emitter. The base resistance is 17 Ohms with an 8.6GHz f_T for a 2.9mA bias current (thus r_{e3} is 9 Ohms). Hence, in this case, the cascode emitter impedance according to (3.52) is inductive.

Observe however that r_{b3} can be smaller than r_{e3} while still having a cascode with a transit frequency which is an order of magnitude larger than the 2.5GHz operating frequency. This is possible with the high f_T afforded by state-of-the-art submicron processes. In such a case Z_{e3} would be capacitive.

For example, in chapter 4 the cascode is implemented in a high quality 0.5micron bipolar process. In this case the cascode has a 40x0.5 micron emitter size, a 4 Ohms base resistance and a 26.5GHz f_T for a 2.7mA bias current. Observe that the 2.5GHz operating frequency is more than 10 times smaller than the transit frequency. Now, according to (3.52) the gyrated base resistance contributes only with 0.4 Ohms of inductive reactance seen at the emitter. Also from (3.52) the capacitive reactance is now approximately 1 Ohm and as a consequence Z_{e3} is capacitive. This has been verified with simulations. This is not evident at first glance and could be dangerous for stability.

In the following two sections, we analyze the filter transfer function corresponding to a purely resistive cascode, and then using the actual cascode but neglecting the base resistance for simplicity. Adding the inductive term due to the base resistance will then only enhance stability.

3.2.4.1 Analysis of notch filter with purely resistive cascode

It is very instructive to obtain the filter transfer function assuming an ideal purely resistive cascode. In this case the impedance looking into the emitter of the cascode would be given by:

$$Z_{e3} = \frac{1}{g_{m3}} = r_{e3} \tag{3.53}$$

We can now replace (3.53) into (3.45) to obtain

$$\frac{i_{e3}}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + r_{e3} \cdot j\omega \cdot C_s \cdot \left(1 + \dfrac{g_{m2}}{j\omega \cdot C_{\pi 2}} \right) + 1} \tag{3.54}$$

and rearranging the transfer function for the resistive cascode case is:

$$\frac{i_{e3}}{i_{c1}} = \frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(r_{e3} + R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + r_{e3} \cdot C_s \cdot \dfrac{g_{m2}}{C_{\pi 2}} + 1} \tag{3.55}$$

Formula (3.55) clearly shows that due to the presence of resistor r_{e3} along with the addition of the collector current component (i_{c2}) the spurious pole resonant frequency (ω_p) has now been increased to:

$$\omega_p = \sqrt{\frac{r_{e3} \cdot C_s \cdot \dfrac{g_{m2}}{C_{\pi 2}} + 1}{L \cdot C_s}} = \omega_z \cdot \sqrt{r_{e3} \cdot C_s \cdot \frac{g_{m2}}{C_{\pi 2}} + 1} = \alpha_1 \cdot \omega_z \tag{3.56}$$

In this formula α_1 is always bigger than 1, therefore the spurious pole resonant frequency (ω_p) will always be higher than the zero resonant frequency (ω_z), thus avoiding a zero-pole cancellation. This is useful since otherwise the notch depth would be degraded by the presence of the pole. Let us emphasize that this is a spurious pole, and it will not be used for the bandpass response of the filter because it is not reliable enough (it depends on too many parameters and also it will move when adjusting I_2 for Q tuning the notch). Observe also that for this work the zero frequency is at 2.5GHz while the desired passband is at 1.9GHz, i.e. below the zero frequency, while the spurious pole is located above the zero frequency and therefore will not affect the 1.9GHz passband.

As was mentioned before, during normal operation g_{m2} will be adjusted to comply with equation (3.47). Therefore g_{m2} is adjusted to have:

$$R \cdot \omega_z^{\,2} = \frac{g_{m2}}{C_{\pi 2} \cdot C_2} \tag{3.57}$$

In that situation, at the pole frequency (ω_p) the term in brackets in the denominator of equation (3.55) can be expressed as:

$$r_{e3} + R - \frac{g_{m2}}{\omega_p^{\,2} \cdot C_{\pi 2} \cdot C_2} = r_{e3} + R - R \cdot \frac{\omega_z^2}{\omega_p^2} = r_{e3} + R \cdot \left(1 - \frac{1}{\alpha_1^2}\right) \tag{3.58}$$

Since α_1 is always bigger than 1, as was shown by equation (3.56), the above expression is always positive and the system is therefore guaranteed to be stable. Observe also that the Q of the spurious poles is limited by the additional positive resistance component (r_{e3}) in equation (3.55).

The above analysis indicates that if the impedance looking into the emitter of the cascode was purely resistive, the circuit would be guaranteed to be stable and the zeroes can be tuned for infinite Q without creating stability problems. However, in practice the emitter of cascode Q_3 may be capacitive (see equation (3.52) and in addition will have parasitic capacitances connected to it, such as the collector to substrate capacitance of the input

transistor Q_1 as well as the metal to substrate capacitance of the interconnections, which can be dangerous for stability as will be shown in the following section.

3.2.4.2 Analysis of enhanced notch filter with actual cascode

As previously indicated the cascode emitter impedance given by formula (3.52) may be inductive or capacitive. From a previous analysis (section 3.2.2.2) it is clear that a capacitive emitter impedance is dangerous for stability.

In this section the circuit is analyzed neglecting the cascode base resistance to simplify the analysis. As a result, the emitter impedance (Z_{e3}) becomes capacitive and this represents a worst case scenario. Adding the base resistance will enhance stability as will be shown at the end of this analysis. Before beginning the analysis let us introduce some useful formulas.

Any parallel R_p C_p circuit can be converted into its series equivalent using the following general transformations [34]:

$$R_{series} = \frac{R_p}{1 + Q_p^2} \tag{3.59}$$

$$C_{series} = C_p \cdot \left(\frac{Q_p^2 + 1}{Q_p^2} \right) \tag{3.60}$$

where the parallel RC quality factor can be defined as:

$$Q_p = R_p \cdot \omega \cdot C_p \tag{3.61}$$

for the case when $Q_p << 1$ these transformations simplify to:

$$R_{series} = R_p \qquad C_{series} = \frac{C_p}{Q_p^2} \qquad (Q_p \ll 1) \tag{3.62}$$

For the cascode Q_3 of figure 3-11, based on (3.49) and neglecting the base resistance for simplicity, the impedance looking into the emitter of the cascode (Z_{e3}) can be seen as r_{e3} in parallel with $C_{\pi 3}$. In this case the quality factor of Z_{e3} would be given by:

$$Q_p = re_3 \cdot \omega \cdot C_{\pi 3} = \frac{1}{g_{m3}} \cdot \omega \cdot C_{\pi 3} = \frac{\omega}{\omega_{T3}} = \frac{f}{f_{T3}} \tag{3.63}$$

This formula indicates that the cascode transit frequency must be substantially larger than the operating frequency in order to obtain low Q_p. Now, using (3.62), Z_{e3} would have the following series equivalent, when neglecting r_{b3} and for small Q_p:

$$Z_{e3} = r_{e3} + \frac{1}{s \cdot \frac{C_{\pi 3}}{Q_p^{\,2}}} = r_{e3} + \frac{Q_p^{\,2}}{s \cdot C_{\pi 3}} \tag{3.64}$$

This expression shows that the cascode equivalent series representation has a series resistance equal to its original parallel component (in this case r_{e3}) and a capacitive reactance much smaller than the original parallel reactance (since Q_p is less than 1). Therefore a low Q_p ensures that the impedance looking into the emitter of the cascode is mostly resistive and this, as will be shown below, leads to a stable system.

Replacing (3.64) in (3.45) yields now the following transfer function for i_{e3}/i_{c1}:

$$\frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + \left(r_{e3} + \dfrac{Q_p^{\,2}}{j\omega \cdot C_{\pi 3}} \right) \cdot j\omega \cdot C_s \cdot \left(1 + \dfrac{g_{m2}}{j\omega \cdot C_{\pi 2}} \right) + 1} \tag{3.65}$$

and rearranging terms i_{e3}/i_{c1} now becomes:

$$\frac{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} \right) + 1}{-\omega^2 \cdot L \cdot C_s + j\omega \cdot C_s \cdot \left(R + r_{e3} - \dfrac{g_{m2}}{\omega^2 \cdot C_{\pi 2} \cdot C_2} - \dfrac{g_{m2} \cdot Q_p^{\,2}}{\omega^2 \cdot C_{\pi 3} \cdot C_{\pi 2}} \right) + \dfrac{C_s \cdot Q_p^{\,2}}{C_{\pi 3}} + r_{e3} \cdot C_s \cdot \dfrac{g_{m2}}{C_{\pi 2}} + 1} \tag{3.66}$$

Comparing the denominator of this expression with the denominator of equation (3.55), for the purely resistive cascode case, shows that due to the presence of $C_{\pi 3}$ an additional negative resistance term has been added to the term in brackets in the denominator which increases the Q of the pole and, if excessively large, could make the system unstable.

Observe also that the spurious pole frequency has now been increased by the presence of both r_{e3} and $C_{\pi 3}$. The spurious pole frequency (ω_p) has now been shifted to:

$$\omega_p = \sqrt{\frac{r_{e3} \cdot C_s \cdot \frac{g_{m2}}{C_{\pi 2}} + \frac{C_s \cdot Q_p^{\,2}}{C_{\pi 3}} + 1}{L \cdot C_s}} = \omega_z \cdot \sqrt{r_{e3} \cdot C_s \cdot \frac{g_{m2}}{C_{\pi 2}} + \frac{C_s \cdot Q_p^{\,2}}{C_{\pi 3}} + 1} = \alpha_3 \cdot \omega_z \tag{3.67}$$

where

$$\alpha_3 = \sqrt{r_{e3} \cdot C_s \cdot \frac{g_{m2}}{C_{\pi 2}} + \frac{C_s \cdot Q_p^{\,2}}{C_{\pi 3}} + 1} \tag{3.68}$$

Observe that α_3 will always be greater than 1, thus the spurious pole frequency is always higher than the zero frequency and zero-pole cancellation is avoided, thus ensuring a frequency response with a deep notch.

To evaluate stability let us now examine the term in brackets in the denominator of equation (3.66), referred here as $B(\omega)$. Since g_{m2} will be tuned to comply with equation (3.57) we can express $B(\omega)$ as follows:

$$B(\omega) = R + r_{e3} - \frac{\omega_z^2 \cdot R}{\omega^2} - \frac{g_{m2} \cdot Q_p^{\,2}}{\omega^2 \cdot C_{\pi 3} \cdot C_{\pi 2}} \cdot \frac{C_2}{C_2} = R + r_{e3} - \frac{\omega_z^2 \cdot R}{\omega^2} - \frac{\omega_z^2 \cdot R \cdot Q_p^{\,2}}{\omega^2} \cdot \frac{C_2}{C_{\pi 3}} \tag{3.69}$$

In order to check stability we evaluate this expression at the pole frequency (ω_p):

$$B(\omega_p) = R + r_{e3} - \frac{\omega_z^2 \cdot R}{\omega_p^2} - \frac{\omega_z^2 \cdot R \cdot Q_p^2}{\omega_p^2} \cdot \frac{C_2}{C_{\pi 3}} = R + r_{e3} - \frac{R}{\alpha_3^2} \cdot \left(1 + Q_p^2 \cdot \frac{C_2}{C_{\pi 3}}\right) \quad (3.70)$$

Hence, for the system to be stable the above expression must yield a positive resistance. Thus, one must minimize the negative resistance term and therefore a cascode with very low Q_p at the pole frequency is desirable. For the present application, for the schematic of figure 3-11, for a 2.5GHz notch, $C_2/C_{\pi 3}$ is typically in the order of 2. Thus, since α_3 is always larger than 1, making Q_p equal to, say, 0.1 would ensure that equation (3.70) above is positive.

For more insight it is useful to rewrite equation (3.69) as follows:

$$B(\omega) = R + r_{e3} - \frac{\omega_z^2 \cdot R}{\omega^2} - r_{e3} \cdot \frac{\omega_{T2}}{\omega_{T3}} \quad (3.71)$$

which at the spurious pole frequency becomes:

$$B(\omega_p) = R - R \cdot \frac{\omega_z^2}{\omega_p^2} + r_{e3} - r_{e3} \cdot \frac{\omega_{T2}}{\omega_{T3}} \quad (3.72)$$

Since the spurious pole is at a higher frequency than the zero the first two terms of the right hand side of this equation yield a positive result. The last two terms will yield a positive result provided that the cascode transit frequency (ω_{T3}) is larger than the resonator transit frequency (ω_{T2}). This is typically the case for this type of circuit. Once again this shows that a cascode with high transit frequency minimizes the negative resistance contributed by the fourth term, hence improving stability.

Recall that, so far, the formulas in this section were derived neglecting the base resistance. If the base resistance was included in the above analysis (3.72) would become:

$$B'(\omega_p) = R - R \cdot \frac{\omega_z^2}{\omega_p^2} + r_{e3} - r_{e3} \cdot \frac{\omega_{T2}}{\omega_{T3}} + r_{b3} \cdot \frac{\omega_{T2}}{\omega_{T3}} \quad (3.73)$$

Thus the presence of the base resistance improves stability.

For example in the 0.8micron BiCMOS implementation of section 3.2.5 the cascode emitter impedance r_{b3} is larger than r_{e3} and Z_{e3} is inductive as discussed when examining formula (3.52). Additionally, simulations indicate that the cascode has an 8.6 GHz f_T for a 2.9mA bias current, while the resonator has a 5 GHz f_T. Hence, for this BiCMOS circuit (3.73) is positive and stability is assured.

However, for the 0.5 micron implementation of chapter 4 the cascode emitter impedance is capacitive because the cascode base resistance is smaller than the emitter dynamic resistance as discussed when examining formula (3.52). However, in that design (see section 4.3.3) the resonator transit frequency is made much smaller than the cascode transit frequency and as a result (3.73) will be positive and stability is also assured.

From the above analysis, it is concluded that for the cascoded notch filter which uses the enhanced resonator (shown in figure 3-11):

- a capacitive impedance Z_{e3} looking into the cascode emitter tends to make the system unstable.
- Z_{e3} must have low Q, that is it must be made mostly resistive to ensure stability. Hence, the cascode must have an f_T substantially larger than the operating frequency.
- a mostly resistive Z_{e3} results in a transfer function with a spurious pole frequency which is higher than the zero frequency and therefore avoids pole-zero cancellation and a better (deeper) notch should therefore be obtained.

Therefore the cascode transistor must be properly selected, with sufficient transit frequency to ensure stability as well as lowest noise. For a given bias current, say 3mA for low power operation, a smaller cascode would yield higher transit frequency but also higher noise, while a larger cascode would yield lower noise but also poorer transit frequency. This is a design trade-off.

3.2.5 A notch filter for image rejection

The basic notch filter is now combined with a tuned amplifier to implement the completed image reject filter shown in Figure 3-14.

The circuit consists of a cascoded amplifier (Q_1, Q_3) to which the series (notching) resonator has been added (L_2, Q_2, C_2). The cascoded configuration provides improved frequency response [41]. The combination of Q_3 and the L_3-C_3 tank resonator provides a common-base amplifier which gives power gain from node v_{e3}. The error current i_{e3} in the notch filter, equation (3.41), now becomes the input current to the common base amplifier implicit in the cascode transistor Q_3.

Resistor R_{E1} at the emitter of Q_1 provides degeneration for improved linearity at the price of an increased noise figure. The cascoded amplifier is tuned to the passband at 1.9GHz using an LC tank (L_3, C_3) at the collector of transistor Q_3. The on-chip capacitor (C_4) at the cascode base ensures a good AC ground. The cascoded amplifier output is buffered with a pair of emitter followers to enable it to drive 50 ohm loads for testing purposes.

The series resonator (L_2, Q_2, C_2) is tuned for 2.5GHz. To intuitively grasp the circuit operation, assume that the series resonator creates a zero impedance at the emitter of Q_3 when the series resonator Q is tuned to infinity. This zero impedance path shunts the input signal current from Q_1. Thus, at the notch frequency, no current flows through Q_3 and there is no output signal on the LC tank (L_3, C_3). However, at the passband frequency (1.9GHz) the series resonator presents high impedance (and removes itself from the circuit) and thus the circuit acts as a tuned amplifier with gain.

Assuming that transistor Q_1 is operating at high frequency and that the output buffer is ideal the transfer function of the notch filter can be approximated as follows.

$$\frac{v_{out}}{v_{in}} = \frac{v_3}{v_{in}} = \frac{i_{c3} \cdot Z_3}{i_{c1} \cdot \left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}} \right) \right)} \tag{3.74}$$

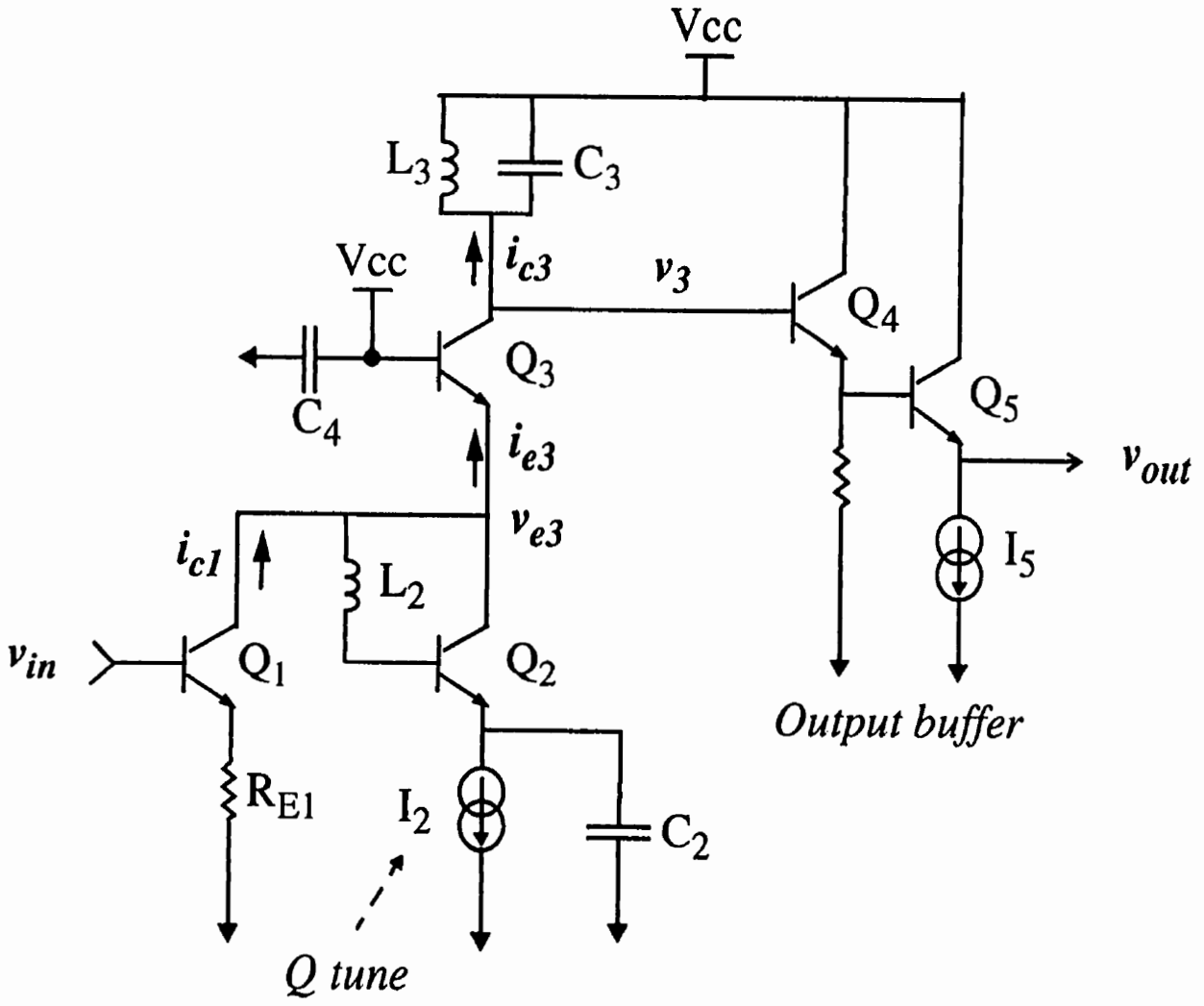

Figure 3-14: Image reject filter schematic

where Z_3 is the complex impedance of the L_3-C_3 tank, r_{e1} is the dynamic emitter resistance of Q_1 and ω_{T1} is the transit frequency of Q_1.

For simplicity, assuming an ideal cascode and considering i_{e3} equal to i_{c3}, the previous equation becomes:

$$\frac{v_{out}}{v_{in}} = \frac{v_3}{v_{in}} = \frac{Z_3}{\left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}}\right)\right)} \cdot \frac{i_{e3}}{i_{c1}} \tag{3.75}$$

The ratio of i_{e3}/i_{c3} is as previously developed in equation (3.65) and contains a pair of complex zeroes at the image frequency(2.5GHz) and a pair of spurious poles at a higher frequency as explained in section 3.2.4.3.

Replacing the expression for Z_3 in the previous equation yields:

$$\frac{v_{out}}{v_{in}} = \frac{1}{\left(r_{e1} + R_{E1} \cdot \left(1 + j \cdot \frac{\omega}{\omega_{T1}}\right)\right)} \cdot \frac{j\omega / C_3}{\left((j\omega)^2 + \frac{1}{R_{p3} \cdot C_3} \cdot j\omega + \frac{1}{L_3 \cdot C_3}\right)} \cdot \left(\frac{i_{e3}}{i_{c1}}\right) \tag{3.76}$$

In this expression the parallel tank resistance R_{p3} represents the inductor losses. Clearly a new pair of poles have been added due to the presence of the tank, with resonant frequency ω_{p3} given by:

$$\omega_{p3} = \frac{1}{\sqrt{L_3 \cdot C_3}} \tag{3.77}$$

Thus the filter transfer function of equation (3.76) has a pair of complex zeroes located at a frequency ω_z, defined by equation (3.46), a pair of desired passband poles located at frequency ω_{p3}, defined by equation (3.77), and finally a pair of spurious poles which were defined in equation (3.67). For the present application the passband poles would be located at 1.9GHz and the zeroes at 2.5GHz, while the spurious poles would be located at a higher frequency. This transfer function shows that to obtain good passband gain at the resonant frequency ω_{p3}, a large R_{p3} is useful, that is, a good quality inductor is beneficial. Also, transistor Q_1 should have a transit frequency (ω_{T1}) which is, say, an order of magnitude

larger than the desired passband frequency to avoid degrading the gain. Note that this transfer function is only a guideline to understand the functioning of the filter. To develop a full transfer function which includes parasitics and second order effects would be very complicated. Instead we rely on computer simulations to complete the design.

The frequency response of the completed filter obtained using the HPEESOF/Libra simulator is shown in Fig.3-15. This simulation did not include layout parasitics. The passband can be seen at approximately 1.8GHz and the notch at 2.67GHz (the measured results will show that due to parasitics, the notch frequency is actually very close to the desired 2.5GHz). The notch Q was tuned for maximum depth by adjusting the bias current through transistor Q_2 to a value of 0.8mA (see schematic, Fig.3-14).

The Libra simulation of the image reject filter included bondwires (assumed to be 1nH) but did not include capacitive parasitics. However, care was taken in adjusting the inductor model as follows. A test fixture of the inductor by itself was also fabricated and measured on-wafer and with these measurements the inductor model was adjusted for more accurate simulation. It was found that the 4nH nominal inductor yielded a measured inductance of 4.95nH at 2.5GHz. This was due primarily to two factors: the additional inductance due to the inductor connections and the inductor self-resonance. The original model consisted of two π-sections each with a 2nH ideal inductor. The π-section model has been described by Long [5] and is not repeated here. The nominal 2nH inductor was increased to 2.3nH so as to obtain a simulated inductance which at 2.5GHz agreed with the measured value of 4.95nH.

The image reject circuit was fabricated in the bipolar subset of NORTEL's 0.8 micron BiCMOS technology [42] [43]. It was packaged in a 20 pin Ceramic Surface Mount Package and mounted in a high frequency test fixture manufactured by Triquint Semiconductor. The input was not 50 Ohm matched.

The forward transmission coefficient (S_{21}) was measured with an HP8753B network analyzer both on-wafer and in the packaged device. A "Bias-T" network connected to the base of Q_1 was used to bias Q_1 to a 2.1mA collector current.

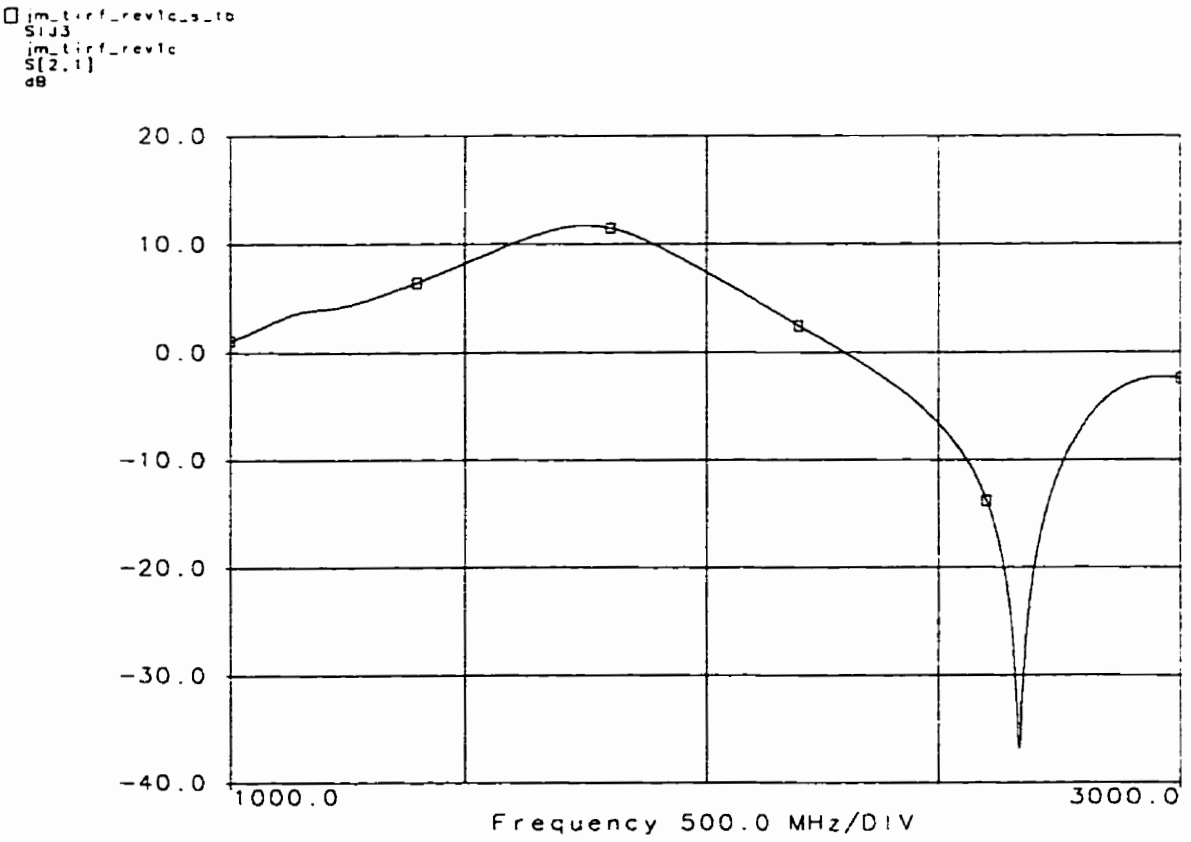

Figure 3-15: Simulated image reject filter forward transmission coefficient (S_{21}) on 0.8 micron BiCMOS

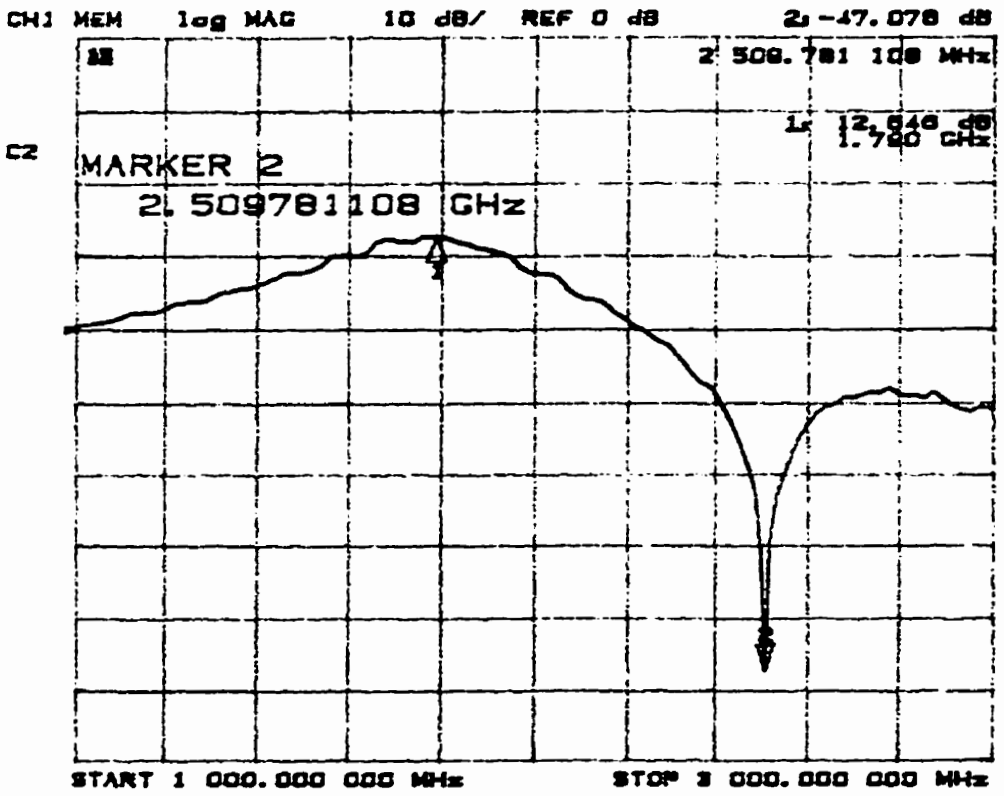

Figure 3-16: 2.5GHz image reject filter measured forward transmission coefficient (S21) without input matching (0.8 micron BiCMOS)

The measured S_{21} for the packaged device is shown in Fig. 3-16. The notch depth was adjusted by tuning the current source I_2 at the emitter of Q_2 to 1.15mA (see schematic Figure 3-14). The plot clearly shows the notch at 2.52GHz with -47dB loss while the passband gain is 12.6dB at 1.8GHz. Thus the measured rejection was 59dB.

Observe that the simulated notch frequency (2.67GHz) is 160MHz higher (6%) than the measured one (2.509GHz), which is to be expected due to parasitics and process variation. The fact that the notch frequency was exactly at 2.5GHz is because it was designed this way based on a previous experiment. A previously fabricated chip with a capacitive load of 5.25pF formed by 10 small 0.5pF and one 0.25pF capacitors in parallel was micro-surgered and it was found that when the load was made 2pF the notch was at 2.519GHz.

Table 3-1 summarizes the simulated and measured results obtained for this filter. As mentioned previously the Libra simulation did not include parasitics while the HSPICE simulations did include capacitive parasitics.

Table 3-1: 2.5GHz Notch filter results (fabricated on 0.8 micron BiCMOS):

Parameter	**Simulation, Libra**	**Simulation, Hspice**	**Measured (packaged)**
Gain @ 1.8GHz	11.5dB	12.3dB	12.6dB
NF @ 1.8GHz	11.3dB	11.1dB	11.4dB
Input IP3	-3.2dBm	n/a	-4.7dBm
Notch frequency	2.67 GHz	2.65 GHz	2.509 GHz
Notch depth	50 dB	50 dB	59 dB
DC current	2.8mA	2.72mA	3.2mA
Power supply	3V	3V	3V

Table 3-1 shows good agreement between simulation and measurement results. Measured and simulated gain and noise figure are very close. However the passband is not at 1.9GHz

but instead at 1.8GHz because in the first iteration layout parasitics were not extracted and therefore the simulation was inaccurate. This has been corrected in future versions. It was also interesting to observe that the HSPICE and the Libra simulation results agree very well.

The measured NF (11.4dB) is higher than desirable, due to the presence of degeneration resistor R_{E1} and also due to the presence of the notch which tends to pull the NF up. Additionally the circuit was not input matched. In a matched circuit an increase in gain and improvement in noise figure would be expected. These results also indicate that a low noise pre-amplifier is required in front of this filter in order to ensure an overall low NF for a receiver front-end application, as will be done in chapter 4. Observe also that the filter input matching is not a requirement when the filter is used within a monolithic context as will be done in this work.

In summary, the image reject filter presented in this chapter consists of a tuned amplifier with 12dB passband gain at 1.9GHz and a deep notch located at 2.5GHz (non-tunable in this iteration) to reject the undesired image. The complete transfer function for the notch filter was derived and the design equations for the passband and notch frequencies provided. Measured results show that the circuit is stable and that 59dB image rejection is possible by adjusting a current source to obtain a deep notch.

Thus, this chapter demonstrates for the first time the feasibility of a low power monolithic notch filter for image rejection [31]. However, improved performance is needed. This is addressed in the next chapter where the above image filter is improved and integrated with an LNA.

Chapter 4 LNA with image reject filter

We now go on to integrate an LNA with an improved and tunable version of the previously described notch filter. It is essential that the circuit be stable. Additionally, low noise is fundamental, as well as high IIP3 and sufficient gain to overcome the noise created by the mixer stage, which will follow. The proposed circuit must meet all these (sometimes) conflicting criteria.

A narrowband receiver is in general suitable for cellular applications. For example for DECT the frequency band is 1881-1887MHz, i.e., a 6MHz total band centered at 1884MHz. With the availability of on-chip inductors it is now possible to implement monolithic tuned amplifiers which are inherently better than broadband amplifiers for RF applications as described in chapter 2. The use of inductors instead of resistors allows for a lower supply voltage and also yields a reduction of circuit noise. Therefore a tuned amplifier is used for the LNA in this work.

The design of an LNA integrated with the image filter will be briefly described and, very promising simulated results with NORTEL's NT25 0.5 micron bipolar technology [38] will be presented. The circuit was fabricated in two different fabrication runs referred to as batch 1 and batch2. Experimental results are reported here.

NT25 is a 0.5 micrometer self-aligned silicon bipolar process which exhibits vertical NPN transistors with 25GHz transit frequency (f_T) and a maximum oscillation frequency (f_{max}) of 40GHz. NT25 offers Triple Layer Metal (TLM) interconnects. The on-chip inductors are realized with 2 micrometer thick top metal aluminum for Qs from 6 to 10 depending on the inductor geometry. The process exhibits 5V linear Metal Insulator Metal (MIM) capacitors with 1fF/μm^2 capacitance. Capacitors measured by the author yielded Qs of 30 at 1.9GHz.

NT25 is much superior to the 0.8 micron BiCMOS process with 11GHz f_T which was used for the first filter prototype presented in chapter 3, and was therefore selected for the integrated receiver, which begins in this chapter with the integration of the LNA and the image filter.

4.1 Design considerations (stability, noise figure and linearity)

Typically the LNA is the most important contributor to the receiver noise figure. Thus it is essential to have an LNA with as small a noise figure as possible. Usually, the LNA will have some form of feedback to ensure stable operation and high linearity.

A common-emitter topology is selected for the LNA in order to minimize the noise figure while obtaining good gain [36]. A cascoded amplifier was also considered because it would eliminate the Miller capacitance, thus increasing the bandwidth of the amplifier and making the input transistor practically unilateral, thereby simplifying the input matching network. Unfortunately a cascoded LNA amplifier exhibits higher noise than a single transistor topology (for the same bias current). Additionally a single transistor LNA has the potential to be used at a very low voltage supply (1V) while the cascode requires a larger supply (1.9V minimum).

The LNA integrated with the image filter is shown in Fig.4-1. The LNA consists of transistor Q_1 with an LC tuning tank at the collector (L_1 and C_1) and emitter degeneration provided by inductor L_{e1}. Components L_1 and C_1 are selected to resonate at 1.9GHz to provide the desired passband response. For this design, in order to minimize base resistance, the largest available transistor in NORTEL's NT25 library was selected for the LNA. This is a transistor with 80micron x 0.5micron emitter and it was biased at 3mA. This bias current was selected to minimize power consumption and also to obtain a low noise figure by keeping the device current density close to the minimum noise figure region. Bipolar transistors show an optimum noise current density ten times smaller than the peak f_T current density [38]. Our device reaches its peak f_T with a 22mA collector current (based on device simulation), hence a collector current in the order of 2-3mA will ensure minimum noise figure.

Emitter degeneration inductor L_{e1} provides feedback necessary to ensure stability and improve linearity. A large L_{e1} reduces the amplifier gain and improves stability but degrades the noise figure because monolithic inductors on silicon have limited Qs in the order of 6 to 10. Thus a larger inductor has larger losses which inject more thermal noise to

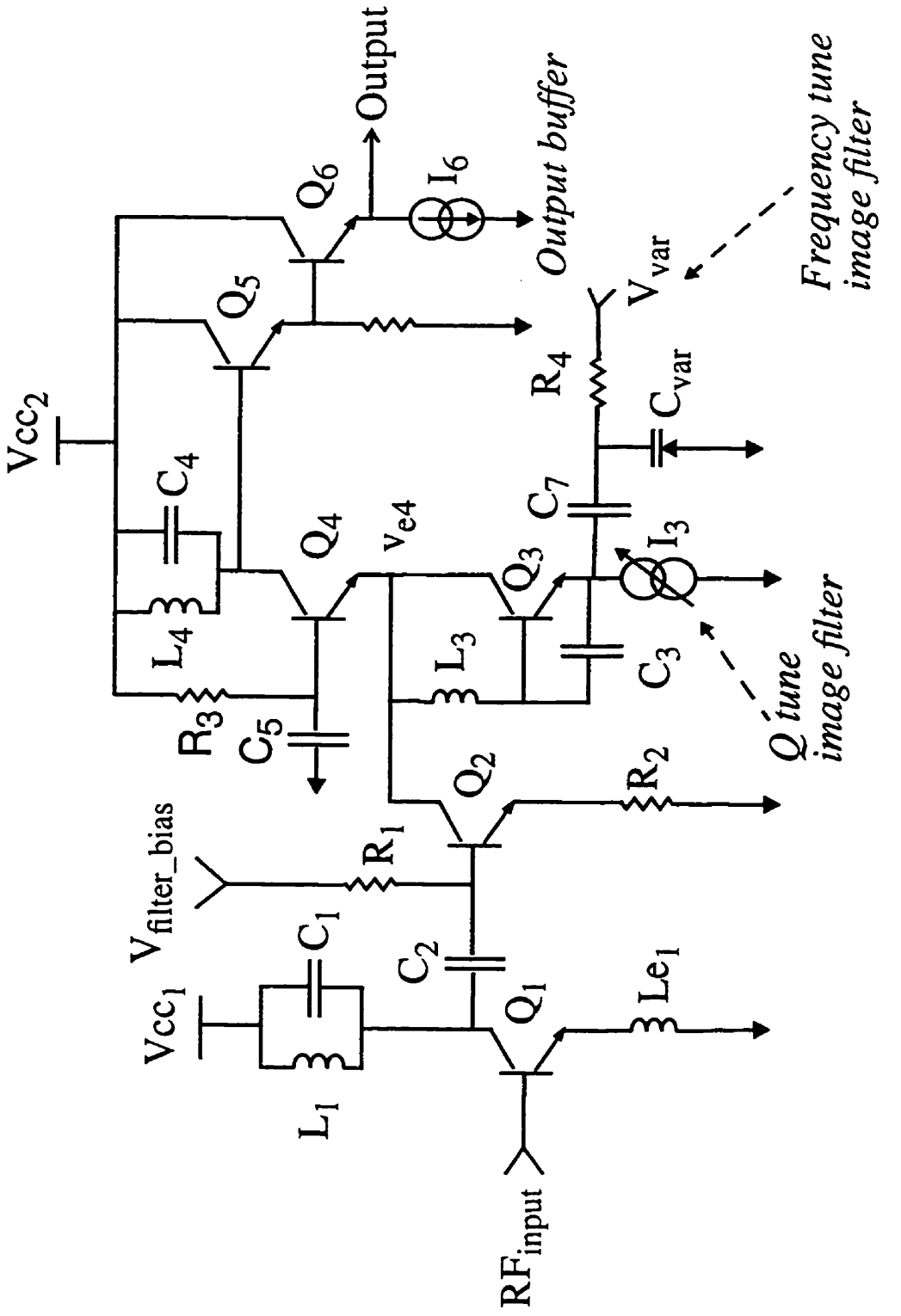

Figure 4-1: LNA with tunable image reject filter

the amplifier input. At the same time L_{e1} determines part of the input impedance, thus indirectly defining the input matching network.

It is well known that at high frequencies an inductor at the emitter is gyrated to look like a resistor at the base of the LNA transistor [44] as was illustrated in Figure 3-6 of section 3.2.1 for the case of the emitter follower. Since the LNA transistor has a very small base resistance (approximately 2 ohms for the selected transistor) the gyrated load reactance practically defines the real part of the input impedance. Thus it would appear convenient to select the inductor size so as to make the real part of Z_{in} equal to 50ohms [38][40], thus simplifying the input matching network (a single off-chip series inductor connected to the base of the transistor would then be required to achieve 50ohm input matching). However, this concept must be carefully evaluated here because the device is not unilateral.

When the LNA LC tank resonates (at 1.9GHz) the collector load is purely resistive and in the order of 250 ohms, thus yielding a large voltage gain. In this situation the strong feedback due to the Miller capacitance substantially reduces the input impedance. As a consequence, in order to obtain the desired 50 ohms, an excessively large emitter inductor would be required, thus degrading the noise figure as shown by the simulation results in the Table 4-1 below. Adding a cascode to the LNA to reduce the Miller effect was also considered but was found to degrade the noise figure further.

Table 4-1: 1.9GHz LNA with image reject filter (0.5 micron bipolar)

L_{e1}	Z_{in}	NF	Gain	K	B_1	IIP3
1.3nH	37.9 -j82.8	3.4dB	24.3dB	2009	0.96	-13.5dBm
1.7nH	52.4 -j96.7	4.0dB	22.7dB	2330	0.95	-11.9dBm

The simulations of Table 4-1 for two different values of L_{e1} were done at the schematic level with the circuit nominal component values, but without actual layout parasitics (inductive nor capacitive). Inductor L_{e1} is simply modeled as an ideal inductor in series with a resistor as these are preliminary simulations. The supply voltages V_{cc1} and V_{cc2}

were 3V DC and bias current 3mA. More details on the simulation can be seen in section 4.3.

In Table 4-1 K is the Rollett stability factor [45] and B_1 is the 2-port stability criterion, given by:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{4.1}$$

where Δ is the determinant of the S-parameter matrix.

A set of necessary and sufficient conditions for unconditional stability are:

$$K > 1 \qquad B_1 > 0 \tag{4.2}$$

In Table 4-1 the stability factors at the passband frequency are shown. However, it was verified that the B_1 factor was always larger than zero from very low (10MHz) up to very high frequencies (10 GHz). The minimum value for B_1 was 0.6 and it occurred at 2.95GHz. The K factor was always above 2000 for all frequencies.

Table 4-1 above shows that in order to obtain an input impedance with 50 ohm real part a 1.7nH inductor is required and a 4dB noise figure would be obtained with a -11.9dBm IIP3. On the other hand using a 1.3nH inductor the input impedance reduces to 37.9 ohms but the NF improves substantially to 3.4dB and the linearity reduces to -13.5dBm. Thus there is a clear trade-off between noise figure and linearity. With both inductors comparable stability factors are obtained. Hence, in this work, in order to obtain a lower noise figure the 1.3nH inductor was preferred. The input impedance will then be matched to 50 ohms by means of an external LC circuit. These external components have high Qs and therefore will add minimal noise while ensuring good matching. Note that these external elements will change the noise figure because they change the matching as will be shown in section 4.3.1.

An inductor smaller than 1.3nH could also have been attempted, however this would reduce the IIP3 below -13.5dBm. This value is considered to be a minimum acceptable in order to have some margin so that the whole receiver front-end has sufficient linearity for a portable radio application. Since it is not desirable to further reduce linearity and it is unwise to further reduce stability, the 1.3nH inductor was kept. It was decided to first

obtain experimental data from fabricated devices before attempting any additional optimization.

In summary the approach used for the LNA design was to make the emitter degeneration inductor Le_1 as small as possible for low noise figure and maximum gain, but not too small so as to cause unacceptable linearity and stability. The input matching will then be realized using an off-chip LC network.

Hence a 1.3nH nominal inductor was designed with GEMCAP2 [5][46]. A few iterations were needed to obtain the finished square spiral geometry.

As shown in Fig.4-1 the LNA collector is AC coupled to the image reject filter input by means of capacitor C_2. The filter is described in detail in the following section.

4.2 Improved image reject filter incorporated with the LNA

The series resonator used for the integrated LNA with image rejection described in section 4.1 is an improved version of the previously fabricated filter which was described in chapter 3. As shown in Figure 4-1 the image reject filter proper consists of transistors Q_2, Q_3 and Q_4. Transistors Q_2 and Q_4 form the cascoded amplifier to which the series (notching) resonator has been added (L_3, Q_3, C_3, C_7, C_{var}). Resistor R_2 at the emitter of Q_2 provides degeneration for improved linearity at the price of some increased noise. Transistor Q_2 is biased nominally at 2.5mA by applying a DC bias voltage (V_{filter_bias})to resistor R_1 which also acts as an RF blocking resistor.

The cascoded amplifier is tuned to the passband at 1.9GHz using an on-chip LC tank (L_4, C_4) at the collector of transistor Q_4. Observe that the base of the cascode (Q_4) is now connected to Vcc_2 by means of resistor R_3 to provide the required DC bias and the on chip capacitor C_5 ensures a low AC impedance connection to ground.

The cascoded amplifier output is buffered with a pair of emitter followers (Q_5, Q_6) to enable the circuit to drive 50 ohm loads for testing purposes as well as to drive the mixer

stage that follows. In this manner the mixer load will not detune nor reduce the passband gain of the filter response.

The series resonator is implemented here with inductor L_3 in series with the base of the emitter follower Q_3 whose emitter is loaded with a capacitor C_7 in series with C_{var}. Observe that now there is an additional capacitor (C_3) connected across the base emitter junction of Q_3, i.e. in parallel with the junction capacitance of Q_3 ($C_{\pi 3}$). The purpose of capacitor C_3 is to improve the tuning as well as the linearity of the notch filter as will be explained in section 4.2.2.

4.2.1 Tuning of notch frequency

The frequency of resonance of the series resonator of Figure 4-1 is now given by:

$$f_{notch} = \frac{1}{2\pi \cdot \sqrt{L_3 \cdot \frac{(C_3 + C_{\pi 3}) \cdot C_s}{(C_3 + C_{\pi 3}) + C_s}}} \tag{4.3}$$

where C_s is the series combination of C_7 and the varactor capacitance (C_{var})as follows:

$$C_s = \frac{C_7 \cdot C_{var}}{C_7 + C_{var}} \tag{4.4}$$

The function of C_7 is simply to decouple the varactor DC control voltage (V_{var}) from the DC voltage present at the emitter of Q_3. C_7 is made larger than C_{var} so that the varactor capacitance will dominate equation (4.4) and effectively control the tuning range.

The frequency of the notch can be centered by adjusting the varactor capacitance with the DC bias voltage V_{var}, thus allowing to compensate for process variations and possible tuning if required. R_4 is an RF blocking resistor which ensures that the low impedance of the voltage source V_{var} does not affect the resonator circuit.

Measured results of the frequency tuning range will be shown in section 4.5.

4.2.2 "Q tuning" of image reject filter

In the circuit of Figure 4-1 the input impedance Z_b looking directly into the base of Q_3 is given by:

$$Z_b = \frac{1}{j\omega} \cdot \left(\frac{1}{(C_3 + C_{\pi 3})} + \frac{1}{C_s} \right) - \frac{g_{m3}}{\omega^2 \cdot (C_3 + C_{\pi 3}) \cdot C_s} \tag{4.5}$$

where $C_{\pi 3}$ is the emitter-base capacitance of transistor Q_3 and g_{m3} is the transconductance of Q_3,which depends only on the DC bias current of the transistor (I_3). Hence, in this circuit the amount of negative resistance seen at the base of Q_3 is controlled by adjusting I_3. Therefore the notch depth is controlled by adjusting I_3; this procedure is referred to as "Q tuning".

Observe that when current I_3 is adjusted for "Q tuning" this will also change $C_{\pi 3}$, thus in principle affecting the resonant frequency given by equation (4.1). However since in this improved design C_3 is approximately 10 times larger than $C_{\pi 3}$ the frequency shift is greatly minimized. This is made possible by the high f_T (25GHz) afforded by NORTEL's 0.5micron bipolar process used in this work, for which the external capacitor C_3 can easily be made an order of magnitude larger than $C_{\pi 3}$ while still realizing a high frequency notch.

Adding C_3 effectively decouples the Q tuning from the frequency tuning, i.e. the notch frequency is changed little when the Q tuning is performed. Therefore, effectively in this design the notch frequency tuning and the notch Q tuning are orthogonal to each other. This also makes the design robust against process variation on the transistors.

The addition of C_3 also substantially improves the linearity of the notch filter by reducing the amount of voltage across the base-emitter junction of Q_3.

4.3 Analysis of 1.9GHz LNA with image rejection

This section presents various simulation results of the LNA with image rejection circuit shown in Figure 4-1. Schematic level simulations were done using the HPEESOFV6.0/ Libra simulator in order to obtain the frequency response as shown in section 4.3.1. Also, using a layout extracted netlist with parasitics, HSPICE simulations were conducted in

order to perform a detailed noise analysis as described in section 4.3.2. Finally in section 4.3.3 the linearity at the image frequency is analyzed.

4.3.1 Frequency response (S21), noise figure and IIP3

These are schematic level simulations which do not contain layout parasitics (neither capacitive nor inductive) because they were originally done before implementing the layout. However the simulations are very valuable because they show functionality and a good estimate of performance. These simulations were done using typical transistor models.

Accurate lumped models are used for the inductors. L_1, L_3 and L_4 are 3.5nH inductors with the high frequency lumped model readily available in the NORTEL's NT25 library. L_{e1} is a 1.3nH inductor which was custom designed for this circuit and a compact lumped model developed by the author. These inductor models are two π-sections in series derived from the inductor layouts using the GEMCAP2 program [5] [46].

For this simulation the wirebonds connecting Vcc_1 and Vcc_2 to their respective 3V DC supplies were assumed to be 1nH with a quality factor (Q) of 30. Note that two different supplies are used for the LNA and the filter in order to prevent feedback which could lead to undesired oscillations.

The LNA transistor Q_1 was biased at 3mA while the filter transistor Q_2 was biased at 2.5mA. For this simulation the passband was deliberately set to 1.9GHz (the desired value) by adding an extra 0.29pf to the filter output tank (in parallel with C_4) to represent parasitic capacitances. C_{var} was represented as a fixed capacitor properly sized to 2.06pF to place the notch at 2.5GHz. Current source I_3 was then adjusted to 0.49mA to obtain a deep notch at 2.5GHz.

The circuit was simulated with and without input matching network. Figure 4-2 shows the simulated forward transmission coefficient S_{21} for the unmatched case, with a passband peak gain of 24.3dB at 1.9GHz and a deep notch at 2.5GHz. This passband gain is very useful because it minimizes the noise contribution of the mixer stage that will follow.

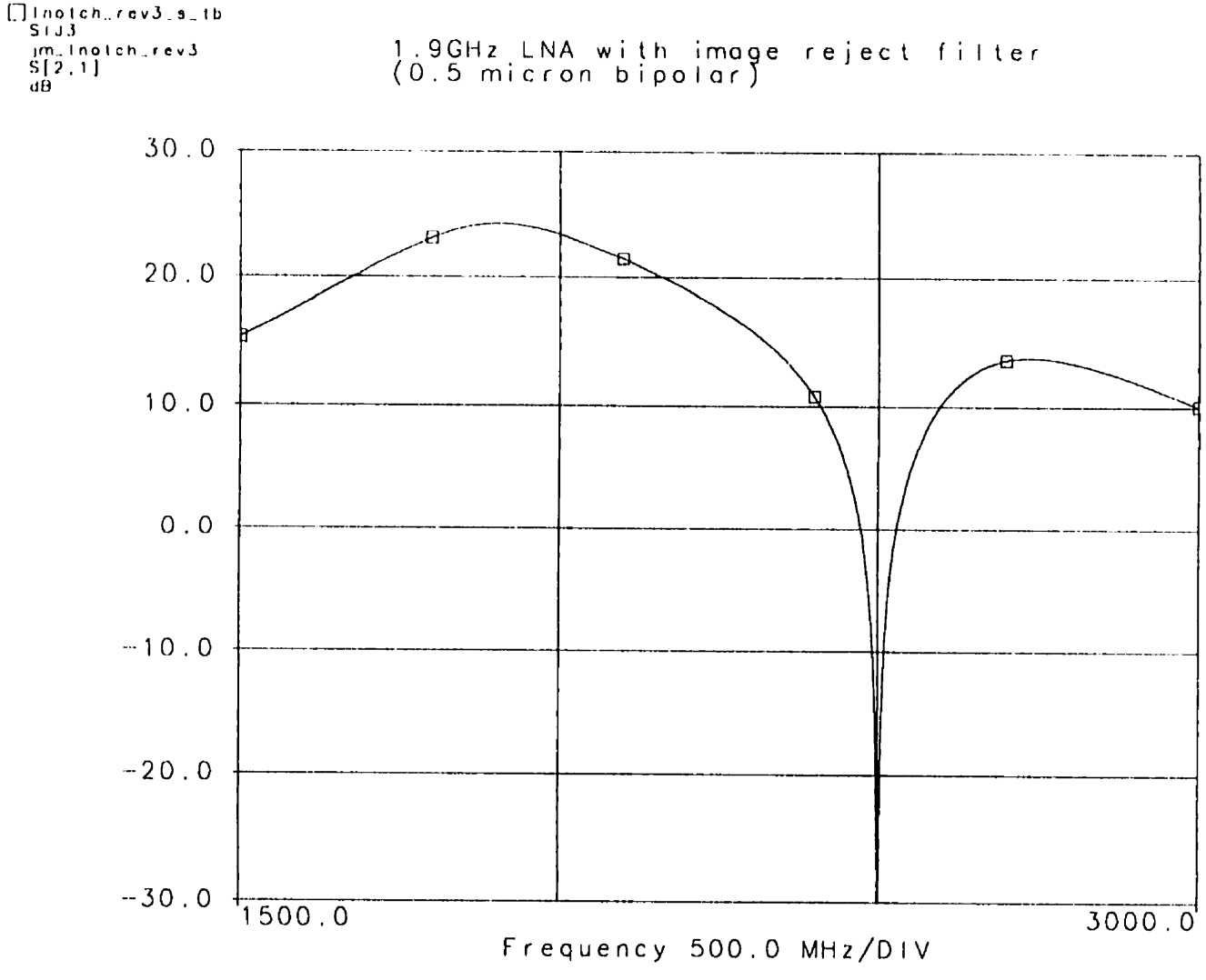

Figure 4-2: Simulated forward transmission coefficient (S21) of LNA with image reject filter (unmatched) with passband at 1.9GHz and notch at 2.5GHz

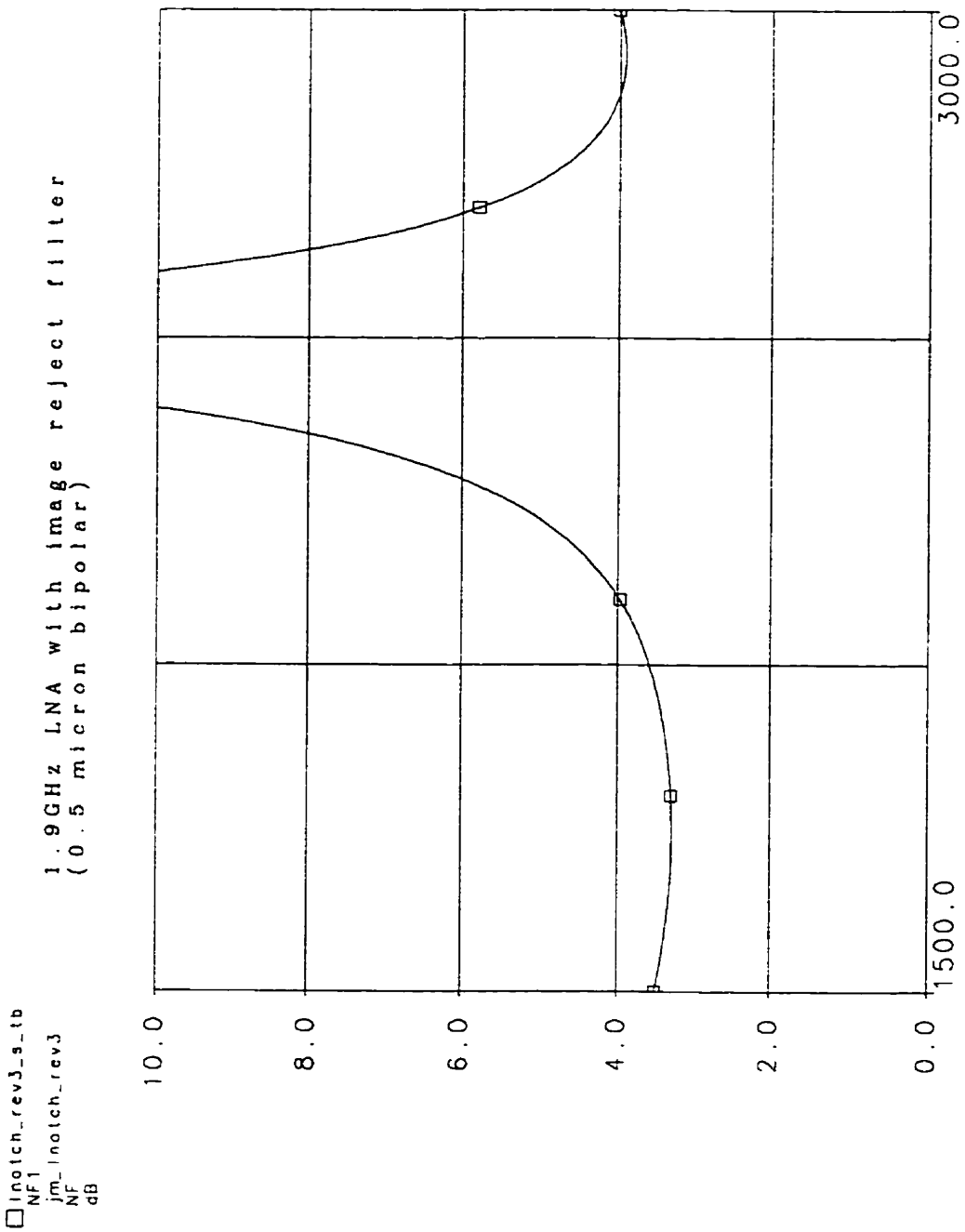

Figure 4-3: Simulated noise figure of LNA with image reject filter (unmatched) with passband at 1.9GHz and notch at 2.5GHz

The simulated noise figure versus frequency plot is shown in Fig.4-3 for the unmatched case also. The noise figure at the 1.9GHz passband is approximately 3.5dB. When the LNA with image filter was input matched the simulated noise figure reduced to 3.1dB and the passband gain became 26dB (the completed receiver front-end is tested with its input matched in chapter 6). Since the circuit exhibits substantial passband gain the mixer noise contribution will be greatly minimized, and a 3.1dB NF on the LNA with image filter could be sufficient to meet the sensitivity requirements of most cellular and cordless telephone standards.

As the plot of Figure 4-3 shows, the presence of the 2.5GHz notch tends to pull up the noise figure at the 1.9GHz passband. Thus it becomes apparent that a notch positioned at a higher frequency would result in a lower noise figure at the passband frequency. Thus the notch filter presented in this work is better suited for higher IFs such as the selected 300MHz IF or higher. This IF range is becoming more popular as progress is made in the available IF filters which are normally used after the downconversion mixer. For example good quality SAW filters at this frequency are readily available. Note that it is also possible to reduce the IF. In such a case the notch frequency would move closer to the passband frequency, thus degrading the passband noise figure (this is obvious from observing the noise curve of Figure 4-3).

Finally a two-tone simulation was done by applying two -40dBm tones at 1.9GHz and 1.89GHz and observing the output spectrum to evaluate the linearity at the passband. For the unmatched case the fundamentals at the output were at -16.5dBm and the third order intermodulation products were at -71.3dBm, from these values an input IP3 of -12.7dBm was calculated using formula (1.6). This input IP3 is higher than in table 4-1 because now inductor L_{e1} is modelled using an accurate high frequency 2π section lumped model and therefore due to self-resonance the actual inductance seen at the emitter at 1.9GHz is higher than 1.3nH thus providing more degeneration. Next the circuit was input matched with an external LC network and this time a -15dBm IIP3 was obtained.

The following table summarizes the above HPEESOF/Libra simulation results for the LNA with image reject filter with the filter tuned to reject a 2.5GHz image. Recall that these simulations are at the schematic level only and do not include any layout information.

Table 4-2: Simulations for LNA with image filter tuned for 2.5GHz

frequency	Gain	NF	IIP3	Input
1.9GHz	24.3dB	3.5dB	-12.7dBm	unmatched
1.9GHz	26dB	3.1dB	-15dBm	matched

The LNA with image rejection of Figure 4-1 was fabricated on a 0.5 micron bipolar process. Experimental on-wafer measurements will be shown in section 4.4 and beyond, but first let us analyze important issues such as noise at both the passband and the image frequency and linearity at the image frequency.

4.3.2 Noise Analysis

In this section we evaluate the output noise of the LNA with image rejection circuit at both the passband and the notch frequencies. Both bands are important as both are downconverted to the desired IF by the mixer that follows.

The simulated circuit is an extracted netlist with capacitive parasitics from the actual layout of an LNA with fixed image filter which has been fabricated (version jm_lnotch_rev5). The circuit is as in figure 4-1 but without the varactor. That is, R_4, C_7 and C_{var} were removed and replaced by a single 1pF capacitor. This was done because at the time no accurate varactor model was available. Thus, by having a circuit without a varactor the extracted circuit accurately represents the actual layout.

Simulations were carried on with HSPICE in order to observe the individual noise contributions of the various transistors in the circuit so as to uncover the most important contributors.

The table below shows the output noise contribution of four key transistors at the passband frequency (1.9GHz). The contribution of all the remaining components is not shown here for simplicity.

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Table 4-3: 1.9GHz Output noise analysis of LNA with image filter (V^2/Hz)

Element	Q_1 (LNA)	Q_2 (filter)	Q_4 (Cascode)	Q_3 (resonator)
rb	7.577e-18	7.470e-19	3.272e-18	6.490e-20
ib (shot)	7.431e-18	1.973e-18	7.986e-19	2.536e-20
ic (shot)	2.311e-17	1.799e-18	6.026e-18	7.301e-19
total	3.812e-17	4.52e-18	1.010e-17	8.203e-19

This table shows that in the passband the most important contributors (underlined) are the LNA transistor Q_1 and the cascode transistor Q_4, followed by the filter transistor Q_2. This is as expected, as the LNA is normally the dominant noise source.

For Q_1 its collector shot noise is the dominant contributor (generates 60% of Q_1 noise) followed by the thermal noise due to its base resistance (20% of Q_1 noise). This is because Q_1 is a large device and the base resistance is very small, approximately 2 Ohms. For the cascode the thermal noise due to its base resistance (32%) and the shot noise due to its collector current (59.6%) generate most of the noise. Hence, by increasing the size of the cascode its thermal noise contribution could be reduced to minimize overall noise. However, for the same bias current, this will reduce the device transit frequency which may not be desirable for gain and stability considerations. This is a design trade-off.

Table 4-4 shows the results of the output noise at the image (notch) frequency, which in this case is 2.62GHz.

Table 4-4 shows that at the notch frequency the noise contributions due to the LNA (Q_1) and the filter (Q_2) have been strongly suppressed (Q_1 noise has been reduced by 50dB and

Q_2 noise has been reduced by 45.8dB below the passband value) due to the presence of the notch resonator.

Table 4-4: 2.62GHz Output noise analysis of LNA with image filter (V^2/Hz)

Element	Q_1 (LNA)	Q_2 (filter)	Q_4 (Cascode)	Q_3 (resonator)
rb	7.036e-23	9.913e-24	1.320e-18	2.306e-19
ib (shot)	7.443e-23	3.770e-23	2.490e-20	1.339e-20
ic (shot)	2.629e-22	6.937e-23	1.647e-18	2.765e-18
total	4.077e-22	1.17e-22	2.991e-18	3.009e-18

Now the dominant noise contributors (underlined) are the cascode (Q_4) and the resonator transistor (Q_3). Observe that the cascode noise is smaller (-5.3dB) than what it was at the passband frequency, 1.9GHz. Once again the cascode noise originates mainly from its base resistance and its collector shot noise. Hence, it would appear useful to make the cascode as large as possible to minimize its thermal noise contribution.

The cascode base resistance noise is amplified by Q_4, which at the notch frequency is acting as a common emitter amplifier with a very low emitter impedance (the series resonator) and a tank (L_4, C_4) at its collector. Thus the gain from base to collector would tend to be high. However two factors will reduce this gain. First the resonator tank is tuned for 1.9GHz and its impedance at 2.62GHz will be in the order of -j75 ohms, i.e. 3 to 4 times smaller than what it was at 1.9GHz, second there is going to be a strong Miller effect due to the higher frequency of operation and finally the device is operating at a higher frequency and therefore its gain is reduced as well. The net result is that the base resistance output noise contribution is smaller than what it was at the passband frequency.

Finally, the table below shows the total output noise and the input referred noise at both the passband and the image frequencies.

Table 4-5: Total output noise of LNA with image filter

Frequency	Total output noise (V^2/Hz)	Total output noise (nV/sqrtHz)	Input referred (nV/sqrtHz)
1.9GHz	2.791e-16	16.7055	1.1705
2.62GHz	1.662e-17	4.0762	-------

This table clearly shows that due to the presence of the notch resonator the total output noise power at the 2.62GHz image frequency is 16.8 times (12.2dB) smaller than at the passband. This means that the image filter circuitry does not add undue noise at the image frequency. Such noise would of course add to the undesired image signal which is present in the input to the receiver.

4.3.3 Linearity analysis at the image frequency

It is important to evaluate how linear is the notch filter in the presence of interferers at the image frequency. The circuit linearity can be expressed in terms of the maximum current or voltage inputs which put the devices at the verge of nonlinearity.

The image filter operation can be viewed as a current cancellation approach (see for example equation 3.39 in section 3.2.4). For more clarity the circuit of Figure 4-1 has been repeated in Figure 4-4 with the relevant AC currents indicated in the circuit.

In Figure 4-4 the resonator generates a total current i_{s3} equal in amplitude but opposite in phase to i_{c2}. Thus the notch filter will be effective, provided i_{s3} can be made as large as i_{c2} thus cancelling it. Thus a smaller i_{c2} will require a smaller i_{s3}, alleviating the linearity requirements for transistor Q_3 at the image frequency.

The amplitude of i_{c2} for a given input voltage at the base of Q_2 will be limited by degeneration resistor R_2. A large R_2 reduces i_{c2} but introduces more noise in the circuit; hence this is a design trade-off. In this circuit R_2 is a 50 ohm resistor. The maximum peak

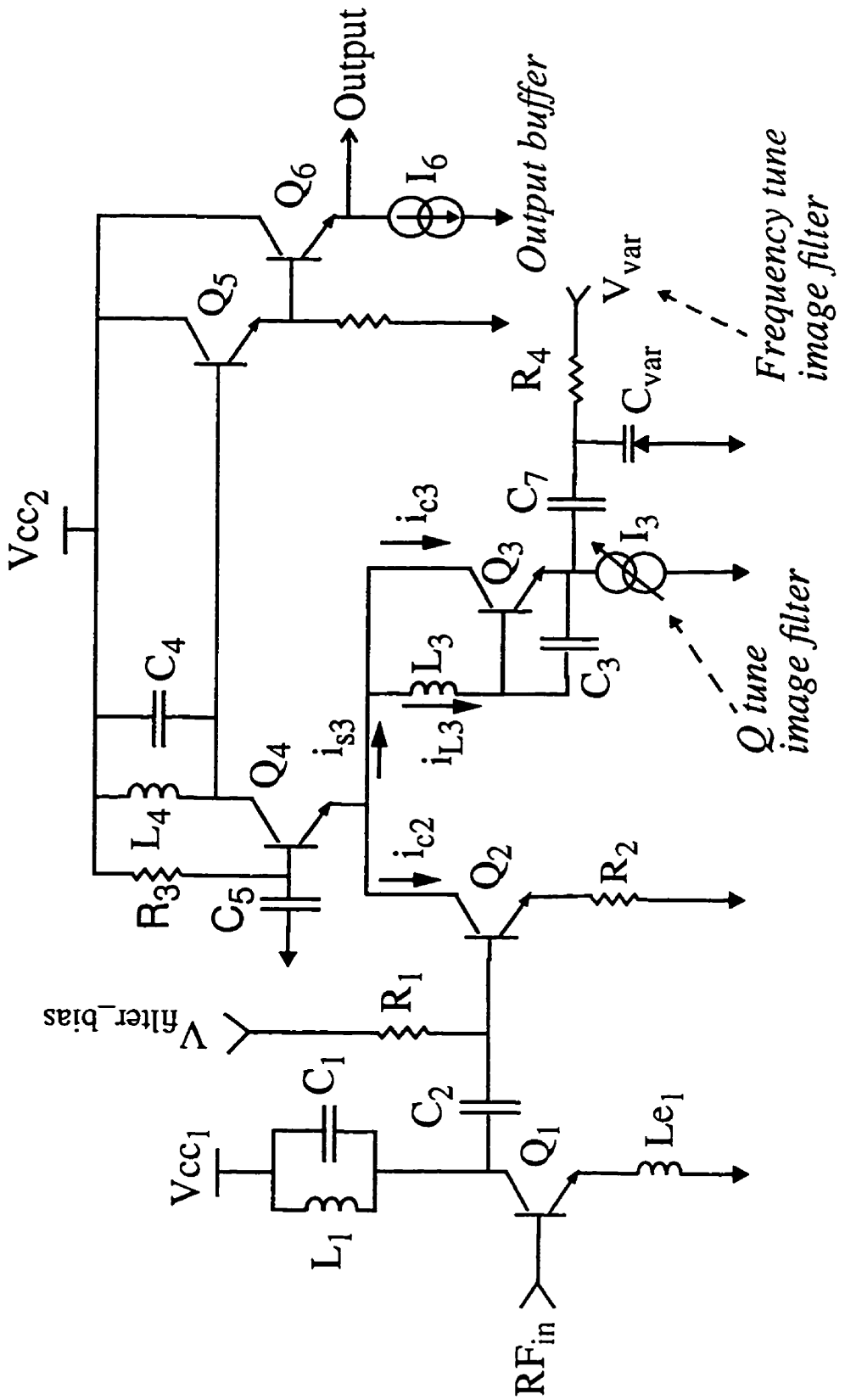

Figure 4-4: LNA with tunable image reject filter showing AC currents of interest

voltage at the base of Q_2 for linear operation of Q_2 can therefore be approximated as follows:

$$v_{b2_{linear}} = (R_2 + r_{e2}) \cdot I_{bias2} = (50\Omega + 10.4\Omega) \cdot 2.5mA = 151mV;peak \qquad (4.6)$$

where r_{e2} is the dynamic emitter resistance of Q_2. This limit applies for both the passband and the image frequencies. However, for the overall circuit, this maximum may or may not be attainable depending on whether the circuit that follows has sufficient linearity at the desired frequency of operation. For our circuit, at the image frequency, if the notch resonator was not able to sink sufficient current, that is i_{s3} could not be made as large as i_{c2}, then the linear limitation would originate on the resonator, that is on transistor Q_3 and not on transistor Q_2. Thus, for this circuit it is necessary to first evaluate how large can the current i_{s3} be, at the image frequency while maintaining Q_3 in the linear region. This is done in the following.

The enhanced resonator total input current i_{s3} consists of two components, i_{L3} and i_{c3}. Hence we must determine how large these currents can be while maintaining linear operation. Current i_{L3} and the reactances of the series resonator will determine the amplitude of the voltages at the base and at the emitter of transistor Q_3.

The base-emitter voltage for transistor Q_3 is directly dependent on i_{L3} and can be calculated as follows:

$$v_{be3} = i_{L3} \cdot \frac{1}{j\omega \cdot (C_3 + C_{\pi 3})} \qquad (4.7)$$

When V_{be3} is below 25mV the transistor Q_3 can be considered to be in its linear range of operation and when V_{be3} is above 25mV the transistor is entering the nonlinear region or beginning compression. Hence, for linear operation of Q_3 the following inequality holds:

$$\left| i_{L3} \cdot \frac{1}{j\omega \cdot (C_3 + C_{\pi 3})} \right| < 25mV;peak \qquad (4.8)$$

This particular circuit is realized with a 0.5 micron bipolar process. As a consequence $C_{\pi 3}$ was made much smaller than C_3 and hence C_3 became the key component to control the linearity at the image frequency. Equation (4.8) shows that a large current i_{L3} will require a large capacitance C_3 in order to maintain transistor Q_3 within its linear region.

Recall that the series resonant frequency (see equation (4.3)) depends on the series combination of C_3 and C_s (see formula 4.4). Hence, a larger C_3 requires a smaller C_s capacitance, that is, a smaller varactor capacitance (C_{var}), in order to maintain the series resonance at the desired 2.5GHz. A small C_s signifies a large emitter regeneration reactance, that is an increased feedback and therefore better linearity as expected. Hence, in the resonator circuit the AC voltage available at the base of Q_3 is split into 2 components, one small component across the base emitter junction and one large component from emitter to ground (across C_s). Thus, a large C_3 and a small C_{var} improve the linear range of Q_3 at the resonant frequency. However the varactor capacitance can not be made too small to maintain sufficient tuning range as well as to ensure reasonable tolerances due to process variation. Let us now briefly discuss the stability implications of adding C_3 and then we will continue with the linearity analysis.

A large C_3 significantly lowers the transit frequency ω_{T3} of the resonator transistor Q_3 while the cascode transit frequency can be very large. For the circuit of figure 4-4 the cascode Q_4 has a 40x0.5 micrometer emitter size and simulations indicate a 26.5GHz f_T for a 2.7mA bias current. On the other hand for the resonator C_3 is 2.5pF while $C_{\pi 3}$ was 0.141pF biased at 0.27mA which yields an effective resonator transit frequency of only 0.625GHz. Using these values in equation (3.72) shows that the fourth term of the right hand side of this equation becomes negligible and therefore the equation will yield a positive result and the circuit is stable. Therefore the presence of C_3 enhances stability. Be aware that in figure 4-4 the resonator is Q_3 and the cascode is Q_4 while in formula (3.72) the resonator was Q_2 and the cascode was Q_3. Now, let us go back to the linearity analysis.

As mentioned, for this work C_3 was selected as 2.5pF while $C_{\pi 3}$ was 0.141pF for transistor Q_3 with a 40 x 0.5 micron emitter size and a 0.27mA bias current. Therefore, replacing these values on the above inequality (4.8) indicates that i_{L3} must be less than 1mA peak for linear operation at 2.5GHz. To this value one must add current i_{c3} to determine the total resonator current i_{s3} at the verge of nonlinearity.

The 2.5GHz collector current i_{c3} can be calculated using formula (3.37), in which the total base emitter capacitance ($C_3 + C_{\pi 3}$) must be now used as follows:

$$i_{c3} = -j \cdot i_{L3} \cdot \frac{g_{m3}}{\omega \cdot (C_3 + C_{\pi 3})} = -j0.248 \cdot i_{L3} \tag{4.9}$$

Observe that the collector current of Q_3 is now only a quarter of the current through the inductor, hence the transit frequency of transistor Q_3 has been effectively reduced due to the presence of C_3. Now the total current into the resonator is

$$i_{s3} = i_{L3} + i_{c3} = i_{L3} - j0.248 \cdot i_{L3} = 1.03\angle -13.9° \cdot i_{L3} \tag{4.10}$$

Since the maximum i_{L3} for linear operation of transistor Q_3 at 2.5GHz is 1mA peak, then replacing this in the above equation (4.10) indicates that the maximum acceptable i_{s3} will be 1.03mA, peak which is then also the maximum acceptable i_{c2} for linear operation of Q_3

The corresponding maximum voltage at the base of Q_2 for linear operation of the resonator at the image frequency (2.5GHz) can then be approximated as follows.

$$v_{b2max} = i_{c2max} \cdot (R_2 + r_{e2}) = 1mA \cdot (50\Omega + 10.4\Omega) = 60mV;peak \tag{4.11}$$

Note that this value is smaller than $V_{b2linear}$ which was calculated in (4.6). Therefore this confirms that the linear range at the notch frequency is limited by the series resonator and not by Q_2. Observe also that a larger R_2 would increase the linear range at all frequencies, but is not desirable due to the increased noise. However, if an LC tank tuned for 2.5GHz was used instead of resistor R_2 (at the cost of additional device area), the linear range at the image frequency would be substantially increased without additional noise. Such a tank

would behave as a 250 ohm resistance at 2.5GHz thus substantially increasing the linearity of the circuit at the image frequency.

Finally, the maximum voltage at the LNA input for linear operation of the resonator at 2.5GHz is obtained by dividing the above V_{b2max} by the LNA gain at the notch frequency (2.5GHz). Since the LNA is tuned for 1.9GHz operation by means of the L_1 C_1 tank, its gain peaks at 1.9GHz, where the impedance of its collector tank reaches maximum and becomes purely resistive (it resonates). The tank impedance depends on the component values (L_1 and C_1) as well as on the Q of the inductor. For our circuit the inductor L_1 is approximately 4nH with a Q of 5 to 6 and the corresponding capacitor is 1.5pF. Hence, the equivalent resistance at resonance (1.9GHz) is in the order of 250 ohms. On the other hand the LNA emitter degeneration is approximately j18ohms, so the LNA provides substantial gain at the passband.

However, at frequencies beyond 1.9GHz the LNA emitter degeneration increases proportionally to the frequency of operation and at the same time the impedance of the collector tank (L_1, C_1) reduces substantially, because it is now dominated by the capacitor (C_1). For our circuit at 2.5GHz, C_1 has a reactance of -j42.4 ohms which is then in parallel with the inductor reactance of +j62.8ohms and also in parallel with the inductor dissipation resistor. This results in a total capacitive impedance of -j120 ohms, that is less than 1/2 the value at the passband resonance (1.9GHz). Additionally the emitter degeneration has now increased to +j23.5 ohms and finally the LNA transistor current gain has dropped proportionally with the increase in frequency. The net result is that, for this design, the LNA gain at the notch frequency (2.5GHz) is approximately 3 times smaller than at the passband (1.9GHz) and has a value of approximately 3 (based on simulations).

Hence, the maximum voltage at the LNA input for linear operation of the notch resonator at 2.5GHz is then:

$$v_{b1} = \frac{V_{b2max}}{LNAgain} = \frac{60mV;peak}{3} = 20mV;peak \Leftrightarrow -30dBm \qquad (4.12)$$

Thus, for this circuit the notch filter enters the nonlinear region when 2.5GHz signals larger than -30dBm are fed to the LNA input. This is a reasonable linear range for the notch filter considering that a bandpass filter normally precedes the LNA and provides additional image rejection, in the order of 30dB, thus alleviating the linearity requirements by the same amount. Observe however, that the filter continues working for larger signals but with diminished rejection.

4.4 Measurements of LNA with tunable image reject filter

This section reports on the on-wafer measurements of the LNA with tunable image rejection (schematic in Figure 4-4). The chip was not input matched. These measurements were carried out on an Analytic probe station using an HP8753C Network Analyzer and microwave RF probes to contact the chip pads. An off-chip "bias T" network was connected to the RF input to bias transistor Q_1 to 3mA. The network analyzer, including the "bias T" network, was properly calibrated before the measurement. V_{cc1} and V_{cc2} were fed with separate probes which connected to the same 3V DC supply. Transistor Q_2 was biased to 2.5mA by applying a DC voltage (V_{filter_bias}) to resistor R_1 which also serves as RF choke. The notch frequency is centered by means of the DC control voltage V_{var} which varies the capacitance of the on-chip varactor and changes the frequency of the notch resonator according to equations 4.3 and 4.4.

The measured forward transmission coefficients (S21) are shown in Figure 4-5 corresponding to the chip designated as E3. These plots show a substantial passband gain of 25.083dB at 1.9GHz which agrees very well with the simulation of section 4.3.1 (24dB in Figure 4-2). No spurious poles or oscillatory tendencies were observed. Two frequency responses have been superimposed in the same plot.

The first response show in figure 4-5 was obtained by applying a 0V varactor voltage and then adjusting current source I_3 to obtain a deep notch located at 2.336GHz (indicated by cursor 2) with -33dB loss for a total rejection of 58.083dB.

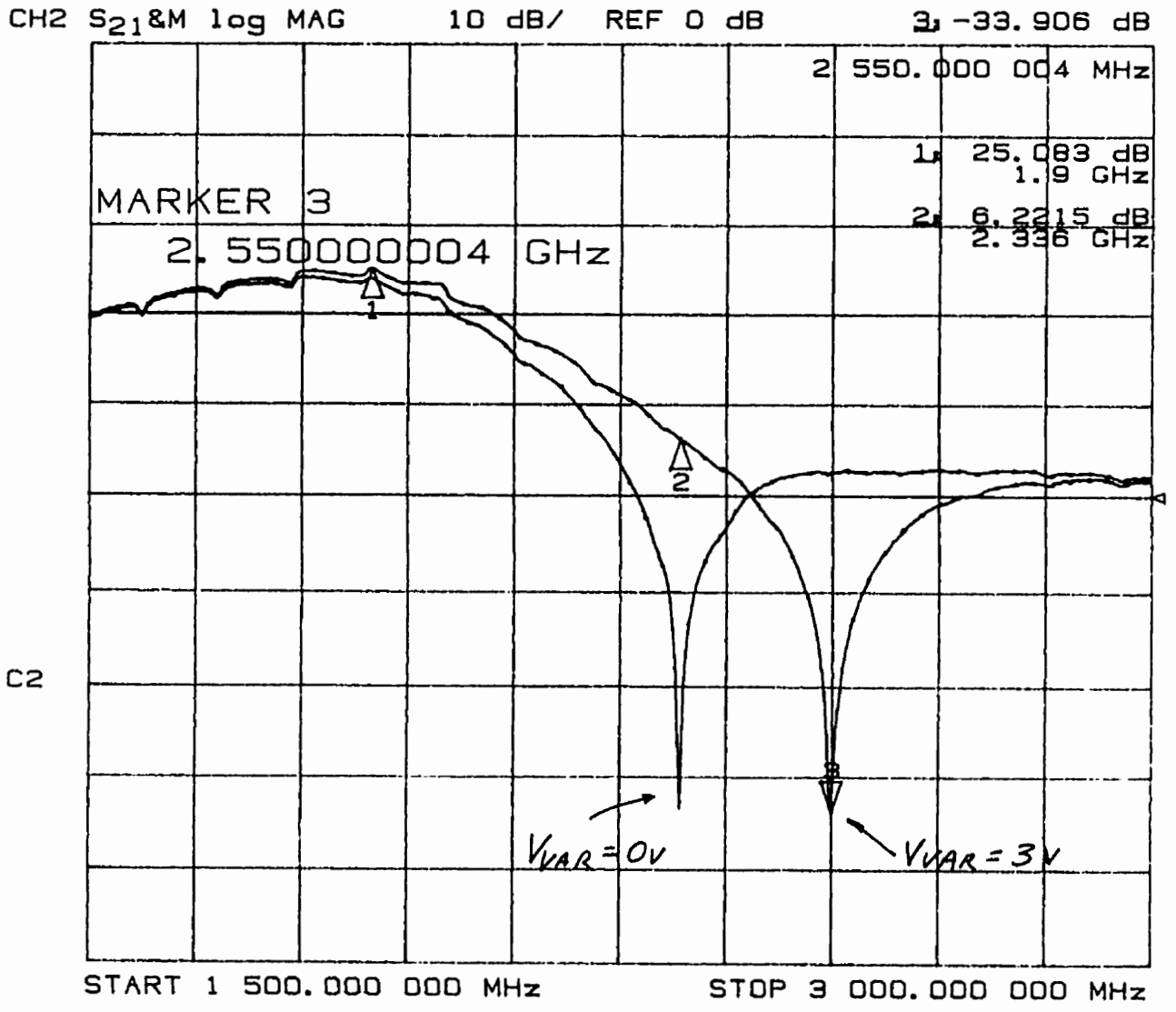

Figure 4-5: Measured forward transmission coefficient (S21) of LNA with tunable image reject filter without input matching. Fabrication batch 2. (0.5 micron bipolar)

The second response was obtained increasing the varactor voltage to 3V and shows the notch now at 2.550GHz and with a loss of -33.906dB (indicated by cursor 3) for a total rejection of 58.98dB. Detailed curves of the notch frequency versus varactor voltage are shown in section 4.5.

When the notch is at the higher end (2.55GHz) it can be seen that the passband gain increases a little between 0.5 to 1dB, due to the fact that the zero has less influence on the passband pole. This increase in gain also improves the noise figure. This illustrates how an image frequency further away from the passband would yield a better noise figure.

The noise figure and linearity of an unmatched LNA with the image filter tuned for 2.5GHz were also measured on-wafer. The noise figure measured with an HP8970 meter was 4.4dB which is higher than the simulated value of 3.5dB indicated in Table 4-2. The reason for this discrepancy is partly experimental as it is difficult to ensure a very good contact between the probes and the chip pads on the wafer, thus the noise figure may be degraded with a poor contact.

To measure the input IP3 two tones at 1.89GHz and 1.9GHz both with -40dBm amplitude were applied to the circuit and the fundamental and third order intermodulation products measured, resulting in a -12.5dBm input IP3 which agrees quite well with the simulated value of Table 4-2.

Thus, these measurements confirmed that the LNA with image reject filter worked well, and was stable and with excellent passband gain and a deep notch which could be tuned from 2.336GHz to 2.550GHz by adjusting the varactor control voltage from 0 to 3V. The measured noise figure, although higher than simulation, was sufficiently low to indicate that the GSM requirement could be met. Finally the linearity was also sufficient to aim at meeting the GSM requirement.

More detailed measurements of the notch tuning frequency are shown in section 4.5.

4.5 Measurements of notch frequency tuning range

This section presents the measured tuning range for the notch frequency of the LNA with tunable image reject filter of Figure 4-4. In this circuit the plus side of the varactor is grounded and the minus side is connected to V_{var} through R_4, hence the full amount of the V_{var} control voltage reverse biases the varactor, ensuring the largest possible tuning range, i.e. from 0 to 3V. Recall also that the varactor capacitance dominates equation 4.3 as well as 4.4 and hence is the major factor in defining the notch resonant frequency.

It is necessary to measure the notch frequency tuning range when V_{var} is varied from 0 to 3V so as to evaluate if it is sufficient to compensate for process variations. It is also important to have an indication of how sensitive the notch frequency is to small changes on the control voltage.

The notch tuning range measurements presented here were made on-wafer and for two different fabrication runs (batch 1 and batch 2).

Three chips were measured in the same wafer from fabrication batch 2. The forward transmission coefficient (S_{21}) of the LNA with image rejection was measured with an HP8753C network analyzer as explained in section 4.4. Then V_{var} was varied in steps from 0 to 3V and the frequency of the notch in the S_{21} response recorded. The varactor control voltage versus the notch frequency was then plotted as shown in Figure 4-6. This figure shows a 200MHz notch frequency tuning range from 2.35GHz to 2.55GHz, corresponding to a 0V and 3V control voltage respectively. These tuning curves show excellent agreement for the three measured chips.

Another wafer fabricated in a previous batch (batch 1) was also measured and for that case the tuning range was from 2.44GHz to 2.67GHz (230MHz tuning range). This clearly indicates that, due to process variation, the tuning range will vary for wafers fabricated in different production runs.

The positive result is that for both batches we were able to precisely center the notch filter for the desired 2.5GHz image frequency.

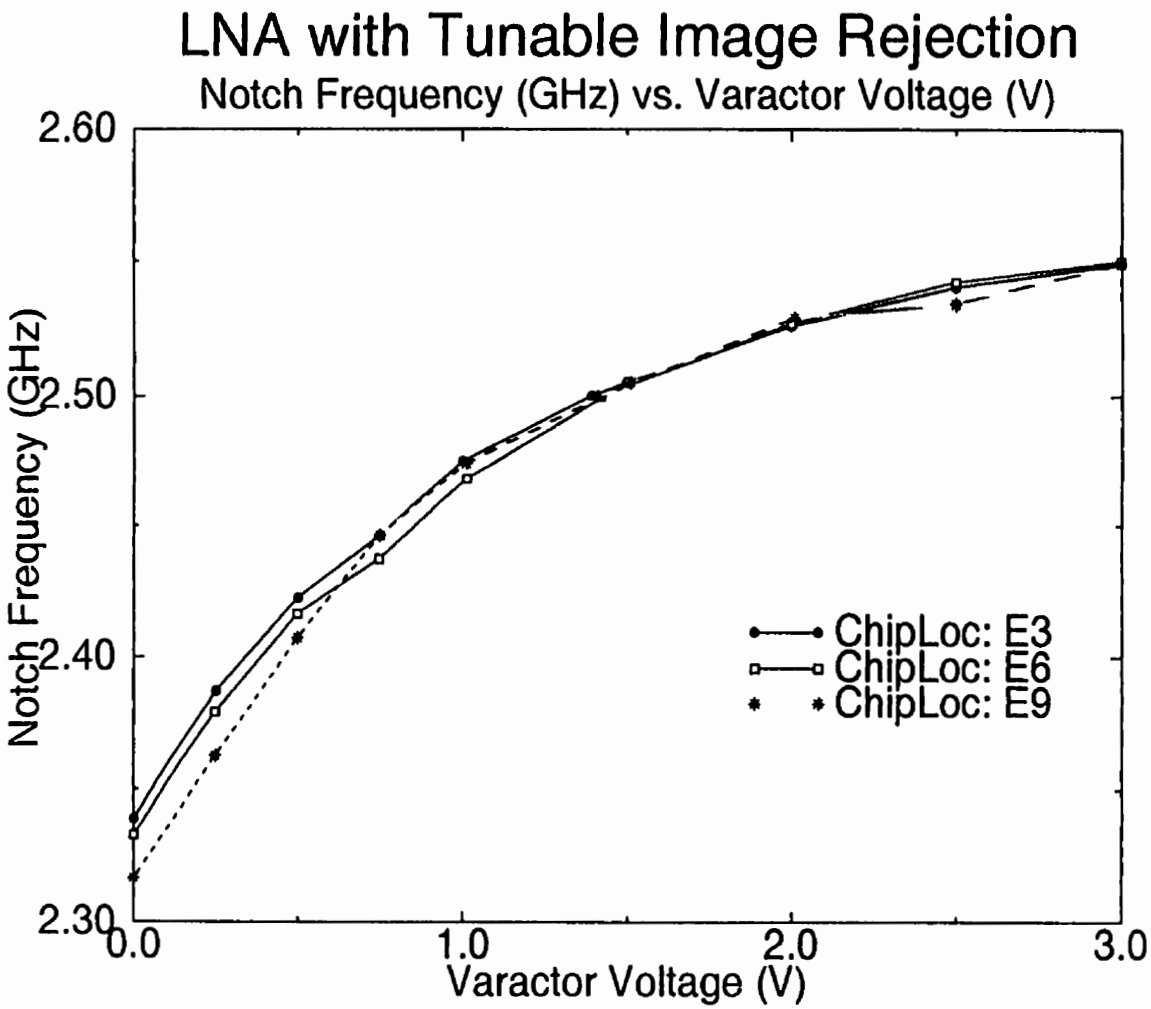

Figure 4-6: Measured notch frequency tuning range for LNA with image rejection (batch 2)

Note also that the tuning curve has a higher slope when the control voltage varies from 0 to 1V, indicating that this covers most of the tuning range.

Measuring the slope of the tuning curve for various varactor control voltage points (from Figure 4-6) yields the following table.

Table 4-6: Notch frequency tuning sensitivity (batch 2)

Varactor voltage	Notch frequency	Slope
0 to 0.5V	----------	177MHz/Volt
1V	2.475GHz	97MHz/Volt
1.4V	2.500GHz	54MHz/Volt
2V	2.525GHz	35MHz/Volt

As this table shows the sensitivity of the notch frequency with respect to the control voltage depends on the value of the control voltage itself. Clearly, the sensitivity is higher for small control voltages. This is due to the nonlinear capacitance versus bias voltage characteristic of the varactor diode.

In Table 4-6 for the nominal 2.5GHz notch frequency the corresponding control voltage is 1.4V with a sensitivity of 54MHz/Volt. Hence if the control voltage varies by 1% (that is, 14mV) the notch frequency would move by 0.75MHz, which would not significantly degrade the notch depth, as will be shown in the measurements of chapter 6 (see sections 6.3.2 and 6.3.4). It should be possible to design circuitry to maintain the varactor control voltage within 1% or 2% of its adjusted value, thus keeping the notch frequency within 0.5 to 1MHz of its desired value.

Hence, these measurements indicate that the notch tuning sensitivity is adequate assuming that the varactor control voltage can be kept within a few percent of its optimal value in order to minimize notch frequency shifts.

4.6 Layout and testing issues

A micrograph of the circuit layout in Nortel's 0.5 micron bipolar process is shown in Figure 4-7 (see schematic in Figure 4-1 or 4-4). The LNA covers the upper half of the chip and the tunable image filter the lower half. In the upper half, the small inductor to the left is the 1.3nH emitter degeneration inductor (L_{e1}) and the one to the right is the 3.5nH inductor (L_1) which forms part of the LNA LC tank. In the lower half the inductor to the left (L_3) is the notch series resonator while the inductor to the right (L_4) is the cascode LC tank. The RF input can be seen on the top and the output is at the bottom. The circuit was laid out with pads suitable for both wafer probing and wirebonding if required. Pads were carefully positioned to minimize crosstalk, especially from output to input.

Multiple ground pads were used throughout, thus minimizing the total inductance to ground. The inductors were laid out using 2 micron top metal for best Q. The capacitors were Metal-Insulator-Metal (MIM) which provide excellent quality factor (in the order of 20 to 30). The supply lines for the LNA and the filter were separated to avoid feedback from the filter output back to the LNA which could cause undesired oscillation, and so separate pads were used for V_{cc1} and V_{cc2} (see schematic in Figure 4-1 or 4-4).

Once the layout was completed a netlist extraction with capacitive parasitics was performed. This netlist was then simulated with HSPICE to verify the frequency response of the circuit before fabrication. The discrepancy between simulation and measurement of the passband and the notch frequencies is examined in section 4.7.

Test structures for some key components of the circuit such as capacitors, varactor, inductors and resistors were laid out for verification purposes.

The frequency response of the LNA with notch filter as well as the test structures were tested on-wafer an analytic station using 50 Ohm microwave probes and a HP8753C network analyzer. Measurements included noise figure and a two-tone measurement to obtain the Third Order Intercept Point (IP3). These results compared well with the simulation results.

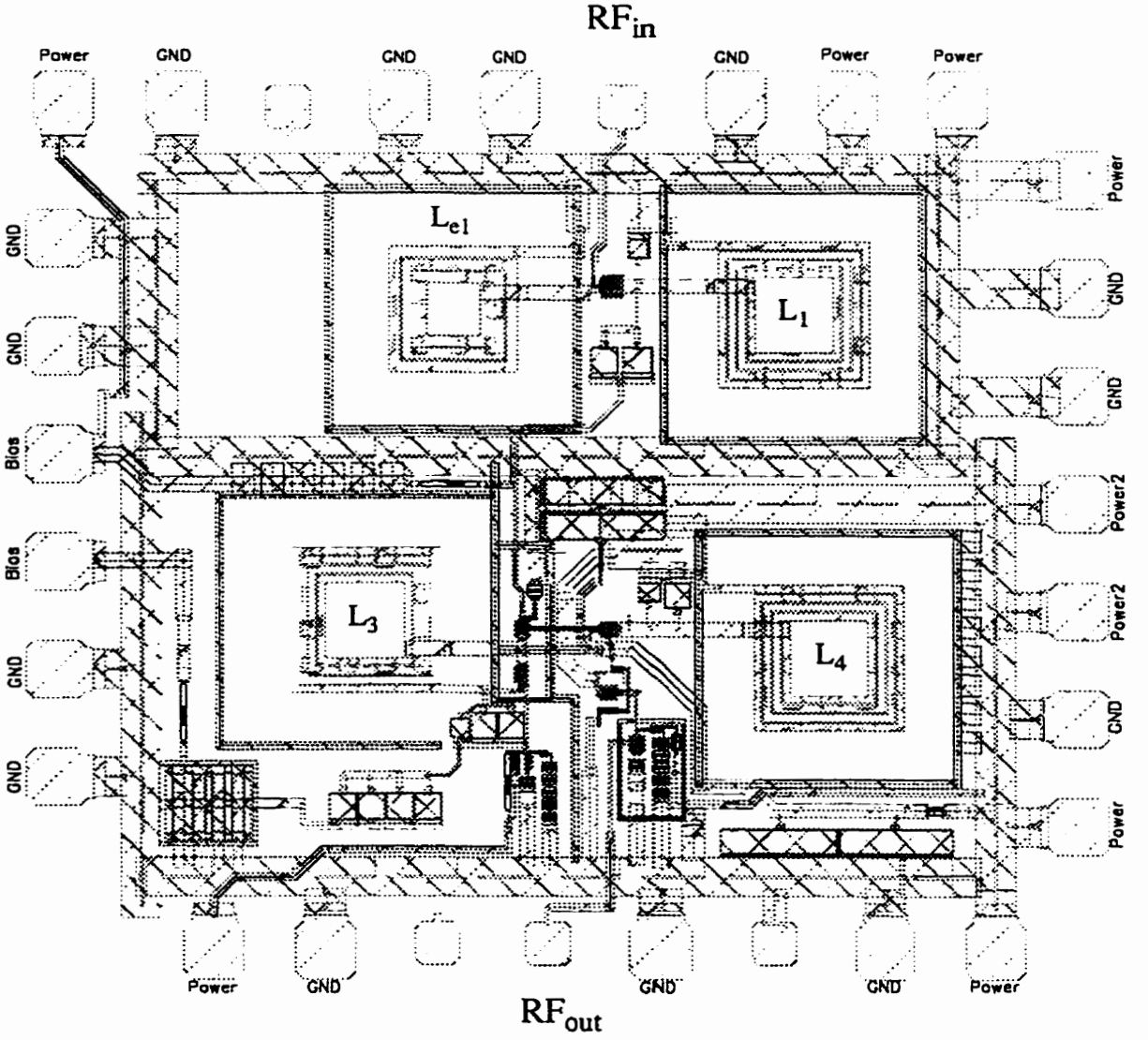

Figure 4-7: Micrograph of LNA with tunable image reject filter (0.5 micron bipolar)

The circuit was not input matched because this is difficult to do on-wafer. It is possible to input match the circuit on a packaged device but this was not considered of fundamental importance at this point of the research. Note that the off-chip input matching network was added later when testing the completed receiver front-end (results are shown in sections 6.3.2 and 7.1.2.1).

Since the filter is now tunable by means of a varactor, the tuning range of the notch frequency was also measured with the results were shown in section 4.5.

Additionally the key components of the circuit, namely inductors and capacitors, varactor and resistors were satisfactory tested confirming that their values were within expectation The measured results for a 3.5nH inductor are described at the end of the following section.

4.7 Accurate simulation versus measurements

This section presents accurate frequency response (S21) simulation results which are then compared with a comprehensive set of measurements to evaluate the simulation accuracy and to validate the models used. The circuit netlist was extracted from the layout including capacitive parasitics and relevant inductive parasitics were later added by hand.

To this purpose an LNA with fixed image reject filter shown in Figure 4-8 is studied here (version jm_lnotch_rev5 corresponding to fabrication batch number 2). This circuit is essentially the same circuit as in Figure 4-1 but without the varactor. Components R_7, C_7 and C_{var} were removed and replaced by a single 1pF capacitor (C_6). A fixed notch frequency was preferred for this experiment for simplicity (simpler test) and to avoid the additional inaccuracies introduced by the varactor model which at the time of this work was not very accurate. (The varactor used in this work was custom made and is not a standard part in the NORTEL's NT25 library. It is difficult to accurately model the varactor losses and find the Q. Hence to characterize the varactor we relied on experimentation. Test structures of the varactor diode were measured to accurately obtain the capacitance and the Q and then these values were used for the simulation when necessary).

In the layout of this circuit, the connections to the inductors have a length in the order of 100 microns and this can add inductance in the order of 0.1nH, which will affect the LC

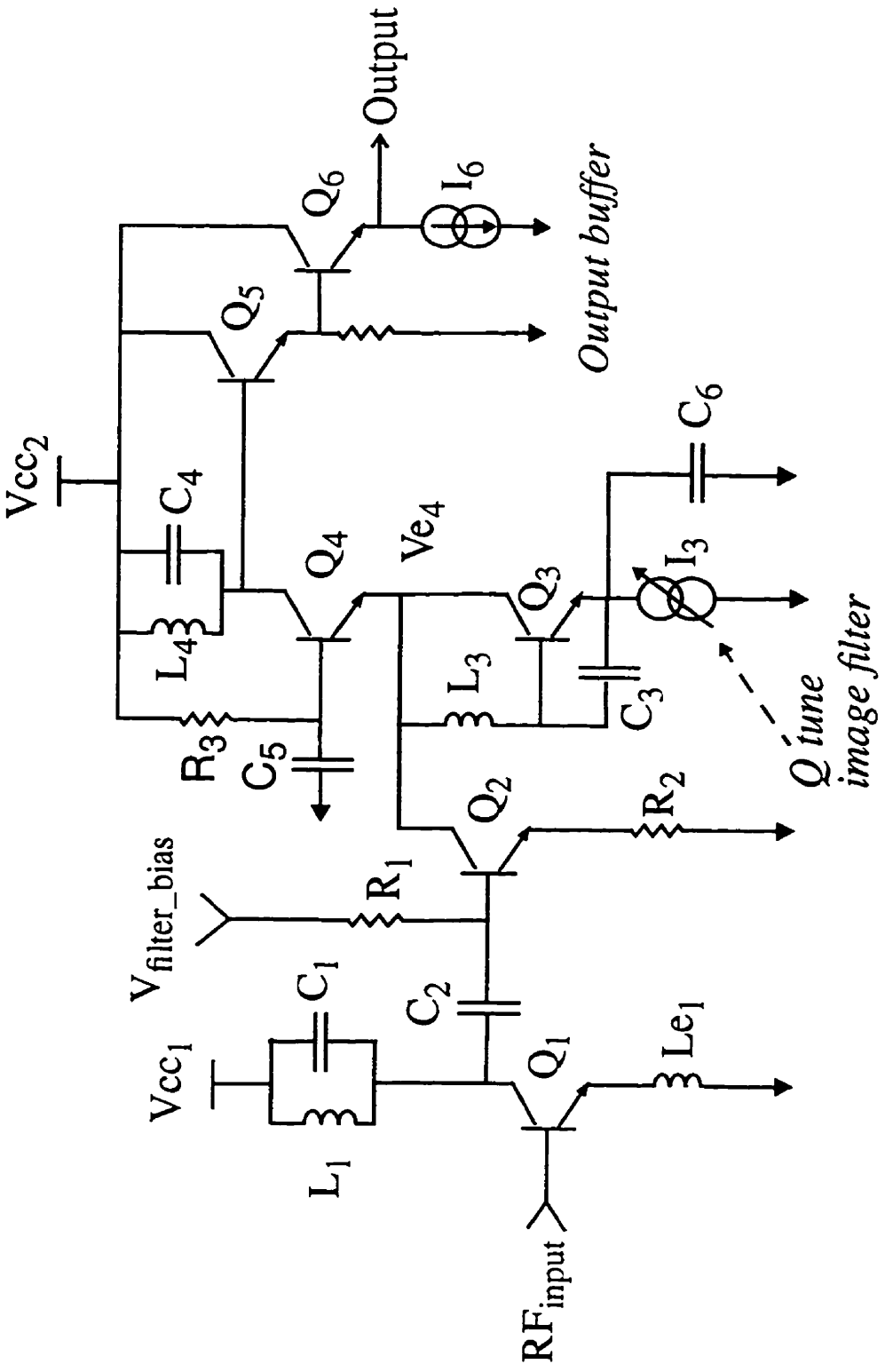

Figure 4-8: LNA with fixed image reject filter (jm_lnotch_rev5)

resonant frequencies. For example the on-chip connections to the emitter degeneration inductor L_{e1} add an additional 0.1nH and the inductor self-resonance further increases the effective inductance a little more. Thus the emitter inductor effectively increases to approximately 1.5nH (at 1.9GHz). This increase in inductance will degrade the gain and noise figure but will also improve stability a little. For the series resonator the connections to inductor L_3 will increase the actual inductance and therefore lower the series resonant frequency. Hence, it is important to properly model the inductor connections.

Unfortunately, at this time, the layout extractor can include only capacitive parasitics. Hence two simulations were done, the first one with the extracted netlist with capacitive parasitics only and the second one with the inductor connections modelled as short transmission lines and then added, by hand, to the extracted netlist to then proceed with a more accurate simulation. Note also that simulations can be done with typical, worse and best case models. For this analysis only typical simulations were included with the results shown in the table below.

Table 4-7: HSPICE simulations of LNA with fixed image filter

Parasitics included	**Passband frequency**	**Passband Gain**	**Notch frequency**
capacitive only	2.0GHz	24.9dB	2.620GHz
capacitive + inductive	2.0GHz	24.4dB	2.580GHz

This table shows that when inductive parasitics were added the notch frequency was reduced by 40MHz (1.6%). Hence, for our operating frequencies (1.9GHz to 2.5GHz) the connections to the inductors do slow down the circuit response and it is important to include them for a more accurate prediction. Note that in Table 4-7 both the simulated passband and stopband frequencies are higher than the desired values (1.9GHz and 2.5GHz respectively), but as will be shown by the actual measurements it seems appropriate to "overdesign" the frequencies involved to compensate for the modelling and fabrication errors.

The following table (4-8) shows the results of a comprehensive set of measurements carried on a wafer corresponding to fabrication batch 2.

Table 4-8: Measurements of LNA with fixed image filter (batch 2/ wafer #1 in 0.5 micron bipolar)

Chip#	Passband frequency	Passband Gain	Notch frequency	Measured notch frequency as % of simulation
E6	1.85GHz	23.2dB	2.479GHz	96.1%
E3	1.90GHz	24.1dB	2.490GHz	96.5%
E9	1.89GHz	23.6dB	2.490GHz	96.5%
B9	1.84GHz	24.2dB	2.490GHz	96.5%
B6	1.90GHz	24.3dB	2.490GHz	96.5%
B3	1.84GHz	24.9dB	2.481GHz	96.2%
H3	1.90GHz	24.5dB	2.481GHz	96.2%
H6	1.86GHz	24.2dB	2.481GHz	96.2%
H9	1.86GHz	22.9dB	2.450GHz	95.0%
AVG.	1.87GHz	23.99dB	2.481GHz	96.2%

The 9 tested chips were carefully selected to cover the whole wafer area as shown in Figure 4-9. The circuits were not input matched as this cannot easily be done on-wafer. A "bias T" network was used at the RF input to bias transistor Q_1 with a 3mA current. The filter (Q_2) was then biased with a 2.5mA current and following this the frequency response was observed with the Network Analyzer which had been previously calibrated. Next the voltage which controls current source I_3 was adjusted so as to obtain a deep notch in the frequency response. Typically a 0.5mA tuning current (I_3) was required. Then both the passband and notch frequencies were recorded as well as the passband gain.

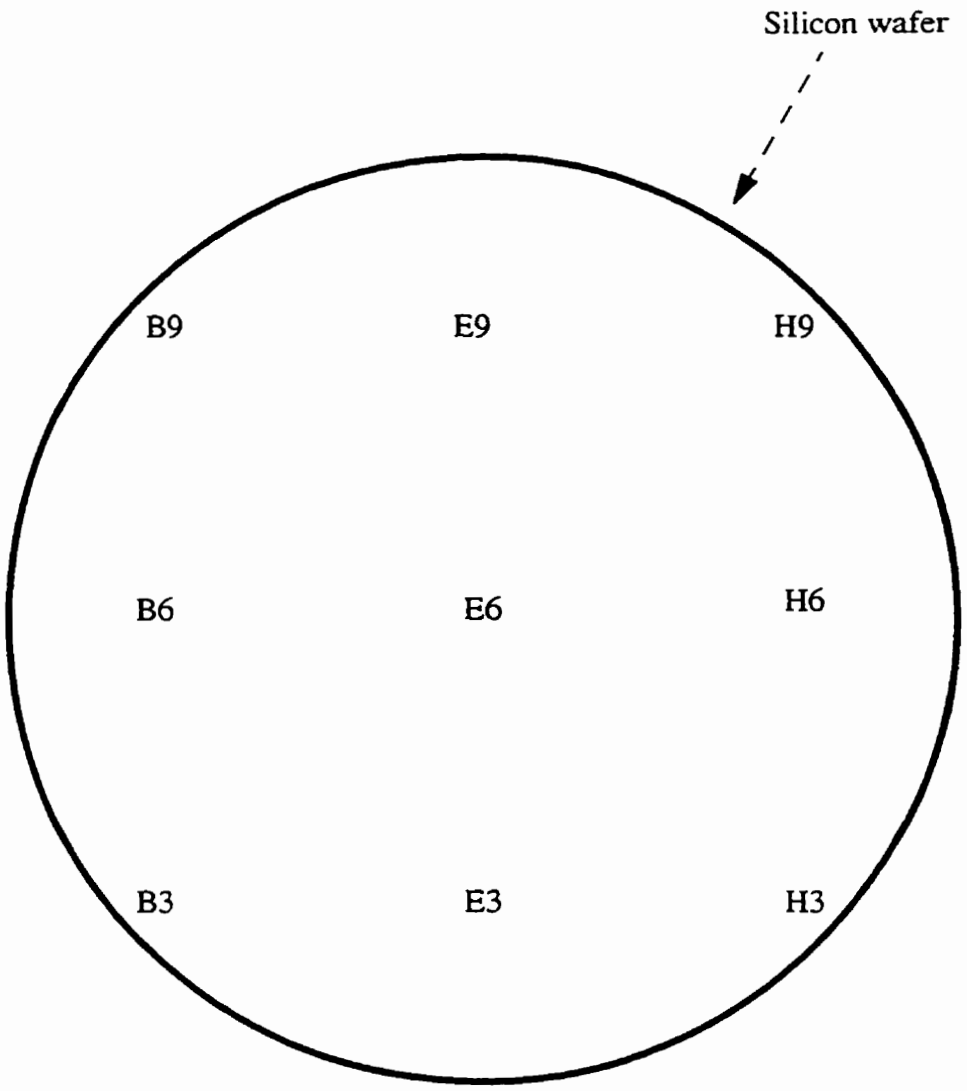

Figure 4-9: Location of measured LNA with fixed image reject filter chips (batch 2)

This procedure was repeated for the 9 chips and the results are summarized in table 4-8 in which the rightmost column shows the measured notch frequency as a percent of the most accurate simulated value (2.58GHz as was shown in Table 4-7).

As the table 4-8 shows the measured notch frequency error is on average within 3.8% of the simulated notch frequency (2.58GHz) obtained when both capacitive and inductive parasitics were included in the simulation. Considering the very high frequency of operation we see that there is excellent agreement between measurement and simulation. In Table 4-8 observe also that the average measured notch frequency is only 0.8% (19MHz) away from the desired value, which is 2.5GHz. All the measured chips show notch frequencies very close to each other demonstrating the good quality of the process.

These results demonstrate the high quality of the bipolar process used here and validate the models used for the simulation. However, these measurements also indicate the need for a tuning mechanism required to bring the notch frequency precisely to the desired value, which in this case is 2.5GHz. This is the role of the tuning varactor (C_{var}) shown previously in the schematic of Figure 4-1 or Figure 4-4.

Neglecting the measurement error (because the Network Analyzer was properly calibrated) this 3.8% discrepancy can be attributed mostly to component tolerances as well as inaccuracies in the models. In this circuit the inductor and capacitors are the crucial components which determine the resonant frequencies at both the passband and notch frequencies. For example, for the notch frequency the inductor L_3 and capacitors C_3 and C_6 are the dominant components and therefore their tolerances will largely determine the manufacturing error.

The tolerance of the MIM capacitors used in this integrated circuit is +/-20% although all our measurements indicate a tighter tolerance. On the other hand the inductors are very repeatable, that is, their tolerance is small. Various inductor measurements on different wafers show excellent agreement. This confirms Long's observations [47]. However, the inductor model is not fully accurate and this error will generate a discrepancy between simulation and measurement.

From our measurements the inductor model error can be estimated to be in the order of 5%. Our inductance measurements consistently show a higher value than the one indicated by the lumped model. For example, the table below summarizes the simulation results of a nominal 3.5nH inductor fabricated in NT25.

Table 4-9: Simulated values for a 3.5nH inductor

Frequency	L	R	Q
1.9GHz	3.62nH	4.72ohm	9.1
2.5GHz	3.68nH	5.9ohm	9.8

These simulations were done with HPEESOF's Libra and using the inductor high frequency lumped model available in the NT25 library. Observe that at 2.5GHz the 3.68nH simulated value is higher than the nominal value of 3.5nH. This is due to the self-resonance which at high frequencies (but below the self-resonance frequency) effectively increases the inductance.

The table below summarizes the measured results.

Table 4-10: Measured values for a 3.5nH inductor

Frequency	L	R	Q
1.9GHz	3.84nH	7.29ohm	6.3
2.5GHz	3.94nH	9.97ohm	6.2

As shown in these results the measured Q is lower than predicted by the simulation, possibly due to inaccuracies in the substrate parameters, or due to the skin effect.

These measurements were done on-wafer and with RF probes. Observe that at 1.9GHz the measured inductance is 6.1% higher than the simulation value and at 2.5GHz it is 7.1% higher than the simulation value. At 2.5GHz the measured inductance is 0.26nH higher

than the simulated value. This excess is partly due to the connections to the inductor (which are not part of the lumped model), which we estimate at approximately 0.1nH because their length is in the order of 100micron. If we discount this value the measured inductance would be 3.84nH, that is, 4.3% higher than the simulation. This suggests to us that the model inaccuracy would be in the order of 5%. Since the frequency of resonance is inversely proportional to the square root of L, this error would introduce a frequency error of 3%, which is consistent with the results of Table 4-8. This also indicates that the capacitor values were very close to the design value.

Hence, the connections to the inductor add additional inductance which cannot be neglected at high frequencies. The inductor model must be able to correctly represent the inductor at low frequency as well as high frequencies. Any error in the modelling of the low frequency inductance (the inductor nominal value) will show up also at high frequencies. The effect of the self-resonance will show properly provided the lumped model satisfactorily represents the parasitic capacitances involved.

Chapter 5 Monolithic RF mixers

The RF mixer in a radio receiver is a fundamental block which allows superheterodyning to take place. A mixer is essentially an analog multiplier which downconverts the received signal from the RF band to an intermediate frequency, or directly to the baseband for demodulation or detection.

There is a wealth of information written about mixers [23] [48][49] [50] so this is only a brief review of some key points. A mixer is typically a noisy circuit, and for this reason, when used in a receiver front-end, an LNA with sufficient gain to ensure overall low noise is placed in front of the mixer. However, precisely because of the LNA gain, the signals entering the mixer have been amplified and thus the mixer non-linearity becomes the limiting factor on the receiver ability to handle large signals. Hence, for a receiver front-end application highly linear mixers are typically needed.

Mixers can be unbalanced or balanced. A double balanced mixer has both the RF and LO inputs applied to separate ports in differential fashion so that neither signal appears at the other two ports, that is, the LO signal does not appear at the RF or IF ports and so forth. These circuits generally require accurate matching of the active devices [49]. In general, balanced mixers are preferred because they ensure superior isolation over the single ended versions. Thus in a monolithic implementation a balanced mixer is more attractive and only balanced mixers are used in this work.

5.1 Mixer performance

Mixer performance is measured with various figures of merit, the most important of which are described below.

Conversion Gain is the ratio of the output (IF) signal power to the (RF) input signal power.

Isolation represents the amount of "leakage" or "feedthrough" between the mixer ports. The LO-IF isolation is the amount that the LO signal is attenuated when measured at the IF port. The RF-IF isolation is the amount that the RF signal is attenuated when measured at the IF output port. Finally the LO-RF isolation is the amount that the LO is attenuated

when measured at the RF input. This is specially important in receiver applications where it is not desirable to radiate the LO frequency to neighbouring receivers.

Two-tone, third-order intermodulation distortion is the amount of third order distortion caused by the presence of a second received signal at the RF port. Mathematically, third-order distortion is defined in terms of the frequency component at $2f_2$-f_1+/-f_0, where f_1 is the desired RF input signal and f_2 is a second RF input signal. Usually the higher the intercept point of a mixer the greater will be the suppression of this product.

Third Order Intercept Point (IP3) is the point at which the fundamental response at the IF and the third-order spurious response curves intersect. It is often used to specify the two-tone, third order suppression of a mixer. It is particularly important that a mixer exhibits high IP3 because the RF signals arriving into it have been substantially amplified by the LNA (and the image reject filter in a monolithic implementation). IP3 can be referred to either of the RF input or IF output of the mixer, through the conversion gain. The normal practice is to use input referred IP3 (IIP3).

5.2 Gilbert cell mixer

Generally a Gilbert cell mixer [48] is the preferred choice for monolithic implementation. A typical conventional Gilbert cell is shown in Figure 5-1 below. The mixer consists of an input differential pair (Q_1, Q_2) with emitter degeneration (R_1) and a quad of switching transistors (Q_3, Q_4, Q_5 and Q_6). Capacitor C_2 is required to AC ground one input of the differential pair, so as to convert the single ended RF at the other input into a differential signal at the differential pair outputs. Transistors Q_7 and Q_8 act as current sources whose current can be adjusted by varying V_{bias}. Resistor R_{lo} is an on-chip 100 ohm resistor which provides matching to an off-chip differential local oscillator.

The IF available at the quad collectors of Q_3, Q_4, Q_5 and Q_6 can be extracted as single ended or differential. A differential output will cancel even harmonics as well as common mode signals such as RF leakage and would theoretically add 6dB gain to the desired IF output signal. To test the differential IF output an external balun (balanced to unbalanced

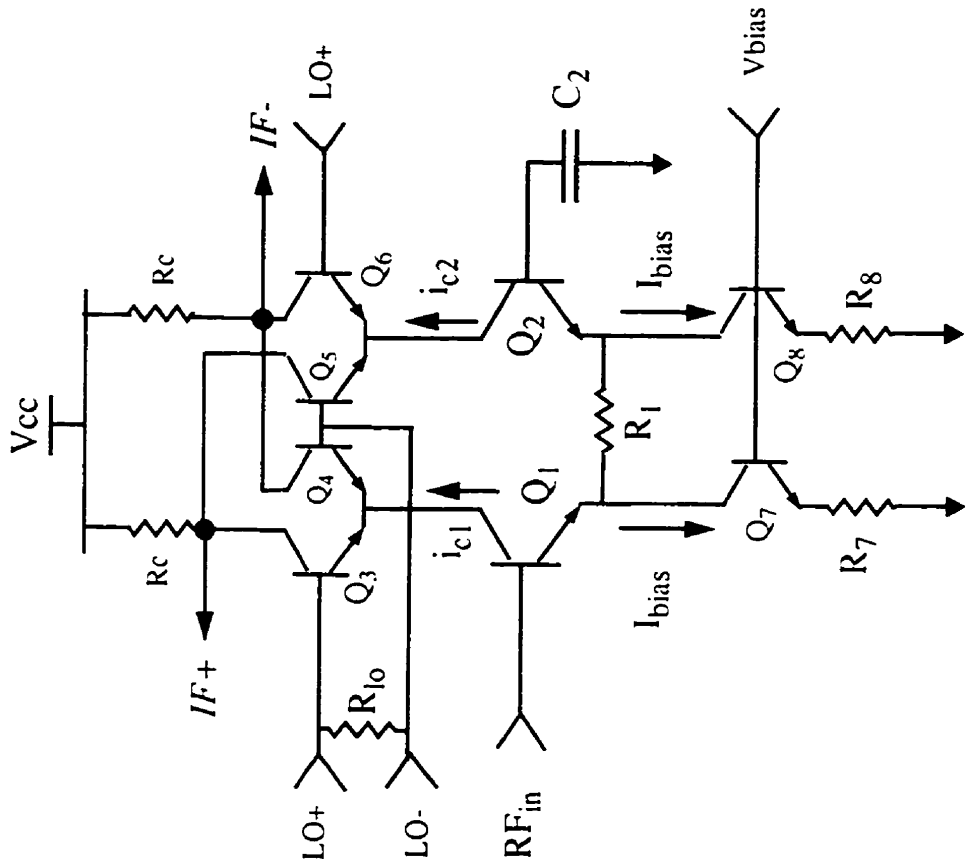

Figure 5-1: A conventional Gilbert cell balanced mixer

transformer) would be connected to IF^+ and IF^- to convert the differential signal back to a single ended output. The balun is required because the measurement instruments are typically single ended. A typical noise figure meter, for example, measures only single ended IF. On the other hand if a single ended IF is used, for example IF^- only, then no balun is required, thus simplifying the testing, specially on-wafer testing.

5.2.1 Mixer noise

For the input pair (Q_1, Q_2), large transistors will ensure lower noise due to reduced base resistance, but sufficient f_T must be provided to obtain acceptable gain. Careful selection of the emitter area and bias current for the transistors in the switching quad is required in order to achieve a good noise figure [5]. The quad transistors cannot be made too large because they must have sufficient f_T to ensure fast switching at the desired frequency of operation.

5.2.2 Mixer conversion gain

The conversion gain is determined by the resistor load (R_c) at the quad collectors and the degeneration resistor (R_1) at the input pair, as well as the dynamic emitter resistance of transistors Q_1 and Q_2, which depends on the operating bias current. Typically the LO is a large signal (such as 0dBm) and therefore the switching quad transistors are turned on and off in a manner which approximates a switching function alternating between +1 and -1. Such a square wave can be represented by its Fourier series. On the other hand the signal current (i_{c1} and i_{c2}) fed into the quad can be expressed as

$$i_{c1} \approx \frac{v_{RFin}}{(R_1 + 2 \cdot r_e)} \tag{5.1}$$

Multiplying the switching function by the signal current (i_{c1}) it can then be shown that the conversion gain for a single ended output is given by [5]:

$$A_v = \frac{2}{\pi} \cdot \frac{R_c}{(R_1 + 2 \cdot r_e)} = 0.637 \cdot \frac{R_c}{(R_1 + 2 \cdot r_e)} \tag{5.2}$$

where r_e is the dynamic emitter resistance of transistors Q_1 and Q_2. This formula shows that a large collector load is useful to increase the conversion gain. The collector load however cannot be made too large because this would excessively reduce the DC voltage at the quad collectors, thus forward biasing the base collector junction. Note that to avoid the voltage drop due to the load resistors the IF signal could be extracted by means of an off-chip transformer connected to the quad collectors.

5.2.3 Mixer linearity

The mixer linearity is essentially determined by the linearity of the input differential pair (Q_1 and Q_2) which acts as a voltage to current converter. The maximum input voltage for linear operation may be approximated by:

$$V_{linear} \approx (R_1 + 2 \cdot r_e) \cdot I_{bias} \qquad volts, peak \tag{5.3}$$

where I_{bias} is the current through each transistor of the differential pair. This value is where nonlinearity begins, and therefore is approximately where compression begins as well. Assuming that formula (5.3) gives the 1dB compression point, a first order estimate of the IP3 can be obtained by adding 10dB to the above value.

Clearly, the degeneration must be sized according to the desired linearity and taking into account the desired bias current, which for this work, in order to maintain low power, is fixed at 1.25mA for each Q_1 and Q_2 for a total bias current of 2.5mA. However a large degeneration resistor generates more noise in the circuit. Thus there is a clear trade-off between linearity and noise figure. It should also be noted that increasing R_1 to increase the linear range will reduce the conversion gain, according to equation (5.2).

5.3 Gilbert cell mixer with inductive degeneration

Traditionally resistive degeneration is used in the input differential pair as was shown in the schematic of Figure 5-1. However with the recent availability of on-chip inductors it is now possible to use inductive degeneration for reduced noise, which is the approach used in this work, as shown in the schematic of Figure 5-2.

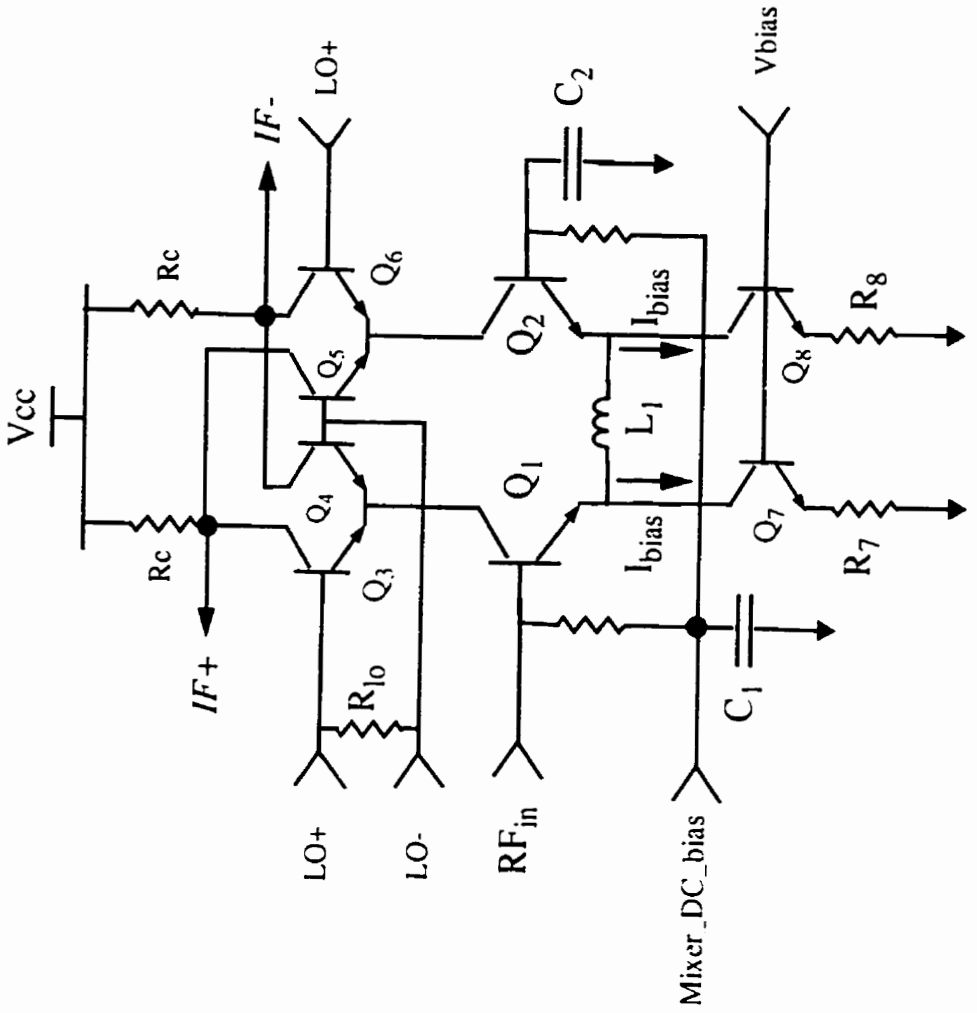

Figure 5-2: A Gilbert cell balanced mixer with inductive degeneration

Our simulations and measurements indicate that by using inductors it is possible to increase the amount of degeneration (for improved linearity) while still obtaining acceptable noise figure. As indicated in section 3.2.1 at high frequencies the emitter degeneration inductor load is rotated by -90° to then act as a resistor when looking into the base of the differential pair transistors Q_1, Q_2. Hence the presence of inductive degeneration increases the resistive component of the mixer input impedance which is useful in a monolithic context as this reduces the loading on the preceding stage.

In this case, the conversion gain formula (5.2) and the linear range given by formula (5.3) must be appropriately modified. For the mixer with inductive degeneration the maximum voltage for linear operation may be approximated as follows:

$$V_{linear} = (j\omega \cdot L_1 + 2 \cdot r_e) \cdot I_{bias} \qquad volts, peak \tag{5.4}$$

Observe that the reactance is in quadrature with the dynamic emitter resistance and therefore they do not add up linearly, thus for a large inductor the reactance will dominate. For example for operation at 1.9GHz, assuming that L_1 is a 7nH on-chip inductor, then the inductive reactance at 1.9GHz would be j83.5ohm and with a bias current of 1.25mA the corresponding r_e is 20.8 ohms.

Hence, using the previous formula would yield a maximum voltage for linear operation of:

$$V_{linear} = (j83.6 + 2 \cdot 20.8)\,\Omega \cdot 1.25mA = 93\angle 64°\Omega \cdot 1.25mA = 116mV, peak \tag{5.5}$$

which corresponds to a -8.7dBm input power assuming a 50 ohm matched input. This can be assumed to be close to the 1dB compression point and consequently the input IP3 would be estimated to be 10dB higher, in this case at +1.3dBm. This will be verified below with simulations.

The mixer of Figure 5-2 was designed on NORTEL's 0.5 micron bipolar process. The differential pair transistors Q_1 and Q_2 were made large for lower noise figure (the emitter size was 0.5 x 80 microns) while the quad transistors were half the size (emitter size 0.5 x 40 microns) of the differential pair for higher transit frequency to ensure fast switching. The degeneration inductor was 7nH as mentioned before and a lumped model used for the

simulation. This is a high frequency lumped model which was available in the NT25 library and was originally obtained from the inductor geometry using the GEMCAP2 program.

The unmatched mixer was simulated with the HPEESOFV6.0 Series IV RF simulator with a -40dBm 1.9GHz RF input and a 0dBm 2.2GHz differential LO, and with the differential pair transistors biased with 1.3mA I_{bias} each. This simulation was at the schematic level and did not include layout information. The obtained single ended IF spectrum is shown in Figure 5-3 with a 300MHz IF of -30dBm and therefore the conversion gain is 10dB. Observe the 1.9GHz RF leakage at -49dBm and the 2.2GHz LO leakage at -41dBm. This would indicate an RF to IF isolation of only 9dB and an LO-IF isolation of 41dB.

The simulated SSB noise figure was 11.8dB. This simulated noise figure is comparable to the state-of-the-art for a 2GHz monolithic mixer. For example Long's 1.9GHz BiCMOS mixer [35] exhibits a 10.9dB SSB measured noise figure which is achieved by using an on-chip transformer. Or compare with the LMX2216B mixer, manufactured by National Semiconductor on their BiCMOS process, which features a 17dB SSB noise figure at 1.89GHz RF. Glenn [51] reports a measured SSB noise figure of 16.5dB at 2GHz RF with 100MHz IF for Gilbert mixers fabricated in Si/SiGe which use a 13 ohms resistor for the emitter degeneration. Sevenhans [52] reports a 1.9GHz BiCMOS Gilbert cell with a 15dB noise figure.

Additionally a single tone simulation was carried out to observe the 1dB compression point. In this simulation the power of the 1.9GHz RF input signal is swept from -40dBm up to 0dBm and the IF output power is obtained (with a 0dBm 2.2GHz LO). The IF output power versus RF input power plot is shown in Figure 5-4, which shows the 1dB compression point at -12dBm (input referred). This is slightly poorer than the estimate previously obtained with formula (5.4), which is justified as the formula does not take into account the nonlinearities of the switching quad. Based on this number the input IP3 would be estimated to be 10dB higher, that is at -2dBm.

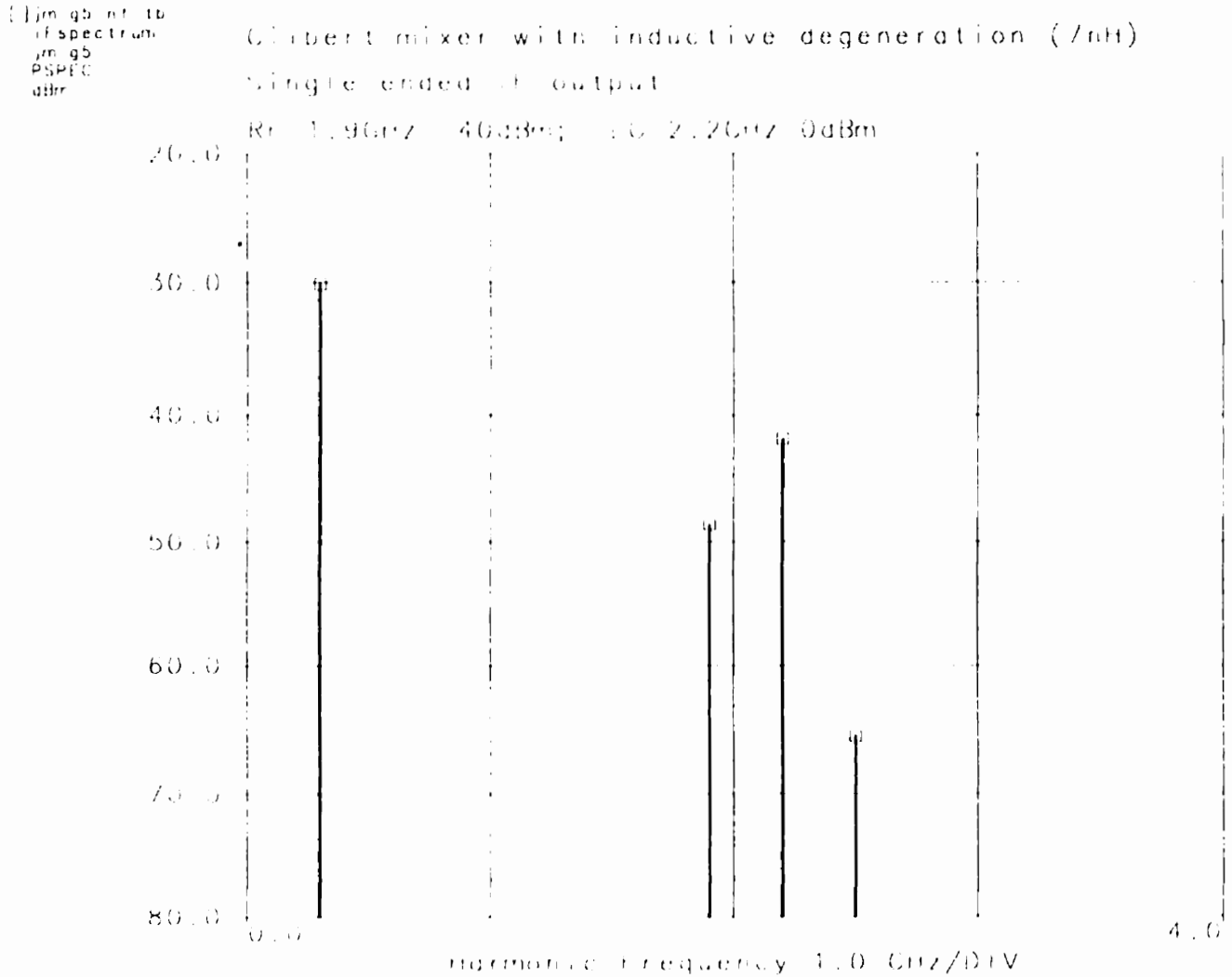

Figure 5-3: Simulated single ended IF output for Gilbert mixer with inductive degeneration; with 1.9GHz -40dBm RF input and a 0dBm 2.2GHz LO

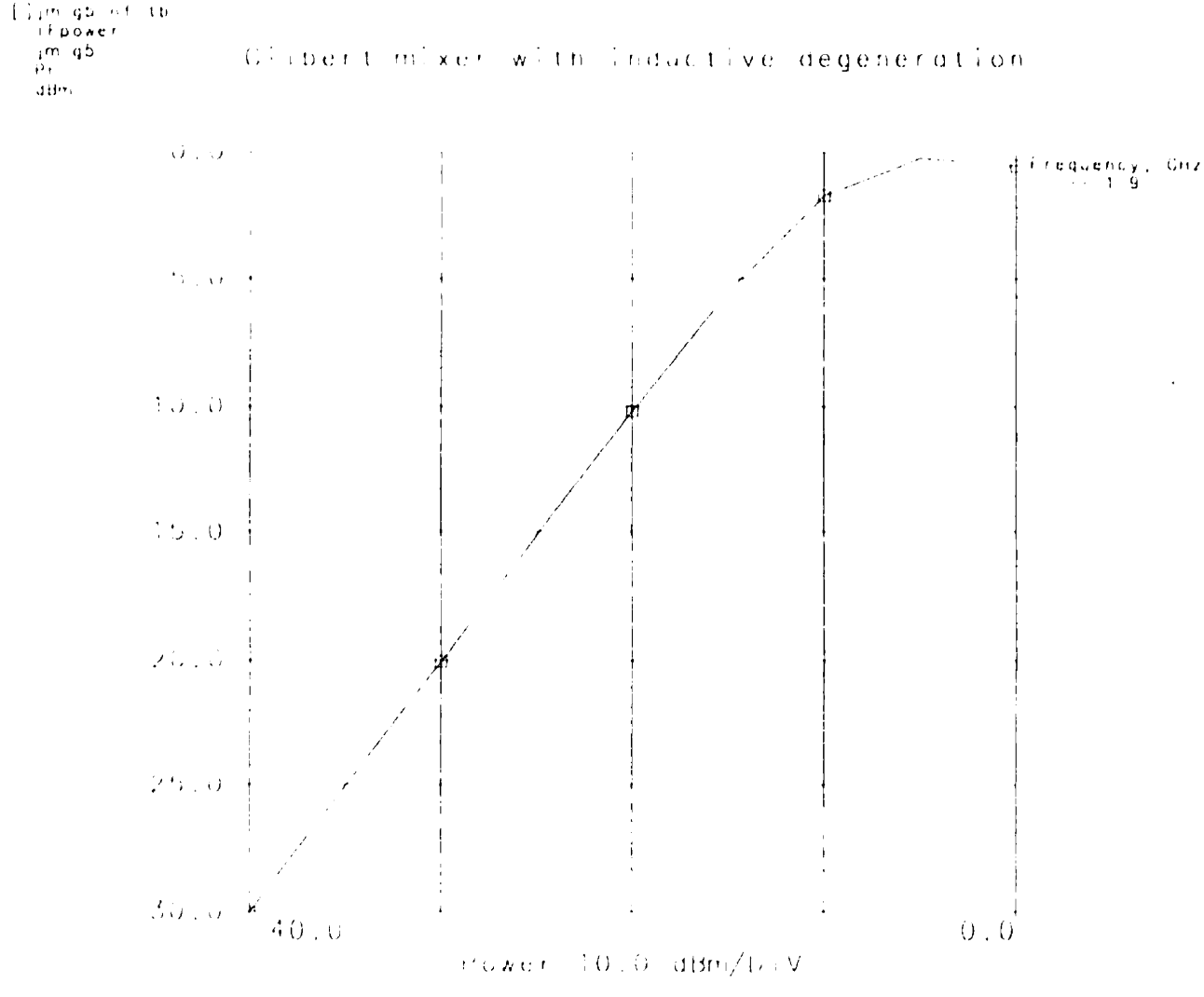

Figure 5-4: Simulated IF Power out versus RF Power In for Gilbert mixer with inductive degeneration. RF in at 1.9GHz with 0dBm 2.2GHz LO

This input IP3 is comparable to other monolithic mixers such Long's recently reported BiCMOS mixer [35] which exhibits a 1.1dBm simulated input IP3 (and was measured at 2.3dBm). Or compare with the LMX2216B mentioned above, where the mixer features a -8dBm input IP3.

The Gilbert cell mixer with inductive degeneration was then fabricated on NORTEL's 0.5 micron bipolar process and tested on-wafer. The mixer noise figure was measured with an HP8970B Noise Figure meter and with a 0dBm 2.2GHz LO for a 300MHz IF. The mixer RF input was unmatched. A DSB noise figure of 8.7dB was measured which is equivalent to 11.7dB SSB and therefore agrees well with the simulated value. The conversion gain was measured by applying a -30dBm RF input and a 0dBm 2.2GHz differential LO and observing the output IF spectrum, which showed a 300MHz IF with a -21.02dBm amplitude. Thus the measured conversion gain was 9dB, which was close to the simulated value. The input IP3 was not measured due to time constraints as a two-tone test required a careful calibration and there was a tight fabrication schedule for the integrated receiver.

Since the Gilbert cell mixer with inductor degeneration was successfully tested, it was incorporated in the overall receiver front-end presented in chapter 6 and submitted for fabrication.

5.4 Transformer coupled doubly balanced mixer

A second mixer topology considered in this work is the balanced mixer which uses a balun transformer as shown in Figure 5-5. This mixer was originally developed by Long [35] on a 0.8 micron BiCMOS process and exhibited excellent performance, with 6.1dB of conversion gain, 10.9dB SSB noise figure and a measured +2.3dBm input IP3 at a 1.9V DC supply. The balun transformer converts the single ended RF input signal into a perfectly differential signal and additionally it enables the mixer to work at a very low voltage supply.

Hence, the transformer coupled mixer was redesigned on the 0.5 micron bipolar (NT25) process used in this work. However Long designed his mixer version with a transformer with 4:5 turns ratio so as to obtain a 50ohm input impedance. This is not necessary within

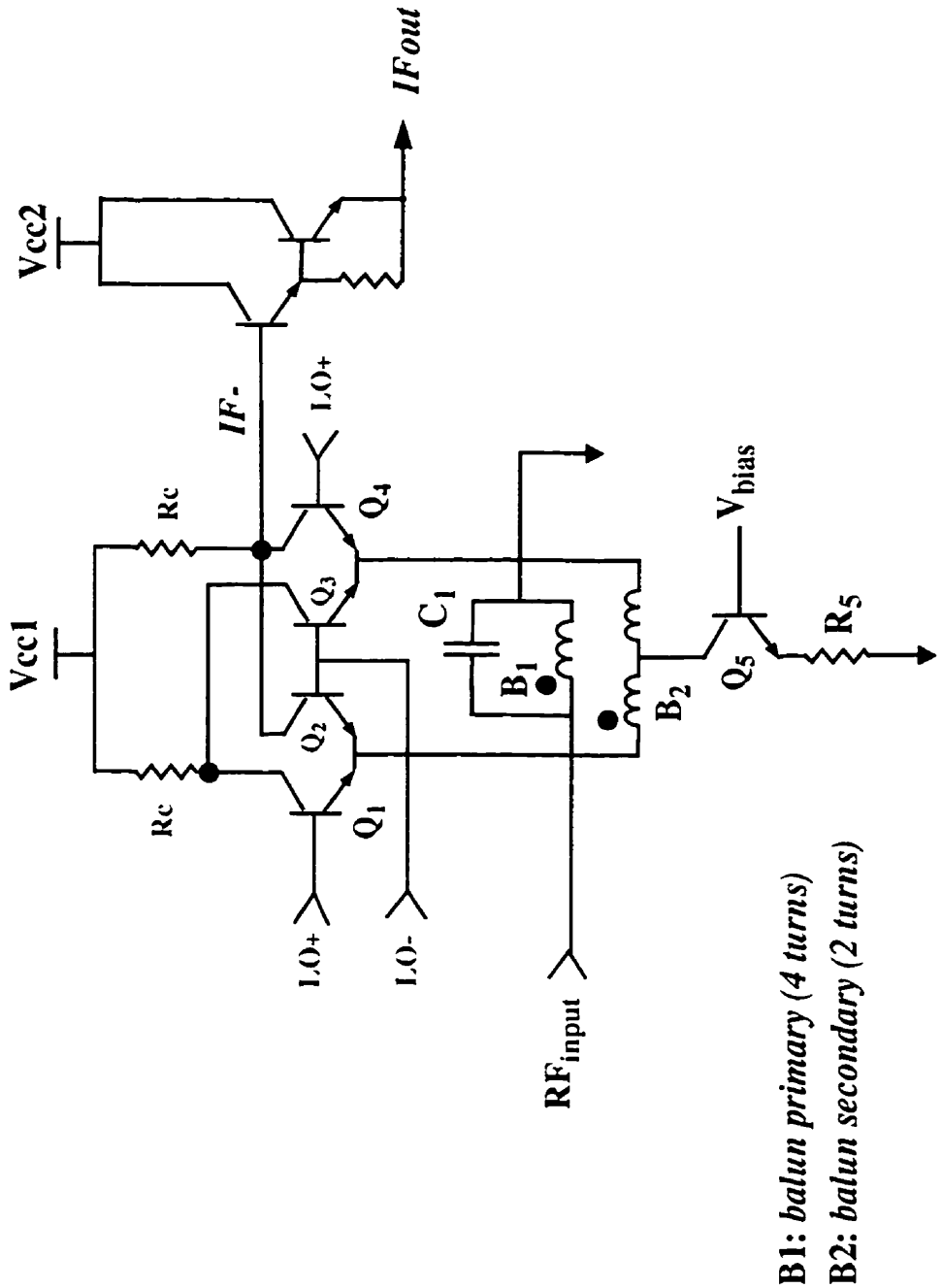

Figure 5-5: The double balanced transformer coupled mixer

a monolithic context. In fact, as will be shown in the integrated receiver (chapter 7) the mixer is connected directly to the collector of the image filter cascode (Q_4 in Figures 4-4 or 4-7). In such a context it is useful to have a higher impedance at the mixer input so as to maintain good gain at the filter output. Thus, we designed a balun with 4 turns in the primary and 2 turns in the secondary (B1 and B2 respectively in Figure 5-5) which then boosts the mixer input impedance. The balun layout is described in some detail in chapter 7, section 7.4.1. A low frequency lumped model was obtained using the GEMCAP2 program. It was verified that this model was reasonably accurate for our frequency of operation (1.9GHz).

The impedance seen at the primary is given by the square of the turns ratio times the secondary load which is the impedance looking into the emitters of the switching quad and is approximately 50 ohms for a 2.5mA bias current [5]. Thus the impedance reflected in the primary (B1) is now the square of the 4:2 turns ratio times the load, that is 4 times the 50 ohms load, for a resulting 200 ohms for an ideal transformer. However because the silicon transformer coupling coefficient is in the order of 0.75 the actual primary input impedance will be less than 200 ohms as will be discussed further in chapter 7. The primary of the balun can then be connected directly to the filter cascode as done in chapter 7 (see Schematic Figure 7-8) without excessive loss of gain.

The transformer coupled mixer was implemented in NORTEL's 0.5 micron bipolar process and then simulated with the HPEESOFV6.0 Series IV RF simulator (Libra). The quad devices were large with an emitter size of 0.5 x 40 microns for lower noise. A total bias current of 2.5mA was used (collector current of Q_5) and the simulations were done twice with a supply voltage of 3V, as well as 1.9V, with similar results.

The mixer was simulated applying a 1.9GHz -40dBm RF input and a 0dBm 2.2GHz LO. The obtained IF spectrum is shown in Figure 5-6. As seen in the spectrum the 300MHz IF sits at -29dBm, which indicates an 11dB conversion gain. Observe that no RF or LO leakages are present (they are below -100dBm!), indicating excellent isolation due to the balun transformer which converts the single ended RF input into a perfectly balanced signal. By comparison Figure 5-3 for the Gilbert cell shows significant leakage. Recall

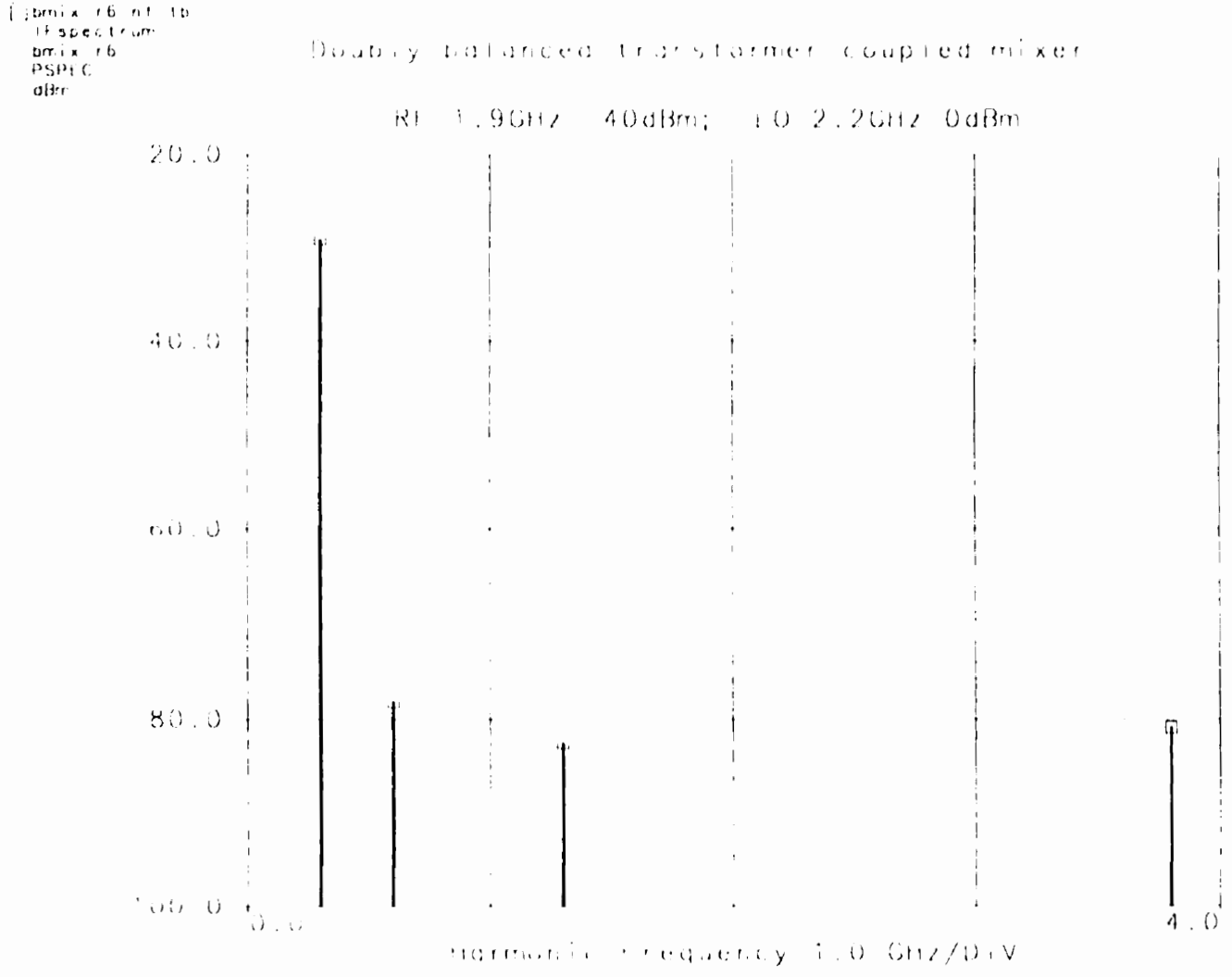

Figure 5-6: Simulated single ended IF output for transformer coupled mixer with -40dBm 1.9GHz RF input and a 0dBm 2.2GHz differential LO

however that these are schematic simulations and do not include layout parasitics. In a fabricated device substrate coupling, device mismatches, layout assymetries and packaging effects will degrade this isolation.

Thus the previous simulations indicate that the transformer coupled mixer isolation would be superior to that of the conventional Gilbert cell. This was one more motivation to use this mixer topology in a fully integrated receiver as it is important to minimize spurious signals.

The simulated SSB noise figure was 14.4dB which is 2.6dB poorer than the 11.8dB simulated SSB noise figure for the Gilbert mixer with 7nH inductive degeneration. This noise figure is also poorer than Long's measured SSB noise figure of 10.9dB, although Long's mixer was measured with a 1.8GHz LO while our version uses 2.2GHz. This degradation in noise figure can be attributed to the fact that in our mixer version the transformer is a step down transformer (turns ratio is 4 to 2), thus the desired RF signal is divided by 2, thus reducing the SNR and degrading the noise figure. Or conversely one could think that the voltage noise generated by the quad transistors has been doubled by the transformer when referred back to the input. However, in our integrated receiver there is substantial gain from the LNA and image filter and it was expected that this would minimize the impact of a higher mixer noise figure on the overall receiver.

To evaluate linearity a single tone simulation was done to obtain the 1dB compression point. The power of a 1.9GHz RF input signal was swept from -40dBm up to 0dBm and the IF output power measured. The resulting plot of IF output power versus input power is shown in Figure 5-7, which shows the input 1dB compression point at approximately -13dBm, which is close to the Gilbert cell mixer with 7nH inductive degeneration.

The simulations of the previous two sections indicated that a receiver with Gilbert mixer would achieve lower noise figure and comparable linearity than a receiver with transformer coupled mixer. However the isolation of a transformer coupled mixer was expected to be superior due to the symmetrizing properties of a balun transformer. Additionally a conventional Gilbert based receiver needs a minimum supply of 2.5 to 3Volts [5]. It is possible to use some type of folded Gilbert cell to reduce the supply voltage [53], however

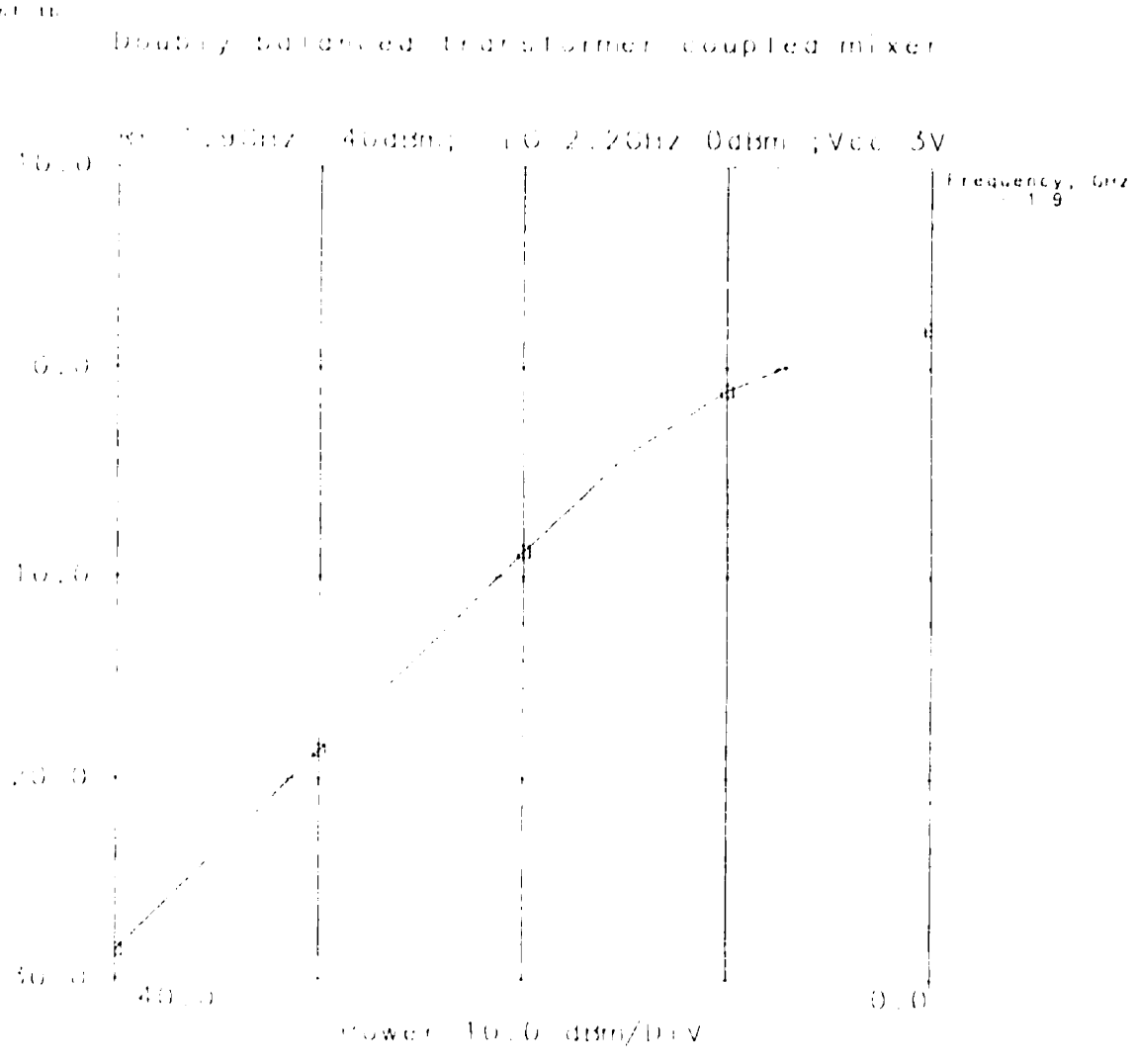

Figure 5-7: Simulated IF Power out versus RF Power In for transformer coupled mixer. RF in at 1.9GHz with 0dBm 2.2GHz LO

the power consumption will not be reduced because then twice as much current is needed. On the other hand a transformer coupled mixer [5][35] has been demonstrated to operate with a supply voltage of 1.9V and can possibly work with lower voltages, thus inherently consuming less power than a conventional Gilbert mixer.

Based on the previous simulations, it was considered worthwhile to proceed with the design of two candidate receiver front-end architectures, one which uses the Gilbert cell mixer and is described in chapter 6, and one that uses the transformer coupled mixer and is described in chapter 7.

Chapter 6 A Monolithic silicon receiver front-end architecture

In this chapter a 1.9GHz monolithic receiver front-end consisting of an LNA, a tunable image reject filter and a mixer on one die is presented [54]. This is ground breaking exploratory work which aims at extending the state-of-the-art by for the first time integrating a receiver front-end with an on-chip filter for the image rejection. The integration is very challenging due to stability, noise and linearity considerations.

The main objectives of this effort are to prove functionality of the proposed receiver front-end, that is, to verify that the circuit is stable and functions properly, that there are no harmful spurs due to undesirable intermodulation products and that the tunable image filter delivers substantial rejection and has sufficient tuning range to compensate for process variations. The thrust of this work is to demonstrate a monolithic silicon receiver front-end with performance suitable for portable radio. Once this is demonstrated the development of on-chip electronic tuning would then be justified. Due to time constraints the completion of this latter task is left to future workers. However, enough work will be done to establish that the sensitivity of the tuning to voltages, currents and parameter variations is such that it is feasible.

Performance will be evaluated by measuring key parameters, such as conversion gain, noise figure, image rejection, third-order intermodulation product, isolation (RF-IF, LO-IF and LO-RF) as well as power consumption. The design trade-offs will be explored and the key limiting factors on performance examined.

Another important objective is to compare measured with simulated performance so as to evaluate the accuracy of the models for the transistors as well as the passive devices such as on-chip inductors, both of which are crucial to a good RF circuit simulation. Furthermore, due to the relative complexity of the receiver front-end, a dozen or so I/O pins are now required (various DC supplies, RF input, differential LO inputs, differential IF outputs, image frequency tuning and image Q tuning control voltages), and hence it is necessary to package the chip for testing. Hence, it becomes necessary to deal with

wirebonds and package modelling if an accurate simulation is desired. Also an off-chip matching network must be designed, as well as a printed circuit board (PCB) in which the chip will be mounted. The PCB is designed with 50 ohm microstrip lines for the RF signals.

In the following sections the receiver front-end with Gilbert mixer is described

6.1 Receiver front-end with Gilbert mixer

The architecture for the receiver front-end explored in this section consists of an LNA, an image reject filter and a Gilbert cell mixer all in the same die. There are a variety of possible topologies for the LNA and the mixer. Since this is a first demonstration a simple two inductor tuned LNA has been selected for the amplifier. The Gilbert mixer has been improved for lower noise by replacing the conventional resistive degeneration with an inductive degeneration [55] as presented in the previous chapter.

This receiver front-end was designed for best conversion gain and lowest noise figure with a 16mA current consumption at 3V. This low noise version is referred to as jm_grx1 and is described in section 6.1.1 that follows.

This receiver front-end builds upon the expertise developed in chapter 4. That is, the LNA with tunable image rejection integrated circuit which was designed in chapter 4 is used here without any modification. The approach is to connect a Gilbert cell mixer to the image reject filter output. This will ensure best conversion gain and therefore lowest noise figure, since the image reject filter has an output buffer which allows it to drive large loads without any gain degradation.

The simulation results for the integrated receiver will be presented in section 6.2 and the measurement results will be described in section 6.3.

6.1.1 Low noise receiver front-end (version jm_grx1)

This chip was the first integrated receiver front-end fabricated using NORTEL's 0.5 micron bipolar process within this work and was designated as jm_grx1. It is distinguished by a Darlington buffer between the notch filter and the mixer.

As the schematic of Figure 6-1 shows, jm_grx1 consists of an LNA (Q_1), an image reject filter stage (Q_2, Q_3, Q_4), the buffer (Q_5, Q_6) and then the Gilbert cell mixer (Q_7, Q_8, Q_9,Q_{10}, Q_{11}, Q_{12}). The LNA transistor Q_1 is DC biased to 3mA by means of an off-chip bias T network, while the filter transistor Q_2 is biased to 2.5mA by adjusting the bias voltage V_{filter_bias}. In this first receiver version the LNA with image rejection module was deliberately left as presented in chapter 4 so as to have known measured data on its frequency response (S_{21}) so as to be able to predict final performance when the mixer was added to compare with measured results. For this reason the buffer Q_5, Q_6 was left in place exactly as was presented in chapter 4. The purpose of the buffer is to protect the filter tuned output (collector of cascode transistor Q_4) from being loaded and detuned by the mixer input impedance. In this way maximum passband gain is obtained (from the LNA and filter circuit) and best noise figure is achieved and the circuit is more robust against process variations, at the cost of the additional buffer current of 6mA. Note that the current of this buffer could easily be reduced by half while still maintaining good performance because the mixer input impedance is relatively high, in the order of 300ohms.

Following the buffer is the doubly balanced Gilbert cell mixer. The single ended RF signal available at the buffer output (emitter of Q_6) is converted into in-phase and anti-phase currents by the differential transistor pair Q_7, Q_8 and fed to the upper four transistors Q_9, Q_{10}, Q_{11} and Q_{12}, usually referred to as switching quad. The switching quad is driven by the 2.2GHz differential local oscillator (LO+ and LO-) which is typically a large signal.

The emitter degeneration inductor L_5 achieves a substantial reduction in noise while providing improved linearity. The mixer input transistors Q_7 and Q_8 were selected as large size devices (80micron x 0.5micron emitter) for reduced noise. They are biased at 1.25mA each by means of current sources (Q_{13}, Q_{14}) whose current is adjusted by means of V_{bias}. The switching quad transistors were made half the size of the input pair transistors for increased transit frequency to ensure fast switching (the LO is 2.2GHz) while still maintaining low noise. Collector load resistors (R_c) were selected to ensure sufficient conversion gain. The IF outputs are fed into two emitter follower buffers (which are not

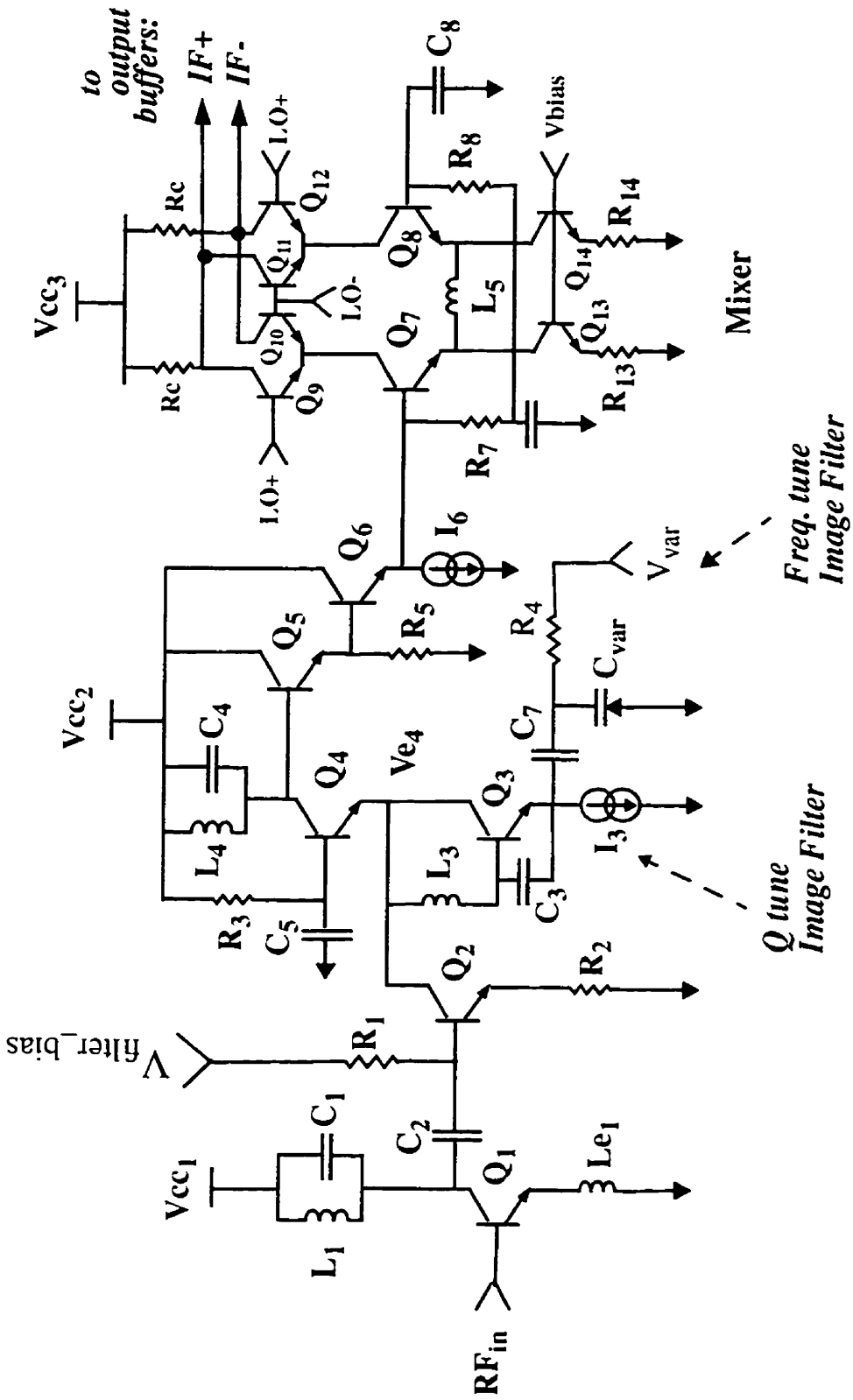

Figure 6-1: Low noise receiver front-end with Gilbert mixer (jm_grx1)

shown in the schematic of Figure 6-1 for simplicity) which can drive 50 ohms loads for testing purposes. This allows testing using single ended or differential IF outputs.

Observe that the conversion from single ended to differential signal is achieved by the differential pair Q_7, Q_8 by AC grounding the base of Q_8 by means of an on-chip capacitor (C_8) while the single ended signal feeds the base of Q_7. For this reason the impedance seen by the base of Q_7 is not the same as the one seen by the base of Q_8. Our experimental results indicate that this asymmetry is not a significant problem.

The DC bias voltage at the base of Q_7 is provided by the emitter of Q_6 which is two "diode drops" below V_{cc2}, that is, approximately 1.3V DC. The resistive network R_7, R_8 provides the base current for Q_8, and therefore the DC voltage at the base of Q_8 is slightly lower than at the base of Q_7. As a consequence the DC collector current through Q_7 will be larger than the current through Q_8. This asymmetry tends to unbalance the mixer and will therefore reduce the isolation, however it does not affect functionality. This problem has been corrected in version jm_grx4 which will be described in chapter 7. The following section describes the layout of this receiver front-end.

6.1.2 Layout of low noise receiver (version jm_grx1)

Fig. 6-2 shows a micrograph of the layout for version jm_grx1 fabricated in NORTEL's 0.5 micron bipolar technology.

Clearly visible are the three stages. The LNA at the top of Figure 6-1 has two inductors; the inductor to the left (L_{e1}) is for the emitter degeneration while the inductor to the right (L_1) forms the LNA LC tank. The middle section is the notch filter, where the left inductor is L_3 while the right inductor is L_4 (see schematic Fig. 6-1). Below the filter is the Gilbert cell mixer which shows two 3.5nH degeneration inductors connected in series, and in a symmetric manner, to form L_5.

The RF input pad is at the top (fourth from the right), the differential LO pads are seen at the bottom (third and fourth from the left) and the IF output pads can be seen at the right hand side (last two to the bottom). These pads were positioned orthogonally to each other to minimize crosstalk due to the wirebonds connected to them when the chip is packaged.

Multiple pads are used for the various Vcc lines so as to connect two or three wirebonds in parallel, thereby minimizing parasitic inductance. Similarly a large number of ground pads (19 for this chip) are used to minimize wirebond inductance to ground.

The inductors were laid out using top metal aluminum with 2 micron thickness, which ensures better Q [47]. Sufficient space is maintained between the outer turn of the spirals and surrounding metal traces in order to minimize unwanted parasitic effects which would disturb the inductor's electrical characteristics [47]. Metal Insulator Metal (MIM) capacitors are used throughout for good quality factor. The active area is approximately 1.1 x 1.5 mm^2.

Before fabrication, a netlist was extracted from this layout and simulated with HSPICE to verify correct functionality.

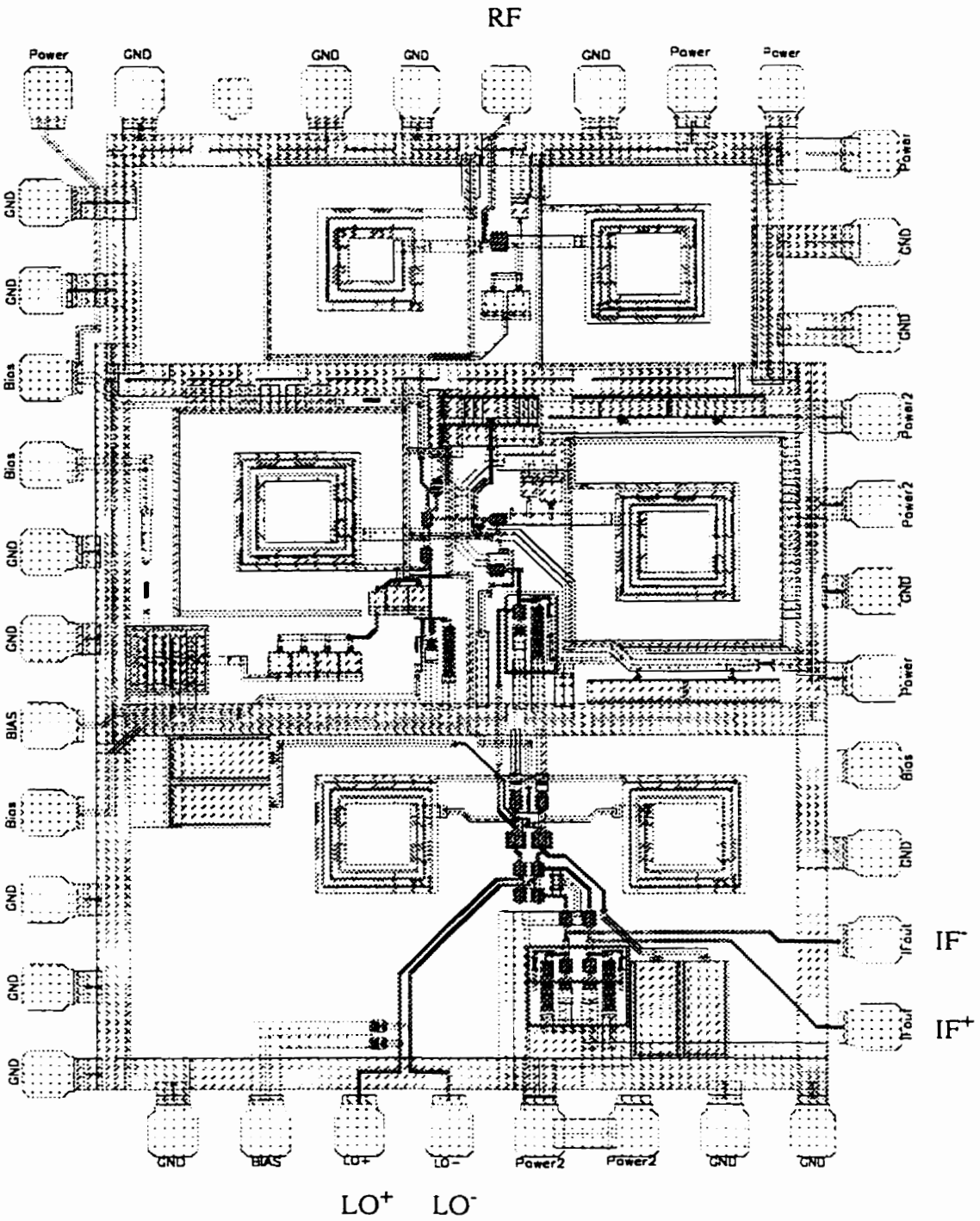

Figure 6-2: Layout of low noise receiver (jm_grx1) on 0.5 micron bipolar

6.2 Simulation of receiver front-end (version jm_grx1)

The simulation results with NORTEL's 0.5 micron bipolar technology (NT25) for the receiver front-end with a Gilbert cell mixer are summarized in the table below.

Table 6-1: Simulation of receiver front-end (version jm_grx1)

Parameter	Unmatched	Matched
Noise Figure	4.0dB	3.5dB
Conversion Gain (1.9GHz RF, 300MHz single ended IF)	31.9dB	34.4dB
Input IP3	-27dBm	-28dBm
Current @ 3V DC	16mA	16mA
Mixer Degeneration	7nH	7nH

The results shown in Table 6-1 were obtained with a 1.9GHz RF input and 0dBm, 2.2GHz differential LO for a 300MHz single ended IF output. The power supply was 3V DC and the receiver input was matched to 50 ohms by means of an off-chip LC network. These simulations were done at the schematic level (without layout parasitics) using SeriesIV HPEESOFV6.0 simulator ("Libra") and using typical models. As the wirebonds for the TQFP package are in the order of 1mm long, they were represented as 1nH inductors with a Q of 30.

Unfortunately, the Series IV HPEESOFV6.0/Libra simulation to obtain the input IP3 for the receiver front-end aborted (it seems that the 3 tone simulation fails to complete when the circuit has a large number of transistors). The input IP3 results presented in table 6-1 are estimates based on the LNA and filter gain combined with the estimated mixer input IP3. The unmatched LNA and filter gain was measured at 25dB (see section 4.4), while the mixer input IP3 is approximately -2dBm based on the simulations of section 5.3, hence a first order estimated input IP3 is -2dBm-25dB = -27dBm for the unmatched case. This estimate agrees well with the experimental measurements to be presented in section 6.3.

Also, in section 4.3.1 the matched LNA and filter was simulated at 26dB and therefore the estimated IP3 for the matched receiver would then be -28dBm.

As Table 6-1 shows, the simulated noise figure and linearity for this receiver are sufficient to meet the DECT requirements described in section 1.3.1. Actually, the noise figure has plenty of margin as the required receiver noise figure is 16.8dB, however the linearity of the matched receiver just meets the required -27.5dBm.

On the other hand the noise figure is sufficiently low to meet the requirements for a GSM application but the required linearity is insufficient.

In summary, this schematic simulation showed very promising results which encouraged the continuation of the work.

6.3 Measured results of receiver front-end with Gilbert mixer

The fabricated low noise receiver front-end jm_grx1 (schematic of Figure 6-1) was packaged, mounted on a printed circuit board (PCB) and tested. The receiver was first packaged on a Nortel's in-house 44 pin ceramic quad flat package (44CQFP) for quick prototyping and tested without input matching, with the results shown in the following section 6.3.1. Later the chip was also packaged on a smaller 20 pin TQFP plastic package and tested with its input matched to 50 ohms, with the results shown in section 6.3.2. In both cases the receiver functioned well, with no oscillatory tendencies being observed.

6.3.1 Unmatched low noise receiver (version jm_grx1)

For this test the receiver front-end chip was packaged on a 44CQFP package which is a relatively large package (the wirebonds are in the order of 4mm long and their inductance can be estimated at 4nH) but was used nevertheless with the main objective of rapid prototyping, as this packaging job was done in-house (at Nortel's facilities). The packaged chip was then mounted on a PCB with 50 ohm microstrip lines for the RF, LO and IF signals.

The RF input was not matched yet as this was the first functional test of this chip. A 0dBm 2.2GHz differential local oscillator was used for all tests. This consisted of an HP83712A RF generator followed by a balun manufactured by Picosecond Pulse Labs which converted the single ended RF generator signal into a differential signal which was properly calibrated for 0dBm.

The IF output was converted from differential to single ended by means of an external balun manufactured by Picosecond Pulse Labs. A 6dB gain improvement is theoretically expected with such a differential to single ended conversion. However the balun used here has approximately 8dB insertion loss and for this reason the output power level measured at the balun output is approximately the same as for the single ended IF output case. Thus, in this measurement the differential to single ended conversion does not show any gain improvement but does show a cleaner spectrum by cancelling spurious common mode signals, such as the RF leakage.

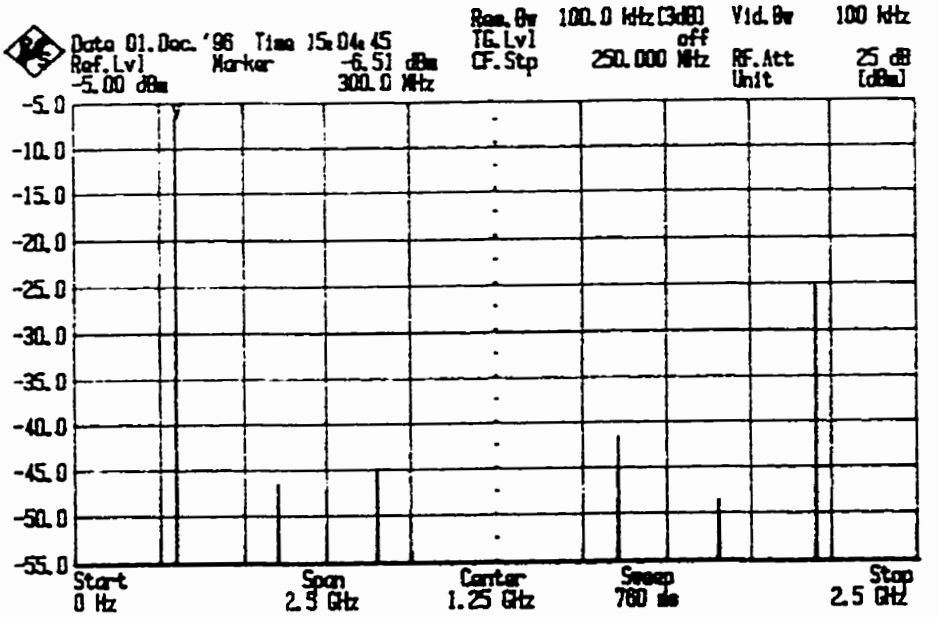

Figure 6-3: Measured IF output with a -40dBm 1.9GHz RF input and a 0dBm 2.2GHz differential LO

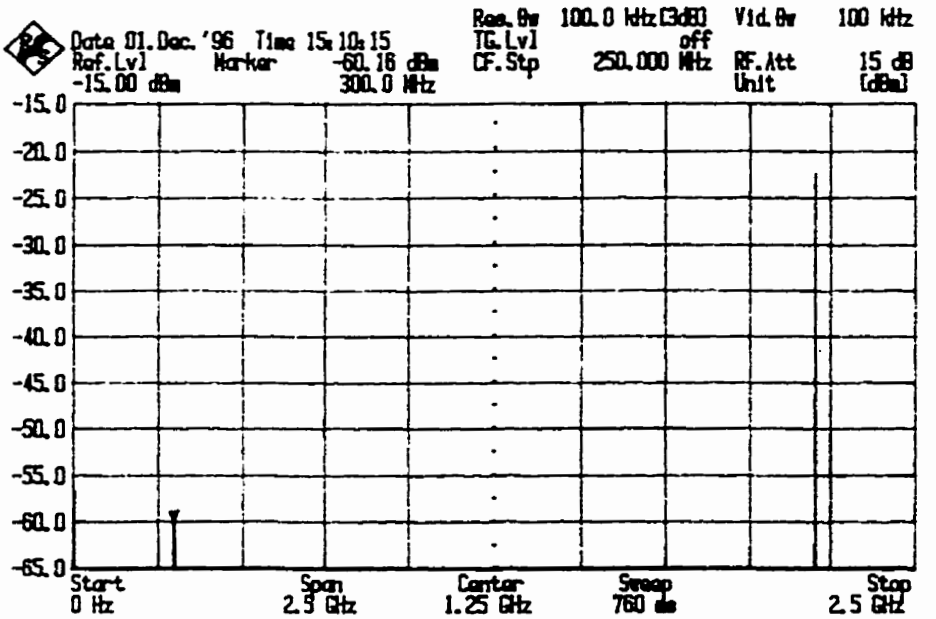

Figure 6-4: Measured IF output with a -40dBm 2.5GHz image at RF input and a 0dBm 2.2GHz differential LO

Figure 6-3 shows the IF output spectrum when a 1.9GHz -40dBm RF signal is applied to the receiver input. The plot clearly shows a 300MHz -6.51dBm IF output, for a total conversion gain of 33.49dB. Reasonable RF and LO leakages are also seen. Thus the unmatched receiver exhibits excellent conversion gain and good isolation.

The measured notch frequency tuning range was 230MHz from 2.4GHz to 2.63GHz, corresponding to a varactor control voltage of 0V and 3V respectively. This receiver chip was obtained from fabrication batch 1 and its notch frequency tuning range is the same as the corresponding LNA with image rejection measured in section 4.4.

The image rejection was verified by applying a -40dBm 2.5GHz image frequency to the receiver input, tuning the varactor voltage to place the notch at 2.5GHz and then adjusting current source I_3 (see schematic Fig.6-1) to minimize the undesired 300MHz IF output. Figure 6-4 shows the obtained -60.16dBm 300MHz IF output due to the undesired 2.5GHz image. Comparing this with Figure 6-3 above shows that the undesired image has been suppressed 53.6dB below the desired RF.

The noise figure was measured with an HP8970B Noise Figure Meter calibrated for a 300MHz IF. The obtained NF of 4.9dB compares well with the present state-of-the-art. This is actually better than all the image reject chips surveyed in Table 2-1 except for the Philips part, which exhibits a superb 4.3dB.

Linearity was tested by applying two -40dBm RF tones at 1.89GHz and at 1.9GHz respectively and observing the IF output on a spectrum analyzer. The obtained third order intercept point of -28dBm is somewhat low due to the relatively high conversion gain, and an improved version is described later.

Current consumption is 15.9mA, divided as follows: 3mA for the LNA, 3.4mA for the notch filter, 7mA for the filter buffer (Q_5, Q_6) and 2.5mA for the mixer. Hence, the total power consumption is 48mW. This power is lower than all the surveyed monolithic image reject downconverters.

The measured results for the unmatched receiver version jm_grx1 are summarized in the Table below.

Table 6-2: Receiver measured results (jm_grx1):

Parameter	jm_grx1 (unmatched)
Conversion Gain	33.5dB
S11	N/A
NF @ 1.9GHz	4.9 dB
Input IP3	-28dBm
Image Rejection (@2.5GHz)	> 50dB
Notch Tuning Range	2.44/2.69 GHz
RF-IF Isolation (mixer)	33 dB
LO-IF Isolation	25dB
LO-RF Isolation	58dB
DC Current	15.9mA
Power Supply	+3V DC
Power consumption	47.7mW
Package	44CQFP

The results shown in the above table are very encouraging. Stability and proper functionality without oscillations was demonstrated. Excellent on-chip image rejection comparable to SAW filter performance was achieved. The measured noise figure of 4.9dB is clearly sufficient to meet a GSM requirement. Unfortunately the input IP3 of this version is weak and insufficient for a GSM receiver. In order to improve this, an upgraded design is presented in chapter 7.

6.3.2 Input matched low noise receiver (version jm_grx1)

The low noise receiver version jm_grx1 was also packaged on a 20 pin thin quad flat package (20TQFP). This is a 5mm x 5mm plastic package and the wirebonds are in the order of 1mm long, thus their influence on the circuit behaviour is reduced. In this case the receiver input was matched to 50 ohms.

The packaged device was mounted on a printed circuit board. On the PCB, 50 ohm microstrip lines were used for the RF, LO and IF signals. High quality surface mount components (SMTs) were used to implement the off-chip input matching network, which consisted of a 3.9nH SMT series inductor and a 1.5pF shunt capacitor. Further details on the matching will be explained in section 7.1.2.1. An input reflection coefficient (S11) of -19dB was measured at 1.9GHz, indicating good matching. This time two tests were performed, the first test with a single RF tone and the second test with two tones, that is, both RF signal and image signal of equal amplitudes were applied simultaneously to the receiver input.

The LNA transistor Q_1 was biased at 3mA using an external "Bias T" and the filter transistor Q_2 was biased at 2.5mA, while the mixer was biased for a total current of 2.5mA. In this case the LO- signal was AC grounded by means of an off-chip SMT capacitor and the local oscillator signal applied to the LO+ input. A 0dBm 2.2GHz single ended local oscillator (HP83712A) was used for all tests. The IF output was converted from differential to single ended by means of an external balun.

The notch filter was first tuned by applying a -40dBm 2.5GHz image to the RF input, adjusting the varactor control voltage (V_{var}) to center the notch at 2.5GHz and then by tuning I_3 (see schematic Figure 6-1) to obtain a deep notch, i.e. to obtain a very small 300MHz IF output (in this case -80dBm was easily obtained).

For the first test, the single -40dBm RF input tone is first swept from 2.4875GHz to 2.5125GHz (image frequencies) and then adjusted to 1.9GHz (the desired RF). Figure 6-5 shows the obtained 300MHz IF output. The spurious IF signals due to the swept image are clearly shown regularly spaced 1MHz apart. The desired 300MHz IF signal is shown in the center. As the plot shows the notch gets deeper as the image approaches 2.5GHz, which is the center of the notch.

The plot clearly shows the desired 300MHz IF at -8.43dBm, while for a 2.5GHz image the undesired IF would be approximately at -80dBm and cannot be distinguished from the

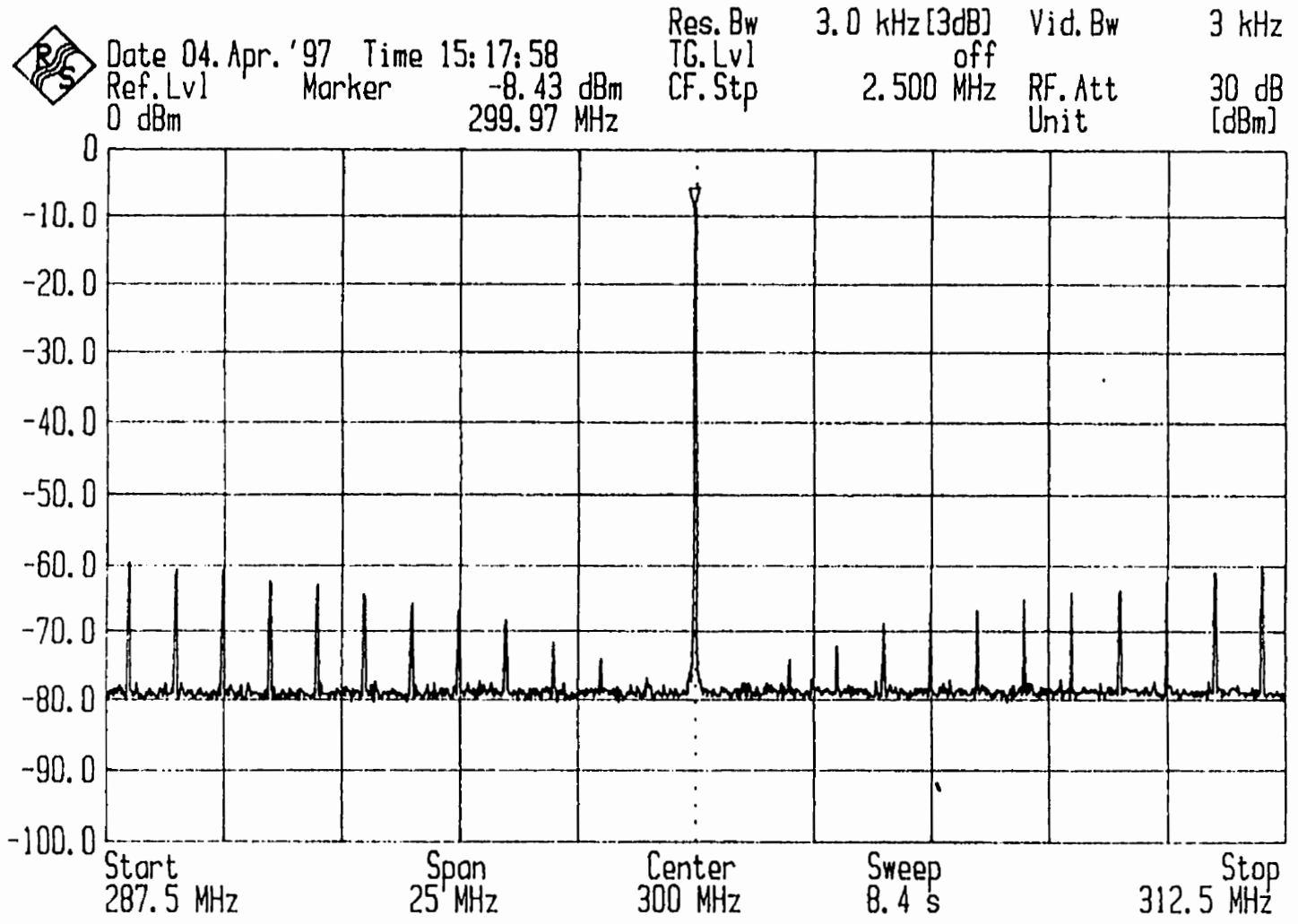

Figure 6-5: IF output of matched receiver front-end; single tone -40dBm RF input swept from 2.4875 to 2.5125GHz (image) and then fixed at 1.9GHz (desired RF). Q tuning current (I_3) was adjusted for best rejection of 2.5GHz image

noise floor. That is the close-in image rejection is 72dB which is better than the previous unmatched receiver of section 6.3.1. This improvement in image rejection can be attributed to a large extent to the input matching network, which improves the selectivity of the circuit because it has been realized with high Q off-chip components. Thus the input matching network provides additional image rejection.

For an image located +/-12.5MHz away from the notch center, the undesired IF has an amplitude of -60dBm. Hence, these measurements show that the notch depth is better than 52dB on a 25MHz bandwidth centered at 2.5GHz.

For the second image rejection test two different tones both with -40dBm amplitude were combined and simultaneously applied to the receiver RF input. The first tone was the 1.9GHz desired RF and the second tone was the undesired image which was swept from 2.4875GHz to 2.5125GHz.

As the plot of Figure 6-6 shows the image rejection is maintained practically identical to the single tone experiment of Figure 6-5. The main difference is that the image tones are not spaced so regularly, which was because the image tone signal generator had to be tuned in a more awkward manual way with a rotating knob. In this case the actual value of rejection is 67dB for a 2.5GHz image (at the center of the plot).

These results clearly show that the receiver front-end works well with an RF input in the presence of the interfering image. The experiments also show that for a notch width of 25MHz a 50dB rejection is obtained and for narrower bands rejections as high as 67dB have been measured. This input matched receiver was also used to examine the sensitivity of the notch to the tuning current I_3 as well as to the varactor tuning voltage V_{var} as presented in the following sections.

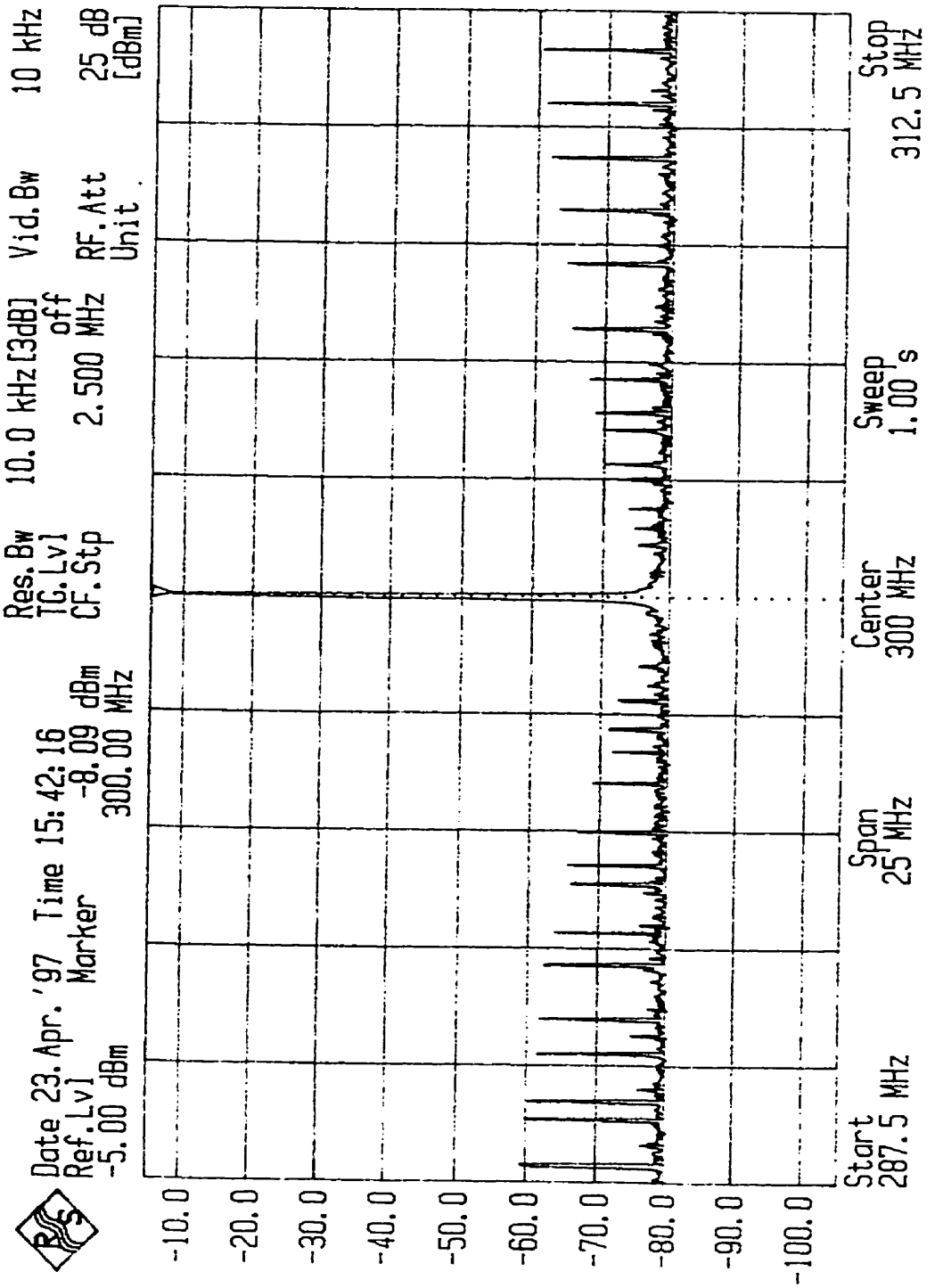

Figure 6-6: IF output of matched receiver with 1.9GHz RF and image applied simultaneously to the RF input. Image swept 25MHz around 2.5GHz. Q tuning current (I_3) adjusted for best rejection of 2.5GHz image

6.3.3 Sensitivity of image rejection to the Q tuning current

Naturally, if the current I_3 (see Figure 6-1) is detuned, the image rejection will be reduced and the undesired image response will grow. Hence, the sensitivity of the image rejection to the Q tuning current I_3 is very important as regards the design problem of tuning circuitry. The sensitivity has been experimentally evaluated on the input matched low noise receiver (version jm_grx1) as follows.

First, a -40dBm, 2.5GHz image was applied to the receiver RF input, the current I_3 was adjusted to obtain the highest image rejection, and the corresponding Q tuning current recorded. I_3 was then detuned to allow the undesired 300MHz IF to increase and the corresponding image rejection was measured by subtracting this undesired 300MHz IF from the desired 300MHz IF, which is at -8.4dBm as indicated in the previous section (Figure 6-5).

The measurement results are summarized in the following table:

Table 6-3: Receiver image rejection versus Q tuning current

Q tuning current (I_3)	I_3 (% of optimal)	300MHz IF	Image rejection
0.668mA	80.3%	-50dBm	41.5dB
0.747mA	89.8%	-55dBm	46.5dB
0.782mA	94.0%	-60dBm	51.5dB
0.802mA	96.4%	-65dBm	56.5dB
0.814mA	97.8%	-70dBm	61.5dB
0.832mA	100%	-80dBm	71.5dB

A similar result was obtained for I_3 greater than 100% optimal. The table shows that to ensure a minimum 50 dB rejection of a 2.5GHz image frequency, the tuning current I_3 must

be maintained within 6% of its optimal value (the optimal value is the value of I_3 for highest rejection which in this case is 0.832mA).

To better illustrate the sensitivity of the tuning current, the test of Figure 6-5 was repeated but with the current source I_3 at 94% of its optimal value, yielding the plot shown in Figure 6-7. Observe in this plot that while the close-in rejection has reduced to 51dB, the rejection at -12.5MHz from the notch center has reduced to 50dB and the rejection at +12.5MHz has reduced to 48dB. Hence, while the rejection at the notch center reduced by 20dB, the rejection at the band edges, that is +/-12.5MHz from the center has reduced only 4dB and 2dB respectively.

Thus, with the Q tuning current at 94% of its optimal value the image rejection across the 25MHz image band is still significant. This shows that for wider RF signal bandwidths, the tuning of the notch would not be so critical. As well, for narrower bandwidth signals, a minimum amount of image rejection of 50dB is relatively easy to achieve and if the control current (I_3) can be maintained within a few percent of its optimum value very high rejection can then be achieved.

The measured sensitivity is reasonable and it should be possible to implement a current source with sufficient accuracy (within a few percent) to maintain substantial image rejection, provided that acceptable control of the frequency of the notch can be achieved. This will be explored next.

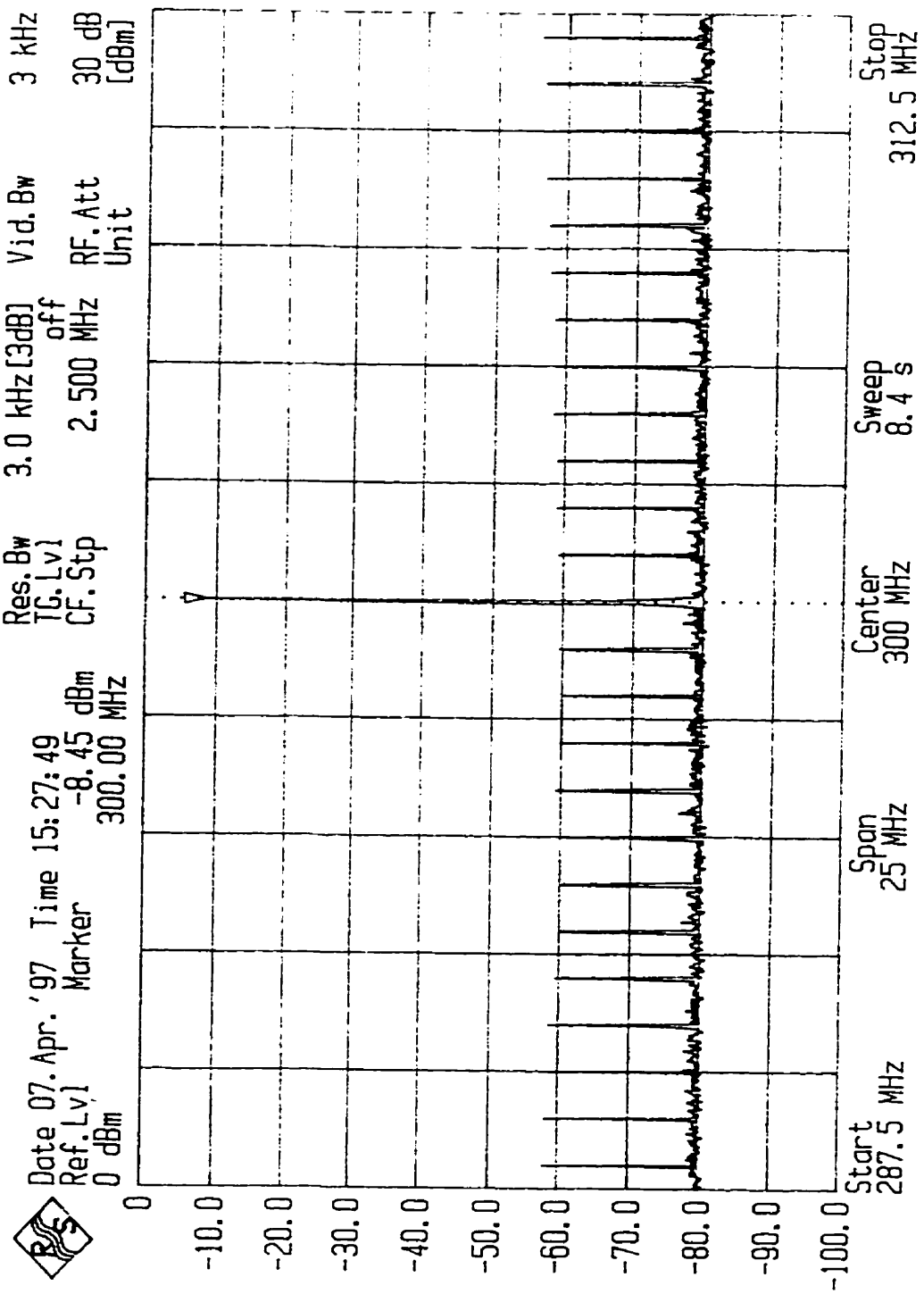

Figure 6-7: IF output of matched receiver front-end (version jm_grx1); single tone -40dBm RF input swept from 2.4875 to 2.5125GHz (image) and then fixed at 1.9GHz (desired RF). Q tuning current (I_3) adjusted at 94% of its optimal value

6.3.4 Sensitivity of notch frequency to varactor control voltage

The notch of the image reject filter is centered with the varactor control voltage V_{var}. Hence, the tuning range and the sensitivity of the notch frequency to this control voltage were measured for the matched receiver front-end (version jm_grx1) corresponding to fabrication batch 1.

The notch frequency tuning range was measured and found to be from 2.429GHz to 2.627GHz from 0V to 3V varactor control voltage respectively, i.e., a total range of 198MHz. The tuning range curve is shown in Figure 6-8. This tuning range is in agreement with the measured notch frequency tuning range for batch 1 of the LNA with image rejection presented in section 4.5.

The tuning curve indicates that to place the notch at 2.5GHz a 0.442V varactor voltage is required; this is referred to as the optimal varactor voltage. Also, the slope or sensitivity at the desired 2.5GHz notch frequency is 130MHz/Volt, which is reasonable as will be apparent from the following analysis. Using the slope value, the notch frequency change due to a small change of varactor voltage around the center value can easily be obtained. The results are shown in Table 6-4 below, in which ΔV_{var} represents the percent of change with respect to the 0.442V optimal varactor voltage.

Figure 6-6 was used to evaluate the corresponding rejection away from the notch center. For example, moving +/-1.14MHz from the center, the rejection is still 67dB. Observing again, Figure 6-6 shows that the image spurs located +/-2.9MHz from the center are below -70dBm (while the desired 300MHz IF is at -8.09dBm) and hence the image rejection is now 62dB.

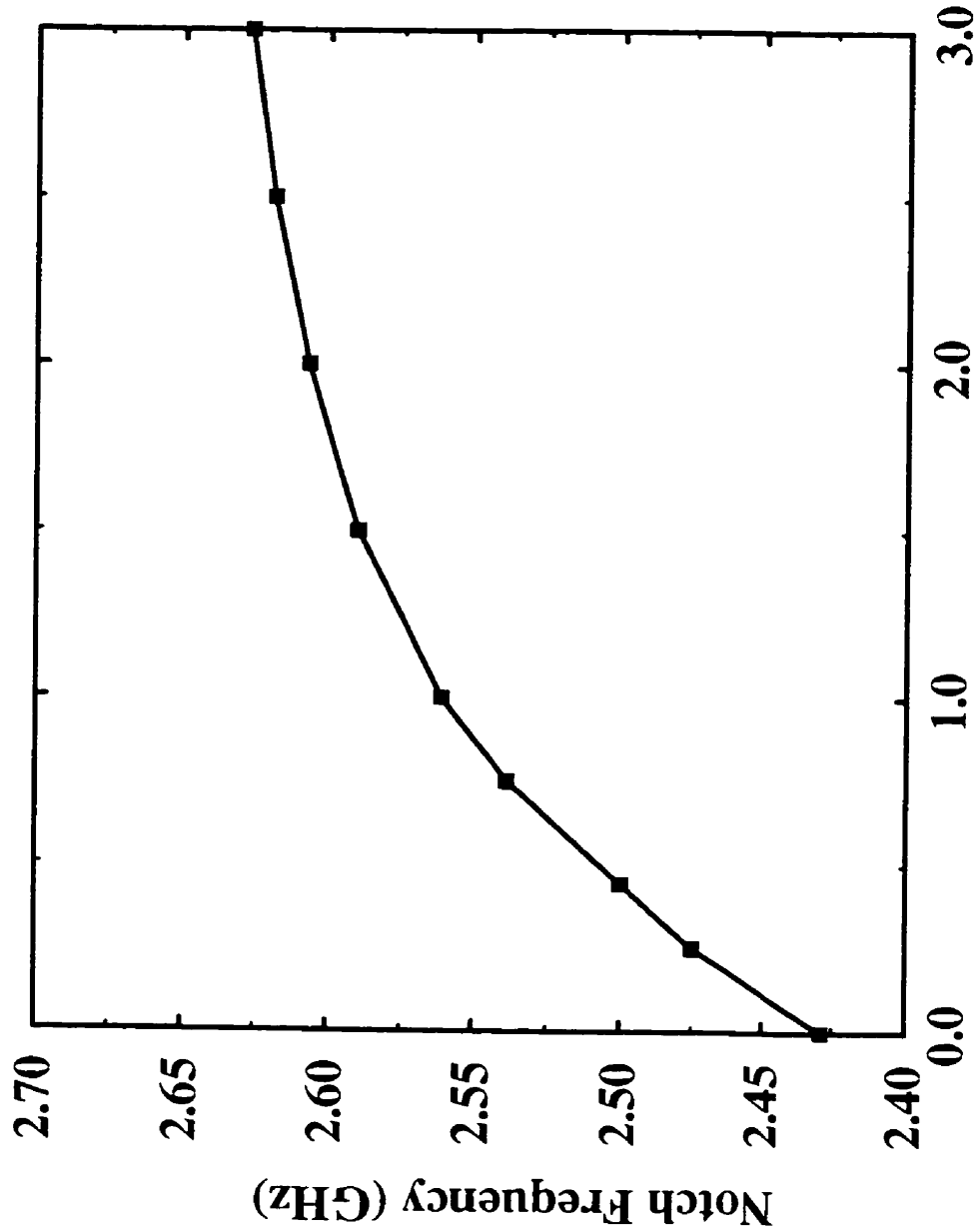

Figure 6-8: Notch frequency tuning range for input matched receiver front-end (jm_grx1)

Table 6-4: Sensitivity of notch frequency to varactor voltage

ΔVvar (in % of optimal)	Varactor voltage change	Notch Frequency change	Image Rejection
+/-2%	+/-8.8mV	+/-1.14MHz	67dB
+/-5%	+/-22.1mV	+/-2.9MHz	62dB

This table shows that maintaining the varactor control voltage within +/-2% does not degrade the notch rejection and if the varactor voltage is kept within +/-5% of its tuned value the notch is degraded only by 5dB.

Hence, maintaining Vvar within +/-5% should still allow 50dB of notch rejection in a 25MHz. band according to the previous section.

Chapter 7 Improved receiver front-ends

In this chapter three additional receiver front-end versions are studied. The first two versions presented in section 7.1 use a Gilbert cell mixer and are improvements over version jm_grx1 introduced in the previous chapter.

A third version presented in section 7.2 is a receiver front-end which uses a transformer coupled mixer instead of a Gilbert cell in an attempt to reduce the DC supply voltage. For each version the schematic is first presented followed by the experimental results.

7.1 Improved receiver front-ends with Gilbert cell mixer

As shown in chapter 6 the first receiver front-end (version jm_grx1) functioned well but had limited linearity and consumed 48mW DC power. In an effort to improve these shortcomings the following two versions were designed:

a) Version jm_grx4 is a version with better linearity obtained by doubling the size of the mixer degeneration inductor. It is described in section 7.1.1.

b) Version jm_grx5 is a low power version which is described in section 7.1.3. In this version the filter output buffer of the previous version jm_grx1 is removed to save 7mA of current and therefore a degradation in conversion gain and noise figure is expected as well as an improvement in linearity.

7.1.1 Receiver front-end with improved linearity (version jm_grx4)

This version (jm_grx4) is an improvement over the previous version (jm_grx1) and was fabricated later in a different fabrication run (referred to as batch 2). The motivation to fabricate this chip was a desire to demonstrate improved linearity, as the input IP3 of the previous version jm_grx1 was not very good.

The schematic for version 2 is shown in Figure 7-1. This circuit is similar to version jm_grx1 (compare with Figure 6-1) except that the emitter of Q_6 is now AC coupled to the base of Q_7 by means of the series capacitor C_6, and both Q_7 and Q_8 now have identical

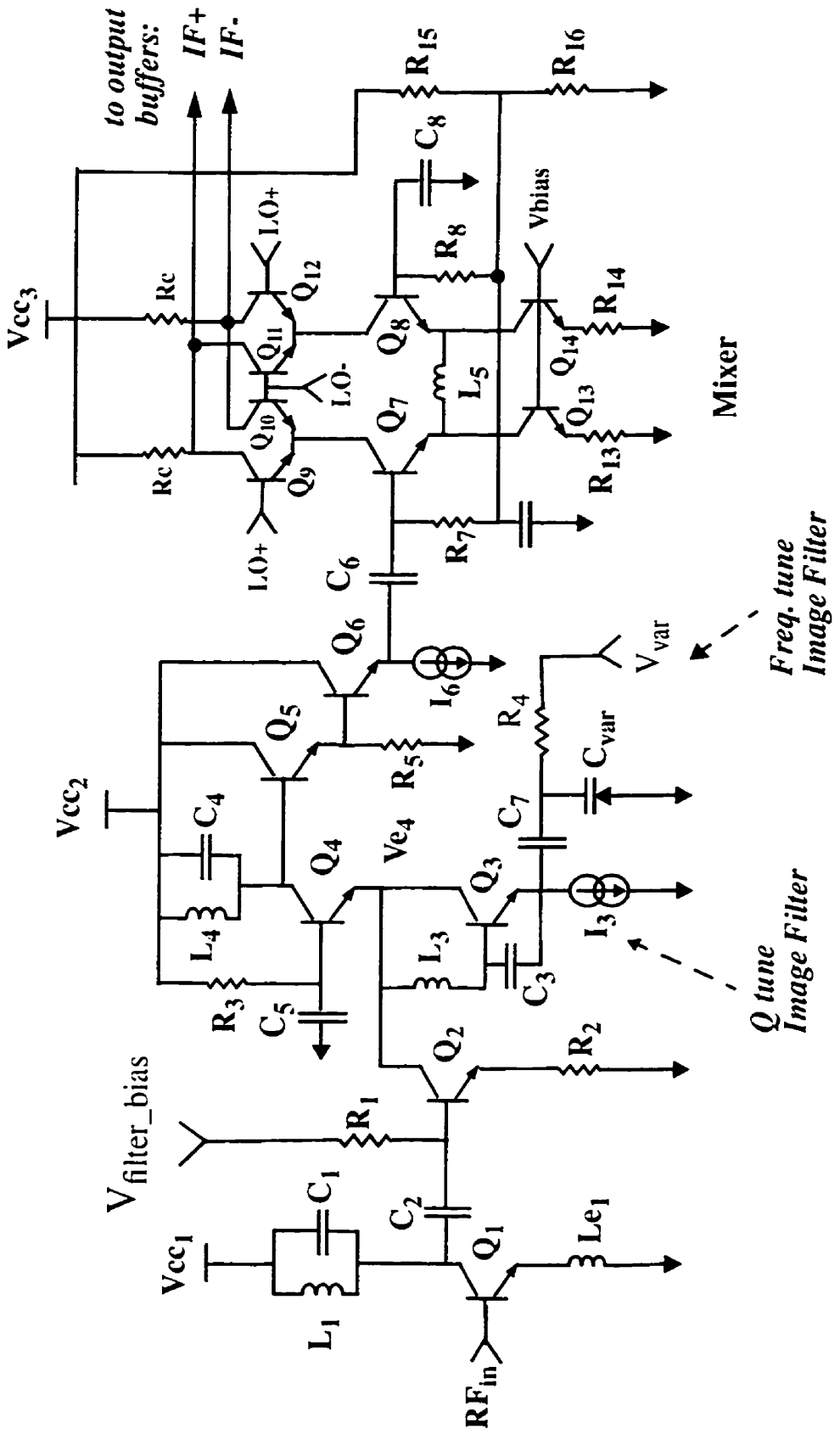

Figure 7-1: Low noise receiver front-end with improved linearity (version jm_grx4)

bias currents by applying the DC bias voltage to the common node of resistors R_7 and R_8. This DC bias voltage is now generated by the voltage divider consisting of on-chip resistors R_{15} and R_{16} (before, in version jm_grx1, the DC voltage available at the emitter of Q_6 was used). This biasing scheme ensures fully symmetric DC currents on the differential pair (Q_7, Q_8) and hence in the switching quad to ensure good balance and best isolation.

Also, in version jm_grx4 the mixer degeneration inductor (L_5) was doubled to 14nH to increase the mixer linear range and thus improve the overall receiver front-end linearity. Naturally this will increase the mixer noise figure, which however will impact little in the overall noise figure thanks to the gain which precedes the mixer.

As will be shown in the simulation results of section 7.2 the penalty for this improvement will be a relatively small degradation of 0.44dB in the noise figure. This penalty is small due to the fact that there is sufficient gain on the LNA with image reject filter module (25dB of measured passband gain as shown in section 4.4) to overcome the increased mixer noise (due to the larger size of inductor L_5).

A chip has been fabricated on NORTEL's 0.5 micron bipolar process (NT25) and the experimental results are described in section 7.1.2 which follows

7.1.2 Measurements of receiver front-end with improved linearity

This second version (jm_grx4) with improved linearity has more recently been fabricated and tested. This chip corresponds to fabrication batch 2 while the previous version (jm_grx1) presented in chapter 6 was fabricated in batch 1. Thus this experiment also shows the effect of process variation in the receiver performance.

This receiver front-end chip was packaged in a commercial 20TQFP plastic package and then mounted on a PCB and tested. On the PCB, 50 ohm microstrip lines were used for the RF, LO and IF signals. This chip was tested with its input properly matched to 50 ohms. First the input matching network is described in the next section and later the measured results are described in section 7.1.2.2.

7.1.2.1 Input matching network

The chip was input matched by means of an external LC network as shown in Figure 7-2 which is a simplified representation of the PCB showing the RF input trace with the SMA connector mounted at one end and the receiver chip mounted at the other end. Conceptually, this is the same matching network as used in chapter 6 to test version jm_grx1. In chapter 6 the PCB was laid out with a pin through hole for the RF input SMA which was positioned vertically, thus creating a discontinuity (90° bend). Also the SMA pin protruded on the bottom of the board by about 3mm. This made the matching more difficult and several experimental iterations were required before the matching was completed. However here the PCB layout has been improved to obtain a more controlled performance. One key improvement was the use of an SMA connector positioned horizontally so as to lay on the 50 ohm trace as shown in Figure 7-2.

In Figure 7-2 the LC matching network consisting of a series inductor L_m and a shunt capacitor C_m is clearly shown. L_m is a 3.9nH series inductor (surface mount inductor chip manufactured by AVX) and C_m a 0.8pF shunt capacitor (surface mount capacitor manufactured by AVX).

The microstrip line is broken in 2 segments (A and B) to allow the mounting of the matching inductor. Segment A is a short transmission line (approximately 3mm long) so as to position the inductor L_m as close as possible to the chip RF input pin. Unfortunately due to the small chip dimensions (very small pitch between pins), line A has to be very narrow and as a result its impedance is somewhat higher than 100 ohms. On the other hand microstrip line B is designed to be a 50 ohm transmission line and is 13mm long, mainly due to the physical dimensions of the overall PCB.

The matching was done experimentally in two steps. First a 3.9nH SMT inductor (L_m) was mounted on the board and the 1.9GHz S11 input reflection coefficient and input impedance observed with a properly calibrated HP8753C Network Analyzer. The measured value for S11 was 0.248 with an angle of +41.99° (inductive), this is referred to as point U.

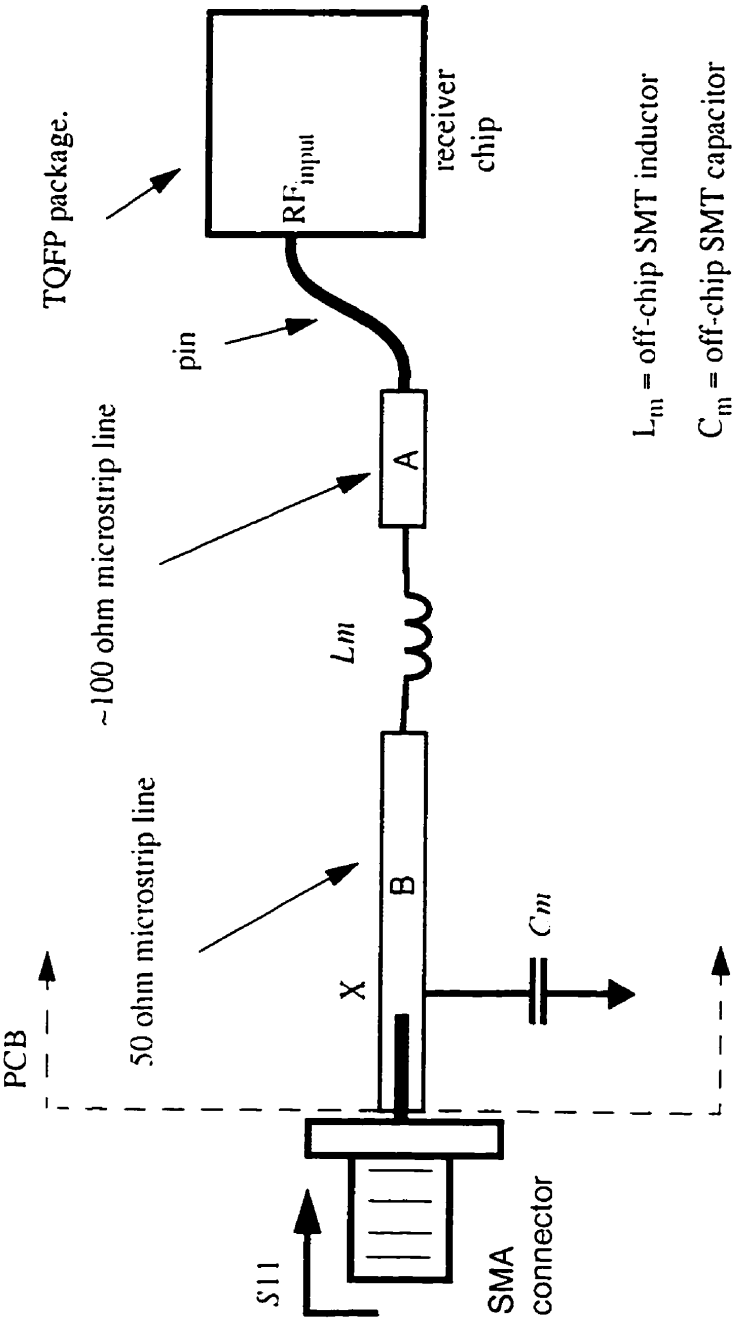

Figure 7-2: Receiver input matching network

Based on this measurement and with the help of a Smith Chart the appropriate location (indicated by an X in Figure 7-2) and the value of the matching capacitor (C_m) along the 50 ohm transmission line B were obtained as follows.

Starting at point U in the Smith Chart a constant amplitude circle was drawn which intercepted the unity admittance circle at point V. Point V had a 0.248 magnitude and an angle of 104°, that is 62° away from point U, thus defining the distance from the beginning of the SMA to the location X of the capacitor C_m. At point V the required shunt admittance to bring the input impedance to 50 ohms was read at +j0.5p.u. Using this value the required shunt capacitance value (C_m) for 1.9GHz frequency of operation was readily obtained as follows. First the required admittance was calculated by denormalizing the read value as follows:

$$y = y_{pu} \cdot \frac{1}{50\Omega} = j0.5 \cdot \frac{1}{50\Omega} = j0.01 mho \qquad (7.1)$$

Next the capacitor admittance is equated to this value as follows:

$$y = j0.01 mho = j \cdot \omega \cdot C_m = j \cdot 2\pi \cdot 1.9 GHz \cdot C_m \qquad (7.2)$$

From this equation a 0.837pF capacitance was calculated. The closest practical value was a 0.8pF capacitance which was then mounted into the PCB at the location indicated by an X in Figure 7-2.

Figures 7-3 and 7-4 show the input reflection coefficient (S11) measured with the HP8753C Network Analyzer in the log magnitude domain and in the Smith Chart respectively. The S11 value of -19dB indicates good matching. Figure 7-3 shows that the best matching point is actually at 1.95GHz with a -35dB S11, this indicates that by increasing the matching capacitor a little the best matching point could be moved to 1.9GHz. The corresponding Smith Chart shows the input impedance at 49 + j7.8 ohms, which is very close to the desired 50 ohms.

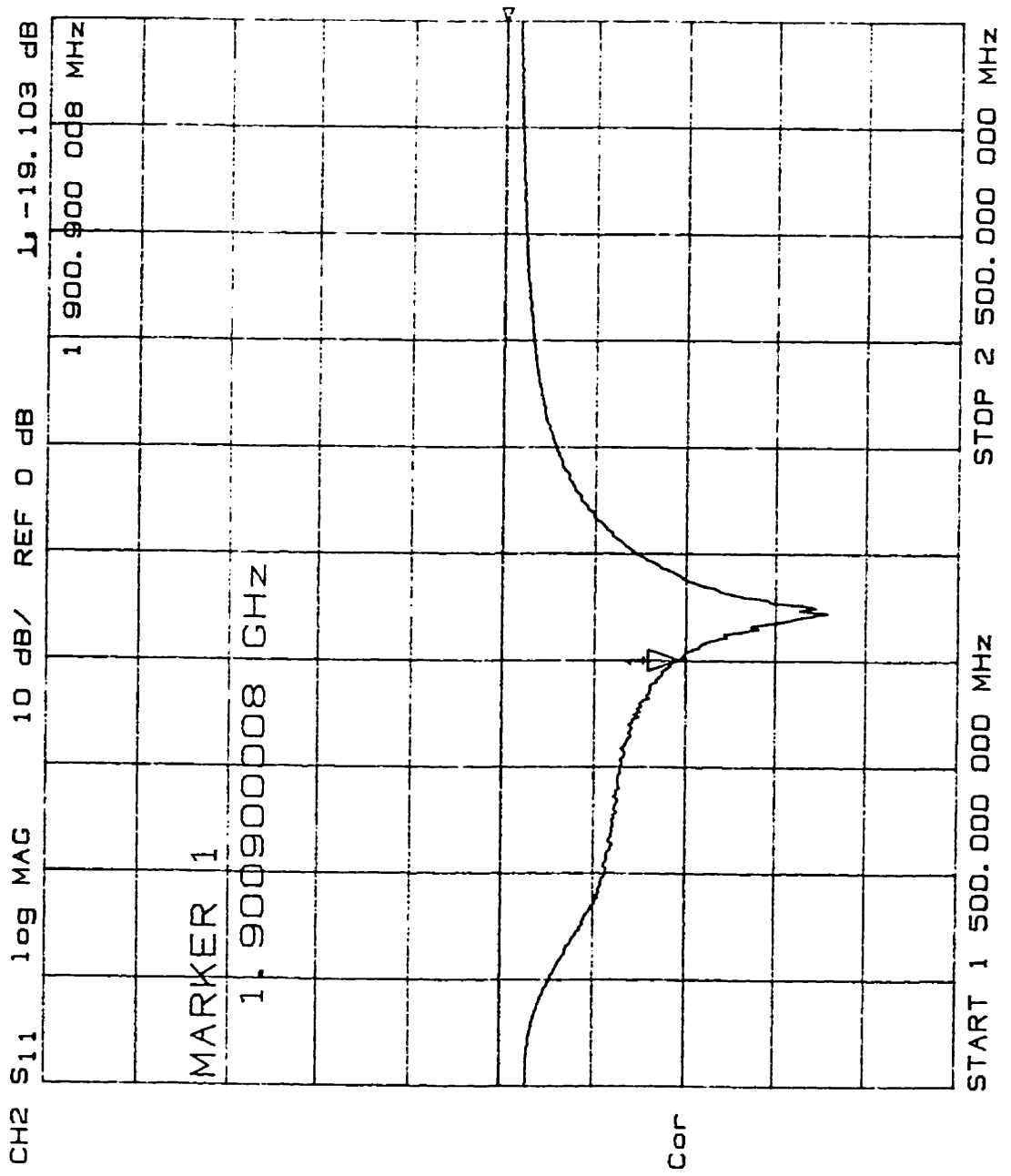

Figure 7-3: Measured input reflection coefficient (S11) for matched receiver (version jm_grx4)

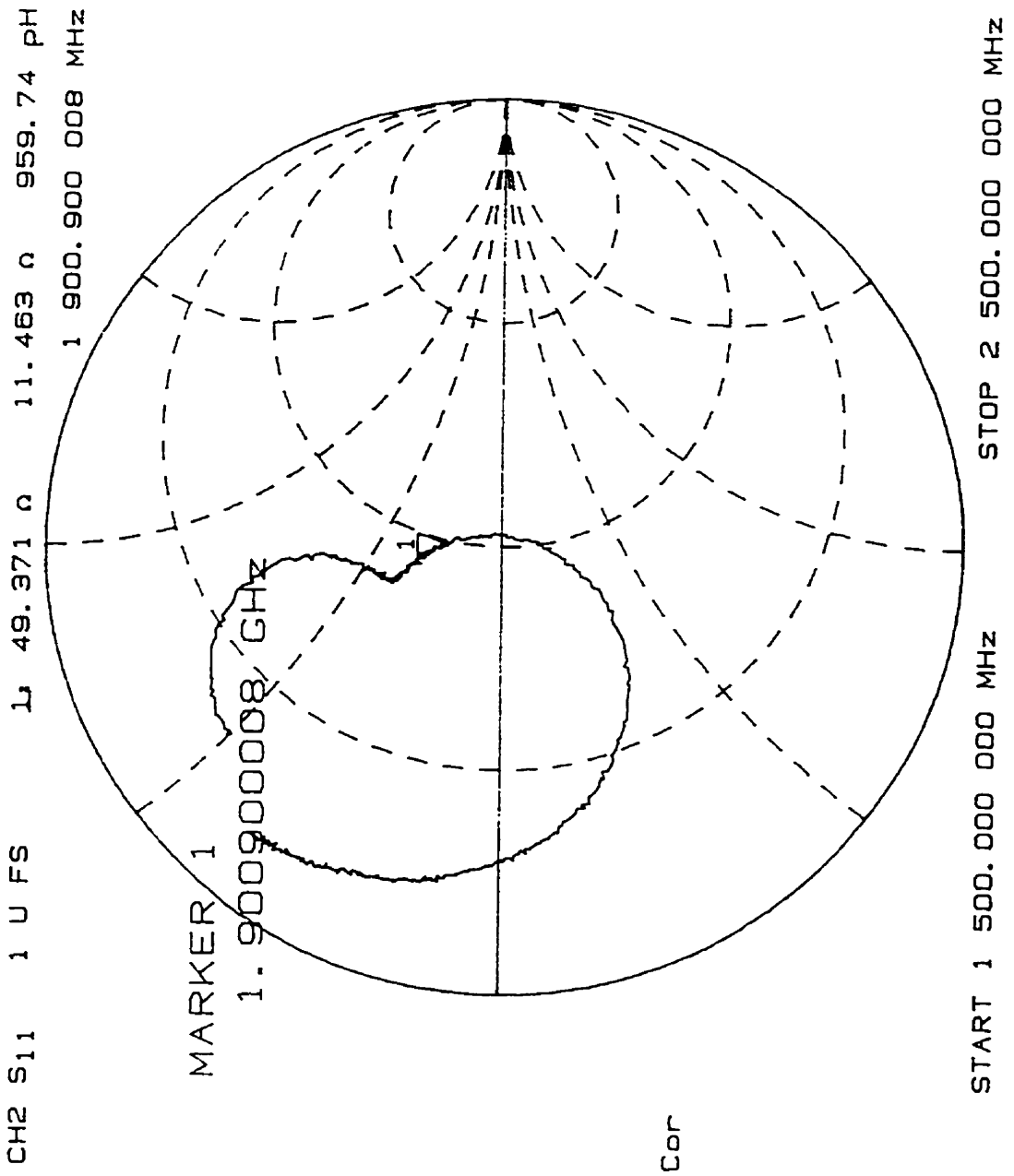

Figure 7-4: Input reflection coefficient (S11) for matched receiver (version jm_grx4)

7.1.2.2 Measured results for version jm_grx4

This chip is an improvement over the previous version jm_grx1 as the results below will demonstrate. This receiver chip was tested with its input matched to 50 ohms as was described in the previous section and with a 1.9GHz RF and a 0dBm 2.2GHz differential LO for a 300MHz IF. The differential LO was generated by feeding a +2dBm 1.9GHz single ended signal generated by an HP8663A generator into a 2 way 180° splitter. The generator is set at +2dBm to compensate for the losses in the splitter as well as in the coaxial cables involved.

The chip was first tested by applying a -40dBm 1.9GHz RF input. The measured single ended IF output spectrum is shown in Figure 7-5. The 300MHz IF is at -15.47dBm, hence the measured single ended conversion gain is 24.5dB. In this version the conversion gain (single ended) has thus reduced from the jm_grx1 value (33.5dB) of the previous chapter due to the reduction in the mixer conversion gain because of the increased inductor degeneration.

Due to discrepancy with the simulation (to be shown in section 7.3) the conversion gain measurement was later redone more carefully by adjusting the RF generator to cancel the losses due to the "bias T" and the coaxial cable connected to the RF input so as to have exactly -40dBm at the RF input SMA connector. Also this time the losses due to the "bias T" (used as a decoupling capacitor) and the coaxial cable connected to the IF output were measured and added to the gain. In this manner the corrected single ended conversion gain was found to be 26.3dB which is the value included in the summary of results (Table 7-1 ahead).

The spectrum of Figure 7-5 also shows the 2.2GHz LO leakage at -41.5dBm. Hence the LO-IF isolation is 41.5dB which compares favourably with existing state-of-the-art. For example compare with the image reject front-ends of Table 2-1. Or compare with 47dB LO-IF isolation measured on a BiCMOS doubly balanced mixer, which however used a lower LO frequency of 1.8GHz [35]. Or compare with the LMX2216B BiCMOS mixer manufactured by National Semiconductor which exhibits a typical LO-IF isolation of 30dB. Observe also that the LO to IF isolation of version jm_grx4 has been substantially

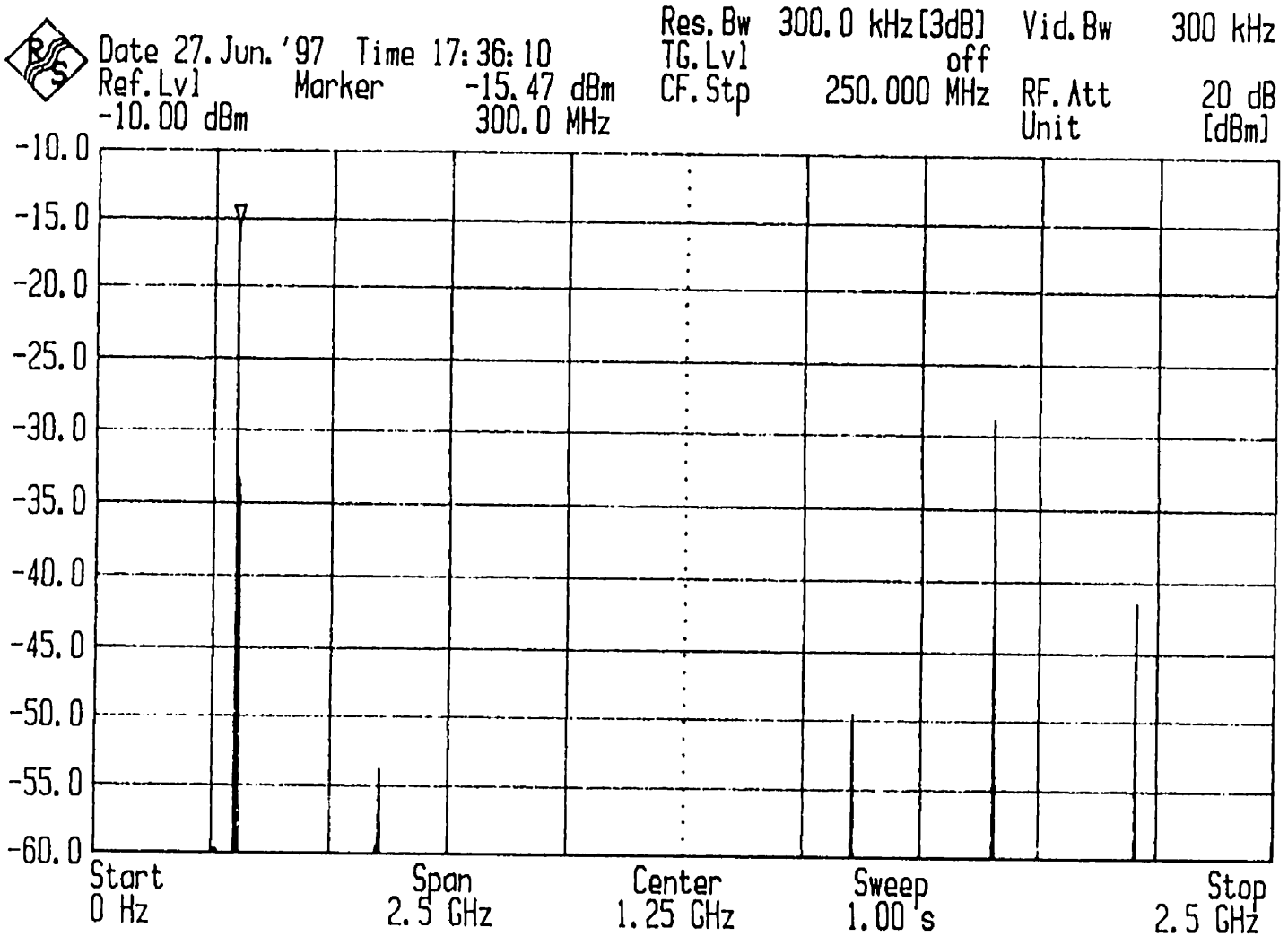

Figure 7-5: Measured single ended IF+ output spectrum for matched receiver (version jm_grx4) with a -40dBm 1.9GHz RF input and a 0dBm 2.2GHz differential LO.

improved from 25dB (on the previous version jm_grx1) to 41.5dB because now the mixer bias currents through Q_7 and Q_8 are fully symmetric.

In Figure 7-5 the RF leakage appears significant, (-29dBm at 1.9GHz). This is due to the 26dB passband gain of the LNA with image filter which amplifies the -40dBm RF at the receiver input to -14dBm at the mixer input. Thus the actual RF to single ended IF isolation in the mixer is 15dB. However this relatively large RF leakage is not of concern because this is only observed on a single ended IF measurement. When the output is used in differential mode (as this chip is intended to), this RF leakage signal is drastically reduced as is shown next.

Figure 7-6 shows the output IF spectrum when a 2way 180° combiner model ZAPDJ-2 manufactured by Mini-Circuits [56] (which acts as a balun transformer) is connected to the differential IF^+ and IF^- outputs to convert the differential IF output signal into a single ended signal which is then fed to the spectrum analyzer. Observe that now the 300MHz IF signal is larger at -11.2dBm for a total conversion gain of 28.8dB. This is 4.3dB larger than in the single ended case, which was -15.47dBm. Theoretically, a 6dB increase was expected, but this is not attainable due to the losses in the combiner, which are specified from 1.3 to 1.8dB in the corresponding data sheet [56], as well as the losses in the decoupling capacitors and the cables used for the connections.

Figure 7-6 shows a reduced RF leakage, now only at -44Bm, indicating that the RF leakage was mostly a common mode signal and therefore the differential connection substantially cancelled it. As mentioned before, due to the LNA and filter gain, the RF signal entering the mixer can be estimated at -14dBm and since the RF leakage at the IF output is -44dBm then the RF-IF mixer isolation is effectively 30dB, which compares very well with existing designs.

In Figure 7-6 it can also be observed that the 2.2GHz LO leakage has increased to -37.5dBm, which may indicate that the LO leakage is a differential signal (possibly due to mismatches of the mixer quad transistors) and therefore the conversion from differential to

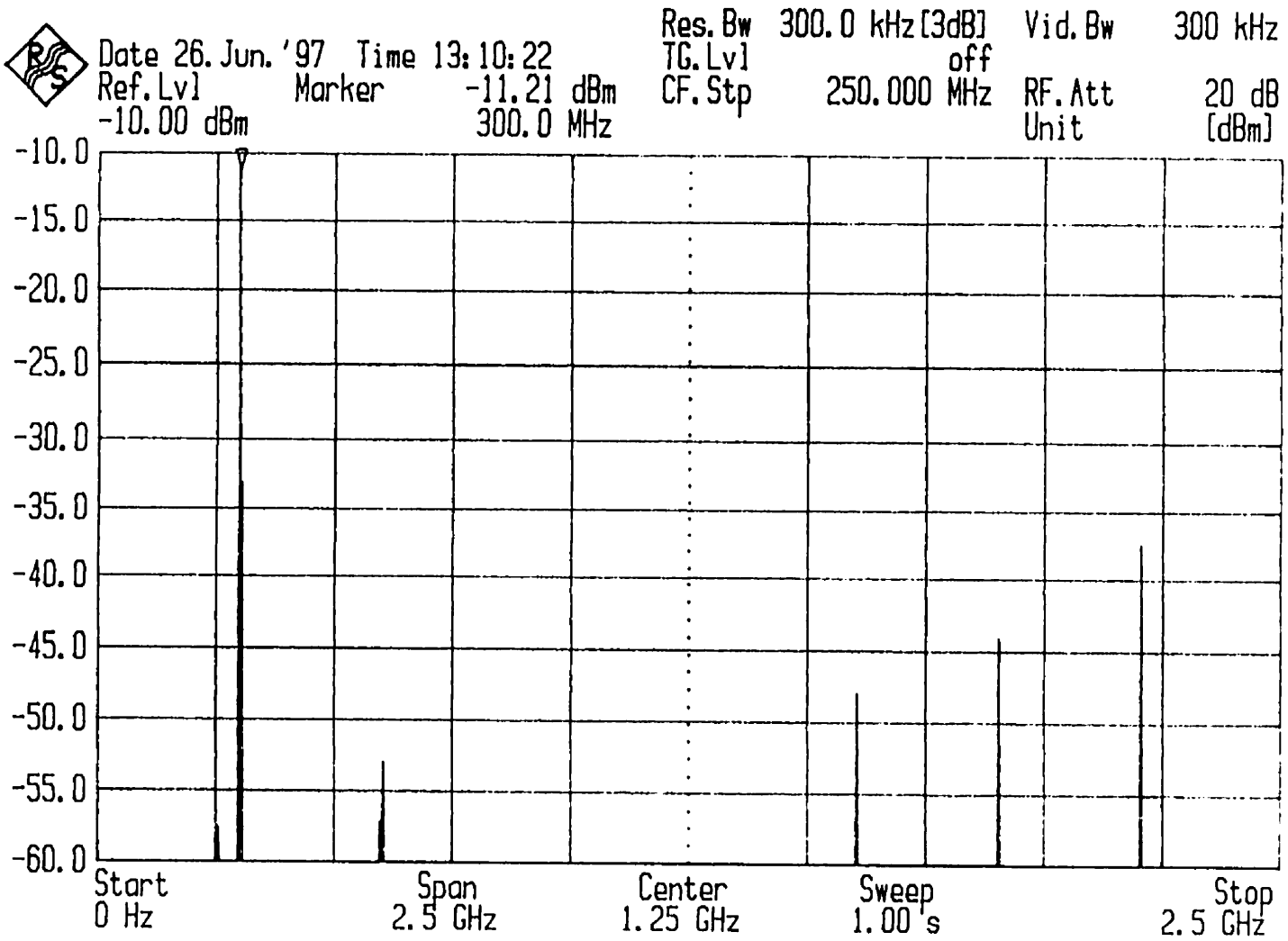

Figure 7-6: Measured differential IF output spectrum for matched receiver (version jm_grx4) with a -40dBm 1.9GHz RF input and a 0dBm 2.2GHz LO

single ended increases its power by approximately 4dB in the same manner as for the IF signal.

To measure the LO-RF isolation, only the 0dBm 2.2GHz LO signal was applied to the receiver and the spectrum analyzer was connected to the receiver input and a -61.1dBm 2.2GHz signal was observed. Hence, the measured LO-RF isolation was 61dB which ensures that little LO signal leaks back into the antenna. This is far superior to existing monolithic image reject front-ends (see Table 2-1 in which the best LO-RF isolation is 30dB for McDonald's chip [24]). Our receiver front-end yields superior isolation due to the presence of the image filter which does not exist in the image reject mixer approach.

The image rejection was tested by applying a -40dBm 2.5GHz image signal to the input of the receiver and then tuning the varactor voltage and the Q tuning current to minimize the undesired 300MHz IF output, to a value of -81dBm. Recall that the desired 300MHz single ended IF had been previously measured at -15.47dBm. Therefore the measured image rejection at 2.5GHz was 65.53dB. This is superior than all the surveyed monolithic image reject front-ends shown in Table 2-1, in which the best image rejection was 35dB for Pache's chip [25].

Additionally, the image amplitude was increased to -30dBm and it was verified that the image rejection remained the same. Next, the amplitude was decreased to -50 and -60dBm and it was observed that the undesired IF output decreased by the same amount. These tests indicated that the image filter linear range of operation was from very small signals up to -30dBm.

The measured image filter tuning range for jm_grx4 was 210MHz, from 2.34GHz to 2.55GHz corresponding to a varactor control voltage of 0 to 3V respectively. This tuning range is located at a lower frequency than version jm_grx1 due to process variation. However the tuning range still covers the required 2.5GHz image frequency.

On this improved version the noise figure was measured with an HP8970 Noise Figure meter properly calibrated for a 300MHz IF. The measured noise figure was 4.6dB. This result demonstrates that by having substantial gain in the LNA and image filter (1.9GHz

passband gain for the unmatched LNA with image filter was measured at 25dB in section 4.4) it was possible to double the mixer degeneration inductor (L_5) without degradation in noise figure. Indeed the noise figure improved from 4.9dB on jm_grx1 to 4.6dB on jm_grx4. This can be attributed to several factors: process variation, the improved mixer circuit which is now truly symmetric and the smaller TQFP package which minimizes wirebond impact on performance.

The measured 4.6dB noise figure is sufficient to meet a GSM requirement and compares very well with the present state-of the art. This measured noise figure is better than all the monolithic front-ends presented in Table 2-1 except for the Philips part UAA2077BM, which exhibits a typical 4.3dB noise figure, and the more recent UAA2077CM with 4dB noise figure which is included in Table 7-1 below for comparison. Compare also with the 4.3dB noise figure for the hybrid implementation presented in Table 2-3, which would combine a silicon LNA and mixer with an off-chip passive filter.

Passband linearity was tested by applying two -40dBm RF tones at 1.89GHz and 1.9GHz to the receiver input and observing the output IF spectrum. The input IP3 was then calculated using formula (1.6). The obtained input IP3 was -19dBm, which is 9dB better than version jm_grx1 due to the increased mixer degeneration. Since increasing the mixer linear range (by doubling its degeneration) did increase the receiver linear range (IIP3 increased from -28dBm for jm_grx1 to -19dBm for jm_grx4) it can be concluded that in this receiver front-end implementation the linearity at the passband frequency is directly limited by the mixer, not by the LNA or the filter.

Current consumption was 16.1mA at 3V DC, for a total power consumption of 48.3mW, that is approximately the same as in version jm_grx1. This power consumption is smaller than all the image reject front-ends surveyed in Table 2-1 and as shown in the table below is almost three times smaller than the 135mW consumed by the UAA2077CM part.

For comparison, Table 7-1 below summarizes the measured results for our receiver version jm_grx4 discussed in this section as well as for the state-of-the-art UAA2077CM 2GHz image rejecting front-end chip manufactured by Philips, which is an upgrade of the previously introduced UAA2077BM in chapter 2. In the author's opinion the Philips part

exhibits the best combined performance of all the surveyed image reject front-end chips. This part is aimed at DCS1800/PCS1900 applications which must comply which GSM like specifications.

In Table 7-1 all tests for jm_grx4 were done for a 300MHz IF and with a 0dBm 2.2GHz differential LO.

Table 7-1: Receiver measured results (version jm_grx4):

Parameter\Version	Philips UAA2077CM	jm_grx4 (matched)
RF frequency	1.805-1.99GHz	1.9GHz
LO frequency	1.617-1.802GHz	2.2GHz
IF frequency	188MHz	300MHz
Conversion Gain	23dB	26.3dB
S11	N/A	-19dB
NF	4dB typ (4.4dB max)	4.6 dB
Input IP3	-17dBm (-21.5dB min.)	-19dBm
Image Rejection	38dB ($f_{RF}>f_{LO}$)	>65dB @2.5GHz
Notch Tuning Range	not applicable	2.34/2.55GHz
RF-IF Isolation (mixer)	n/a	32.9dB
LO-IF Isolation	n/a	41.5dB
LO-RF Isolation	40dB	61dB
DC Current	36mA	16.1mA
Power Supply	+3.75V DC	+3V DC
Power consumption	135mW	48.3mW
Technology	BiCMOS	0.5micron bipolar
Package	SSOP20	20TQFP

Observe that version jm_grx4 easily meets the performance requirements for DECT described in section 1.3 and is indeed very close to meeting the requirements for GSM (the noise figure is sufficient for a GSM application while the linearity is only 1dB short of the required -18dBm IIP3).

Note also that a passive bandpass filter is normally connected before the LNA input as shown in Figure 1-5. This passive filter is typically a ceramic filter with losses in the order of 3dB and therefore its noise figure would be 3dB. Hence, this would degrade the receiver front-end noise figure by 3dB for a total of 7.6dB, thus still meeting the GSM requirement, but with no margin. But at the same time the passive filter loss would improve the IIP3 to make it -16dBm, thus meeting the GSM linearity requirement.

Furthermore, it is possible to increase the receiver linearity by increasing the mixer bias current. For example if the differential IF output was obtained by means of an off-chip transformer directly connected to the quad collectors (Q_9, Q_{10}, Q_{11}, Q_{12}) the DC drop on the collector pull-up resistors would be avoided and the mixer current could easily be doubled from 2.5mA to 5mA for a 6dB improvement in linearity. In such a case the overall receiver front-end input IP3 would improve from -19dBm to approximately -13dBm meeting the GSM requirements and the total current would increase from 16.1mA to 18.6mA at 3V DC.

Table 7-1 above clearly shows that our jm_grx4 receiver front-end compares very well with the best image rejecting receiver front-end available today in the market. The main advantage of the Philips part is in that it does not require tuning. Clearly, the jm_grx4 with on-chip tuning circuit would be very competitive. A further comparison including other chips, is done in section 7.5 at the end of this chapter.

Comparing the jm-grx4 results of Table 7-1 with Table 2-3 for Long's receiver front-end with off-chip image filter shows that this receiver front-end has much higher conversion gain (26.3dB versus 12.6dB), comparable noise figure (4.6dB versus 4.3dB), but poorer linearity (-19dBm versus -4.2dBm) precisely due to the large conversion gain. Note however that is possible to enhance the linearity of our monolithic receiver as briefly explained above.

Additionally, jm-grx4 would have higher image rejection (65dB) than the off-chip passive filter used with Long's receiver which would typically provide 30dB rejection. Finally, Long's receiver front-end requires only 8.55mW of power consumption versus 48.3mW for jm_grx4.

In an attempt to reduce power consumption two additional versions were developed which are presented in the following sections.

7.1.3 Low power receiver front-end (version jm_grx5)

A third receiver version explored in this work is a low power version (jm_grx5) shown in Figure 7-7. This version was studied because a very low power receiver front-end is very attractive for portable radio. This receiver front-end would consume only 8.5mA at 3V (26mW) for the complete receiver front-end with 3mA for the LNA, 3mA for the filter and 2.5mA for the mixer.

As shown in Figure 7-7 in this design, the filter output buffer (Q_5, Q_6) of the previous version (see Figure 7-1) has been removed, thus saving approximately 7mA of current. The filter is now directly connected to the mixer input by means of coupling capacitor C_6. As shown in Figure 7-7, no 50 Ohm interfaces are used here between modules. All interfaces are high impedance, on the order of 250 ohms. No matching networks are used within the chip, for example the LNA output impedance is not the complex conjugate of the filter input impedance. This is possible because all the circuits are relatively close to each other. Therefore the transmission line effects due to interconnections are greatly minimized, and even though the stages are not matched it is expected that problems due to undesired reflections will not occur. Also, circuits with a high load impedance automatically yield a higher voltage gain than circuits loaded with 50 Ohm impedances, for the same current, thus providing a power saving advantage over the conventional 50 Ohm impedance level circuits.

In this receiver version the mixer input impedance will directly load the filter and thus reduce the filter gain as well as detune the filter passband a little. This reduction in gain will degrade the overall noise figure but will also increase linearity. Observe that in this receiver version the emitter degeneration at the filter input transistor Q_2 is now being implemented with an on-chip inductor (L_2), instead of a resistor, for improved noise performance to partially offset the noise figure degradation due to the reduction of gain.

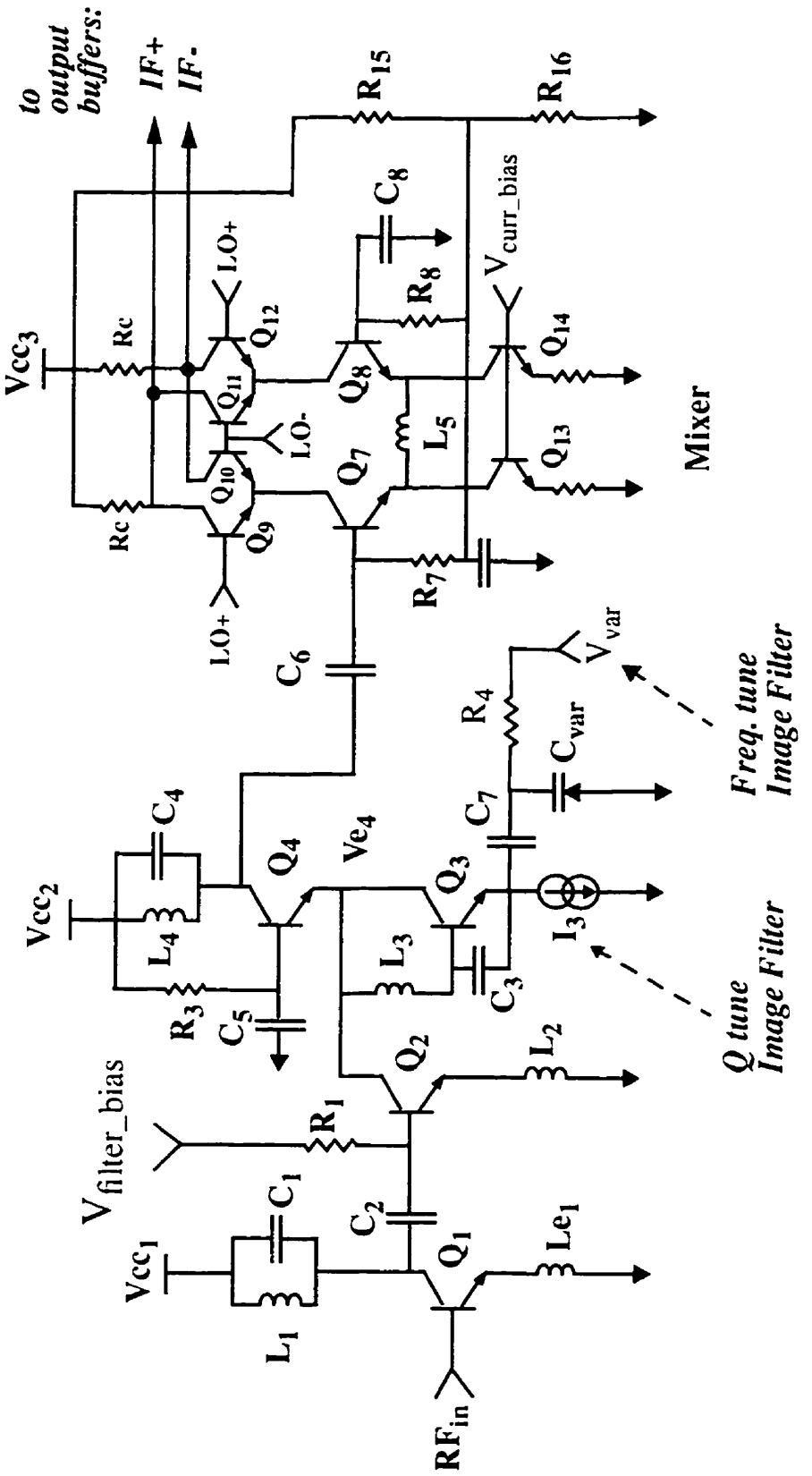

Figure 7-7: Low power receiver front-end with Gilbert mixer (jm_grx5)

The bias current through the mixer input differential pair Q_7, Q_8 is established by current sources Q_{13} and Q_{14} which are controlled by the DC voltage applied to the V_{curr_bias} input. The bases of Q_7 and Q_8 are symmetrically biased by applying a DC voltage to the common node of identical resistors R_7 and R_8, which ensures that both transistors will have identical currents. This DC bias is generated by an on-chip resistive network consisting of R_{15} and R_{16}.

As the schematic shows this circuit now contains 6 on-chip inductors. Thus careful component placement is required to minimize the possibility of crosstalk. In actual fact the layout contains 7 inductors because L_5 is implemented by connecting 2 spiral inductors in a symmetric manner to realize a fully symmetric L_5. This is needed because the square spiral inductor is not symmetric.

The simulated results for this receiver are included further ahead in section 7.2 and show that the simulated performance of this low power receiver front-end is sufficient to meet the DECT specification. But first the actual performance measured on a packaged device is presented in section 7.1.4 that follows.

7.1.4 Measured low power receiver (version jm_grx5)

This third version (jm_grx5) with reduced power consumption was the last chip tested for this exploratory work. This circuit was described in section 7.1.3.

The receiver front-end chip was packaged in a commercial 20TQFP plastic package and then mounted on a PCB. On the PCB, 50 ohm microstrip lines were used for the RF, LO and IF signals. The chip was input matched by means of an external LC network consisting in this case of a 4.7nH series inductor (surface mount chip inductor manufactured by AVX) and a 0.5pF shunt capacitor (surface mount capacitor manufactured by AVX). The input matching network arrangement is the same as described in section 7.1.2.1 but with the component values just mentioned.

The chip was tested using a 0dBm 2.2GHz differential LO. The supply voltage was 3V DC. An external "bias T" was used to bias the LNA transistor Q_1 to 2.7mA. The filter

transistor Q_2 was biased at 2.5mA by adjusting the bias voltage V_{filter_bias} while the mixer total bias current was set at 2.5mA by adjusting the V_{curr_bias} DC voltage.

Once the off-chip matching network was mounted, the input reflection coefficient (S11) was measured at -17dB, indicating good matching. A carefully calibrated -40dBm RF input was then applied to the chip and the single ended IF spectrum was observed to verify conversion gain and isolation. The 300MHz IF was found to be -13.8dBm. The conversion gain was obtained by subtracting -40dBm from -13.8dBm and adding the 0.5dB losses due to the "bias T" (used for AC coupling) and the coaxial cable connected at the IF output. This resulted in a 26.7dB single ended conversion gain.

Next a -40dBm 2.5GHz image signal was applied to the RF input and the varactor control voltage and the notch control voltage were carefully tuned for best rejection. The 300MHz output IF image was then below -90dBm indicating an image rejection better than 75dB at the center of the notch.

This was followed with a 2 tone intermodulation test in which two -40dBm RF tones, one at 1.9GHz and the other one at 1.89GHz, were combined and applied to the receiver input. The IF^+ output was observed in the spectrum analyzer while the IF^- output was properly terminated with a 50ohm load. The IF^+ spectrum showed the two desired IF signals at 300MHz and 310MHz with amplitudes of -14.1dBm and -14.3dBm respectively. Additionally the third order intermodulation products could be seen located at 290MHz and 320MHz were -49.7dBm and -50dBm respectively. Based on these values and using formula (1.6) the input IP3 of -22.2dBm was obtained.

Next the noise figure was measured with an HP8970 Noise Figure Meter properly calibrated for a 300MHz IF. The meter indicated a noise figure of 5.6dB. Finally, the reverse isolation from LO to RF input was measured. The 0dBm LO was applied to the receiver and the spectrum analyzer connected to the RF input. A -55dBm 2.2GHz leakage signal was observed. Thus the LO-RF isolation is 55dB.

The measured results are summarized in the table below.

Table 7-2: Low-Power receiver measurements (jm_grx5):

Parameter	jm_grx5 (matched)
RF frequency	1.9GHz
LO frequency	2.2GHz
IF frequency	300MHz
Conversion Gain	26.7dB
Input reflection coeff. (S11)	-17dB
NF @ 1.9GHz	5.6 dB
Input IP3	-22dBm
Image Rejection (@2.5GHz)	> 75dB
Notch Tuning Range	2.34/2.55 GHz
RF-IF Isolation (mixer)	30dB
LO-IF Isolation	40dB
LO-RF Isolation	55dB
DC Current	8.6mA
Power Supply	+3V DC
Power consumption	25.8mW
Package	20TQFP

The results shown in this table indicate that this receiver front-end would be suitable for a DECT application while requiring only 25.8mW of power consumption at 3V DC, which is lower than any of the monolithic image reject downconverters surveyed in chapter 2.

Comparing these results with version jm_grx4 of Table 7-1 one can see that the price paid for the reduction in power consumption is a degradation of both the noise figure and the linearity (the noise figure is 1dB poorer and the linearity is 3dB poorer than version jm_grx4). However the image rejection is still very good and better than all the image reject chips surveyed in chapter 2.

The RF-IF and LO-IF isolations are still similar to version jm_grx4. The LO-RF isolation was also very good at 55dB but 6dB poorer than version jm_grx4, which can be attributed to the removal of the Darlington buffer (Q_5, Q_6 in Figure 7-1).

7.2 Simulations of receiver front-ends with Gilbert mixer

The typical simulation results with NORTEL's 0.5 micron bipolar technology (NT25) for the receiver front-ends with a Gilbert cell mixer are summarized in the table below. For comparison, the table also includes the first version (jm_grx1) which was presented in chapter 6 as well as the improved versions jm_grx4 and jm_grx5 introduced in this chapter.

Table 7-3: Simulation of receiver front-ends with Gilbert mixer

Parameter/Version	jm_grx1	jm_grx4	jm_grx5
Noise Figure	3.5dB	3.94dB	4.1dB
Conversion Gain (1.9GHz RF, 300MHz single ended IF)	34.4dB	26.7dB	31.5dB
Input IP3	-28dBm	-20.3dBm	-21dBm
Current @ 3V DC	16mA	16mA	9mA
Mixer Degeneration	7nH	14nH	7nH

The results shown in Table 7-3 were obtained with a 1.9GHz RF input and 0dBm, 2.2GHz differential LO for a 300MHz single ended IF output. The power supply was 3V DC and the receiver input was matched to 50 ohms by means of an off-chip LC network. These simulations were done at the schematic level (without layout parasitics) using SeriesIV HPEESOFV6.0 simulator ("Libra").

Unfortunately, the Series IV HPEESOFV6.0/Libra simulation to obtain the input IP3 for the receiver front-end aborted. The input IP3 results presented in table 7-3 are estimates based on the LNA and filter gain combined with the estimated mixer input IP3. These estimates agree reasonably well with the experimental measurements presented in sections 7.1.2 and 7.1.4. The -28dBm input IP3 for jm_grx1 was estimated as described before in chapter 6, based on this value the input IP3 for jm_grx4 was obtained by adding to -28dBm the same amount that the gain decreased due to the doubling of the mixer degeneration. The simulated conversion gain decreased from 34.4dB for jm_grx1 to 26.7dB for jm_grx4.

The difference is 7.7dB and therefore the input IP3 for jm_grx4 can be estimated by adding 7.7dB to -28dBm which results in a -20.3dBm input IP3.

As Table 7-3 shows the simulated noise figure and linearity of all these versions are sufficient to meet the DECT requirements. They also exhibit sufficiently low noise figure to meet the requirements for a GSM application but fail to meet the required linearity, which is -18dBm input IP3. Note however that the estimated input IP3 for version jm_grx4 is very close to meeting the GSM linearity requirement. The measured input IP3 for jm_grx4 was -19dBm (see section 7.1.2.2) which confirms this estimate.

Comparing the simulated performance of jm_grx1 and jm_grx5 we can see a clear trade-off of NF versus linearity (input IP3). For example, jm_grx1 yields the lowest noise figure (3.5dB), the highest gain and the weakest input IP3 while jm_grx5 yields poorer noise figure (4.1dB) and lower gain but superior input IP3.

Version jm_grx4 has a mixer degeneration inductor which is twice that of jm_grx1. As table 7-3 shows jm_grx4 has slightly larger noise figure (0.44dB larger) than jm_grx1 but significantly lower conversion gain (7.7dB smaller) and consequently better linearity. Thus, a NF versus linearity performance trade-off has also occurred. However in this case the increased degeneration has a minimal impact on the noise figure, due to the large gain (25dB measured @ 1.9GHz) of the LNA with image rejection circuit which precedes the mixer. This has been confirmed with the experimental measurements.

It is interesting to point out that perhaps some form of automatic gain control (AGC) could be used to turn off the LNA or to reduce the mixer gain in the presence of large signals. This is the approach taken by Marshall et al. [13]. In their receiver they use two LNAs in cascade which yield a total of 20.5dB gain, and the LNAs can be turned on and off by means of switches.

In summary, these simulations showed very promising results which encouraged the continuation of the work. These simulations are compared with measured results in the following section.

7.3 Simulation versus measurement

It is important to assess the validity of the simulations. Therefore in this section we compare simulated versus measured results for versions jm_grx4 and jm_grx5. Recall that these are schematic based simulations without layout parasitics and were done with the HPEESOF/Libra simulator. Table 7-4 below compares the simulated (from Table 7-3) and measured results (from Table 7-1) for version jm_grx4.

Table 7-4: Results for matched receiver version jm_grx4

Parameter	Libra Simulation	Measured (TQFP pkg)
Noise Figure	3.94dB	4.6dB
Conversion Gain (1.9GHz RF, 300MHz single ended IF)	26.7dB	26.3dB
Input IP3	-20.3dBm	-19dBm
Current @ 3V DC	16mA	16.1mA

The results of Table 7-4 were obtained with a 1.9GHz RF input and 0dBm, 2.2GHz differential LO for a 300MHz single ended IF output. The power supply was 3V DC and the receiver input was matched to 50 ohms by means of an off-chip LC network

This table shows generally good agreement between the simulated and the measured results, thus validating the simulation. Sources of error could be process variation, inaccuracies in the modelling of the transistors and the package as well as calibration errors. Additionally the Libra simulations did not include layout parasitics and did not include an accurate model for the TQFP package. These simulations were done assuming only 1nH wirebonds, however in practice the package pin also adds additional inductance as well as parasitic capacitance. It is important to accurately model the package pins and the wirebonds because they can influence the passband response. For example wirebond which connects the LC tank at the LNA collector (transistor Q_1 in schematic Figure 7-1) to

the Vcc power supply is in series with the tank and will modify the collector load impedance. A similar situation applies to the image filter. Similarly the wirebonds that connect the chip ground pads to the actual package ground plane have finite inductance which will tend to degrade the gain a little.

From our experience a measured noise figure is invariably poorer than its simulated value and in this case a 0.6dB discrepancy is not surprising. The above sources of error could also explain the fact that the measured conversion gain is 0.4dB below the simulated one. Observe also that a loss of gain is consistent with a degradation of noise figure (if there is less gain before the mixer the overall noise figure will be degraded).

To complete the comparison the following table presents the simulated versus measured results for the low power version jm_grx5.

Table 7-5: Results for matched receiver version jm_grx5

Parameter	Libra Simulation	Measured
Noise Figure	4.1dB	5.6dB
Conversion Gain (1.9GHz RF, 300MHz single ended IF)	31.5dB	26.7dB
Input IP3	-21dBm	-22dBm
Current @ 3V DC	9mA	8.6mA

The results for version jm_grx5 (Table 7-5) show more discrepancy between simulation and measurement than for the previous version jm_grx4 of Table 7-4. The measured conversion gain is 4.8dB below the simulation value. This lesser gain could be due to process variation as well as the influence of the TQFP package on the receiver performance. This reduction in gain would explain the increased noise figure which is 1.5dB higher than the simulation. For example if there is less gain on the LNA, or in the filter, then there is less gain in front of the Gilbert cell mixer and the noise figure will increase.

Observe in the schematic of Figure 7-7 that the total capacitance at the collector of Q_4 includes now the capacitance seen at the base of transistor Q_7 which is process dependent. Thus, this may detune the filter passband with a loss of gain at 1.9GHz. By comparison version jm_grx4 has a buffer at the filter output which ensures that the passband gain is independent of the mixer input impedance. Observe also that the inductor L_2 will have larger inductance than its simulated value due to the connections to it thus increasing the degeneration and reducing the gain. However, the estimated input IP3 agrees well with the measurement.

These results would indicate that the low power design is less robust against process variation and package parasitics than the previous version jm_grx4. However, it may be possible to improve this receiver by doing a very accurate simulation and observing if all the stages were optimally tuned or not.

7.4 Receiver front-end with transformer coupled mixer

In this realization the LNA and image reject filter module is connected to a balanced mixer which uses a transformer balun at its RF input as was described in section 5.4. This receiver is referred to as version jm_mrx6. The completed circuit shown in Figure 7-8 consisting of LNA, non-tunable image reject filter and transformer coupled mixer in one die, has been laid out and fabricated on NORTEL's 0.5 micron bipolar process. The chip was successfully tested and the results will be shown in the following section.

As explained in section 5.4 the mixer design used here is a modification of a transformer coupled mixer first fabricated in 0.8micron BiCMOS by J.Long [35]. Long's design is attractive because it can work at very low voltages and also because the balun converts the singled ended RF input into a perfectly balanced (differential) signal required to drive the mixer quads and ensure good isolation.

Long designed his mixer for 50 ohm input impedance and as a consequence his transformer balun had a 4:5 turns ratio. However, in our integrated receiver, a high impedance is preferred at the filter cascode collector (Q_4) output in order to maintain good gain and ensure overall low noise figure. Thus for the present work a balun transformer with a 4:2 ratio was designed, so as to increase the mixer input impedance to a value given by the square of the turns ratio times the load seen at the switching quad emitters, which for a bias current of 2.5mA (through transistor Q_{13}) is approximately 50 ohms. With an ideal transformer the input impedance would be 200 ohms, but in a silicon transformer the coupling coefficient is in the order of 0.75 to 0.8 and so the expected balun input impedance would be lower, probably below 150 ohms. Note that this input impedance could be increased by increasing the transformer turns ratio but this was not attempted due to time constraints.

Now the primary of the balun transformer can be connected directly to the filter cascode collector (Q_4) as shown in the schematic of Figure 7-8. Hence no output buffer is required to drive the mixer, thus saving power consumption. Capacitor C_4 is selected to resonate the balun primary at the desired 1.9GHz passband.

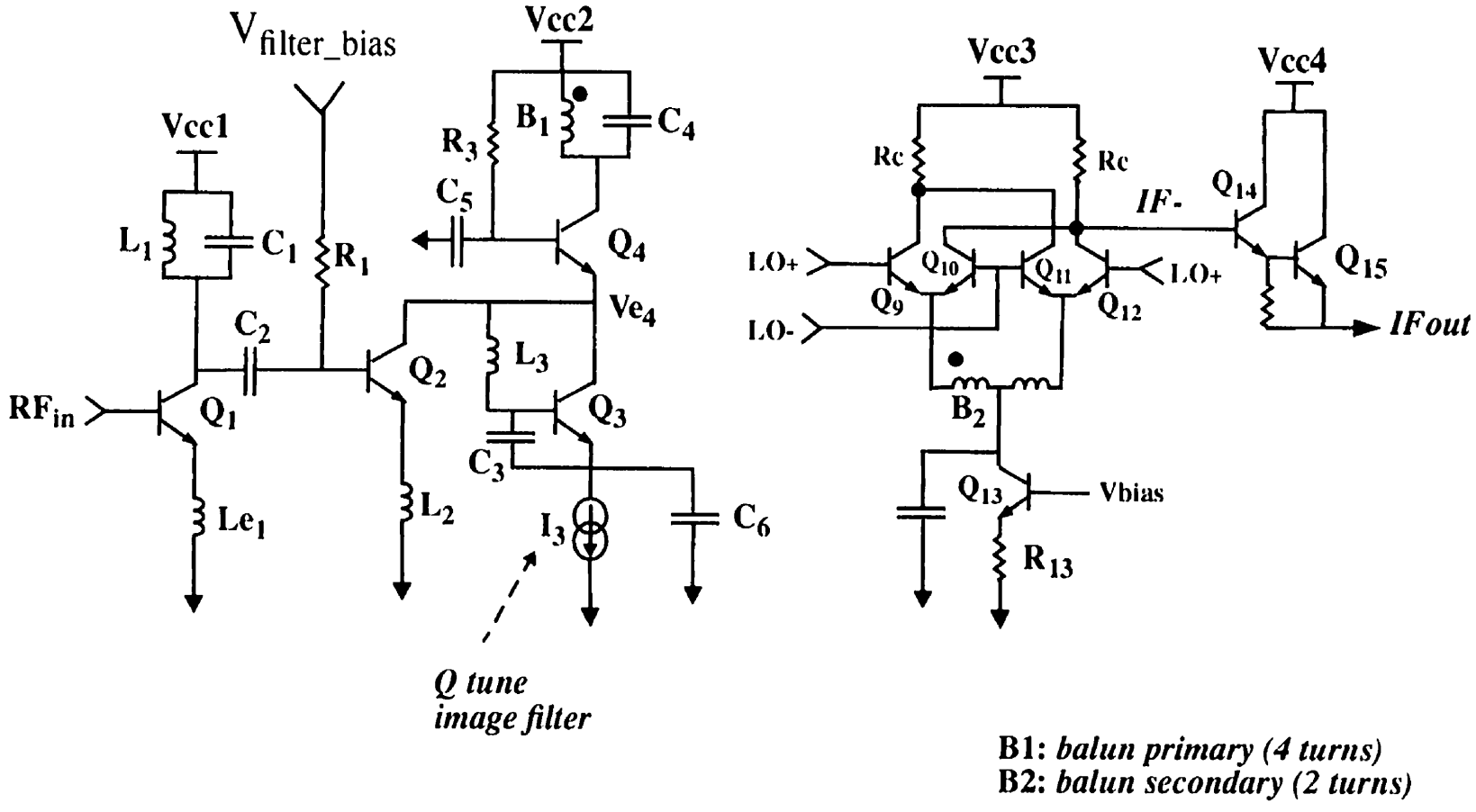

Figure 7-8: Receiver front-end with transformer coupled mixer

This receiver front-end was packaged and mounted on a printed circuit board for testing. The circuit can be tested with either single ended or differential output. In this test the output buffer consisting of a Darlington pair (Q_{14}, Q_{15}) was used for single ended output, which was useful for a quick functionality test. However common mode interferers will be still present.

The key objective of this experiment was to prove functionality and stability of the receiver with a transformer coupled mixer, verify whether substrate coupling was a problem or not (due to the large area of the transformer there was a concern of the transformer picking up substrate noise) and measure performance, particularly noise figure and linearity. RF-IF and LO-IF isolation were also of interest. Successful experimental results are shown in section 7.4.2.

7.4.1 Layout of receiver with transformer coupled mixer (jm_mrx6)

The micrograph of the layout for the receiver transformer coupled mixer is shown in Figure 7-9. Again three stages can be distinguished: the LNA on top, the image filter in the middle section and the mixer on the lower part of the chip. Four spiral inductors can be seen on the upper portion of the chip and the balun transformer (the largest structure) can be seen on the lower portion of the chip. Each inductor is surrounded with a guard ring for better isolation.

The LNA has two inductors, the one to the left forming the emitter degeneration inductor (L_{e1}) and the one to the right (L_1) forming the LNA collector tank. The filter in the midsection has also two inductors, the one at the left (L_3) forming part of the series resonator and the one the one to the right (L_2) the emitter degeneration. The collector of the filter cascode (Q_4) is connected to the primary of the balun.

The lower part of the chip is the mixer in which the balun (4 turns in the primary, 2 turns in the secondary) occupies most of the space. The balun measures 400 x 400 microns and is realized with top metal aluminum with 13.8micron line width and 3 microns linespacing. The windings are fully symmetric to ensure proper operation. Observe that sufficient

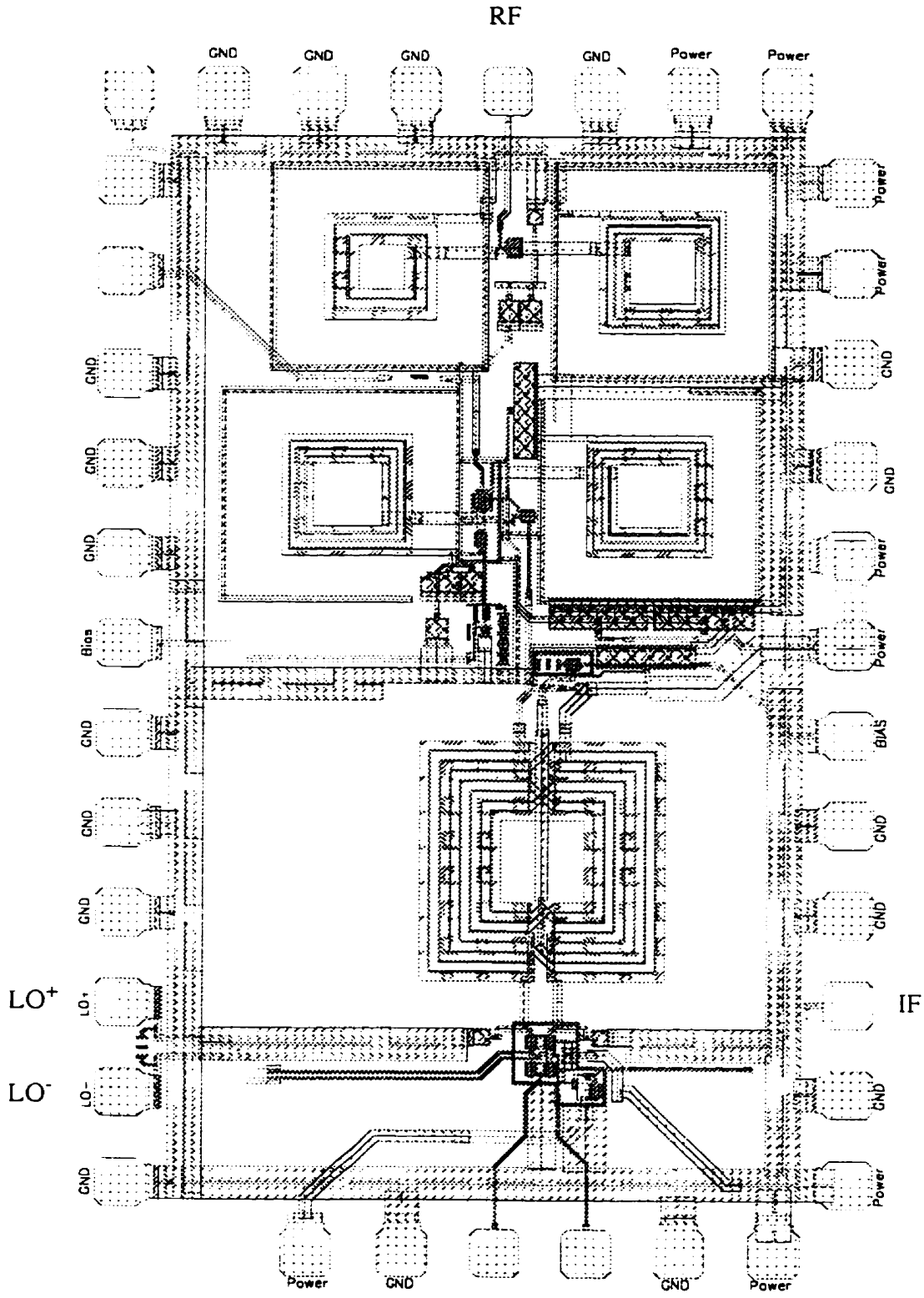

Figure 7-9: Receiver with transformer coupled mixer on 0.5 micron bipolar

clearance is left between the balun and the surrounding metal traces to avoid affecting the balun behaviour.

The RF input is at the top, the differential LO inputs are at the left and the single ended IF output is at the right hand side. These pads are positioned orthogonal to each other to minimize crosstalk between the wirebonds which will be connected to them.

7.4.2 Measured performance of receiver with transformer coupled mixer

This chip version, fabricated on Nortel's 0.5 micron bipolar process, has a non-tunable image filter as shown in the schematic of Figure 7-8. The intention of this experiment was primarily to verify circuit functionality and to compare the performance of this approach with the receiver front-ends which use the conventional Gilbert cell mixer.

The notch filter deliberately does not have a varactor, to simplify the circuit modelling by removing one variable. In this circuit, the model for the balun transformer is very important for proper simulation. Thus, in this experiment one key objective was to first prove functionality, then compare this receiver results with the Gilbert cell approach and third attempt a highly accurate simulation to validate the model for the balun. However, due to time constraints only a low frequency model was used for the balun to quickly obtain a rough simulation result and proceed with layout and fabrication. With a high frequency model for the balun and an extracted netlist which included capacitive and inductive parasitics a fair comparison of measured versus simulated results could be done. This was not completed due to time constraints.

The chip was packaged in a 44CQFP package and mounted on a PCB. The receiver was not input matched for simplicity. The circuit functioned well. A 2.2.GHz differential LO was applied to the circuit. This differential LO was generated with an HP8663A RF generator which fed a 2.2GHz single ended signal into a ZAPDJ-2 Mini-Circuits differential splitter [56]. Each output of the differential splitter was then calibrated to -3dBm for a total differential power of 0dBm into the receiver LO^+ and LO^- inputs.

The table below shows the measured results for a single ended IF at the output of the Darlington buffer.

Table 7-6: Measured results for receiver with transformer coupled mixer (0.5 micron bipolar):

Parameter	jm_mrx6
RF frequency	1.9GHz
LO frequency	2.2GHz
IF frequency	300MHz
Conversion Gain	24.6dB
S11	n/a (unmatched)
NF @ 1.9GHz	9.5 dB
Input IP3	-21dBm *
Image Rejection (@2.46GHz)	> 50dB
Notch frequency (fixed)	2.46GHz
RF-IF Isolation (mixer)	33 dB
LO-IF Isolation	25dB
LO-RF Isolation	58dB
DC Current	8.6mA
Darlington buffer current	10 mA
Power Supply	+2.5V DC
Package	44CQFP

* Note: to obtain the -21dBm input IP3 and 24.6dB gain the output Darlington buffer had to be biased with a 10mA current. When the output buffer was biased to 5mA the gain was 20.5dB and the input IP3 reduced to -26dBm indicating that the output buffer was limiting the circuit linearity.

Based on the above table, version jm_mrx6 meets the performance requirements for DECT while having very low power consumption (21.5mW), as it can work with only 2.5V. Thus this receiver consumes the lowest power of the versions developed in this work.

The table also shows that the receiver with transformer coupled mixer has poorer noise figure than the receiver with Gilbert cell mixer (compare with 4.6dB NF for jm_grx4 in section 7.1.2.2 or with 5.6dB NF for the low power version jm_grx5 in section 7.1.4). This is the result of two factors, as follows.

First, the transformer coupled mixer is relatively noisy as explained in section 5.4, mainly due to the fact that the balun transformer used here has a 4 to 2 turns ratio, thus degrading the SNR. Second the mixer input impedance, that is the impedance seen at the primary of the transformer (B1 in Figure 7-8), is relatively low, thus degrading the passband gain of the image filter. Since the overall NF is dependent on the gain before the mixer, this degrades the overall noise figure. This has been verified with simulations as follows.

Hspice simulations indicate that the gain from LNA input to the filter output (collector of the cascode transistor Q_4 in Figure 7-8) for this version is approximately 10dB lower than the corresponding one for the receiver with Gilbert mixer (version jm_grx4 in Figure 7-1) thus explaining why the transformer version has poorer noise figure.

In the receiver with Gilbert mixer of Figure 7-1 the cascode collector is loaded with an LC tank realized with an on-chip inductor (L_4) in parallel with an on-chip capacitor (C_4). Hence for the receiver with Gilbert mixer the cascode (Q_4) collector load at resonance (1.9GHz) is in the order of 300ohms due to the Q of the 3.5nH inductor, which is in the order of 6 to 7. On the other hand, as explained in section 7.4 for the transformer coupled mixer, the primary of the transformer has an impedance in the order of 150 ohms due to the 4:2 transformation ratio, the load connected to its secondary as well as the non ideal coupling factor, which is in the order of 0.7 to 0.8 for a silicon transformer (an ideal transformer has a coupling factor of 1). Hence, the cascode collector load for the receiver with transformer coupled mixer is substantially smaller than the corresponding one for the receiver with Gilbert cell mixer.

For these reasons the gain from LNA to filter output is reduced and this impacts in the overall receiver front-end noise figure according to Friis formula (1.3). Hence, the

reduction in gain before the mixer explains why the receiver with transformer coupled mixer yields poorer noise figure than the receiver with Gilbert mixer.

Note however that this circuit was a first prototype and possibly could be improved. A careful simulation could be done to ensure that the balun primary is properly tuned for the desired 1.9GHz passband, otherwise the gain is being degraded. The balun model used here was only a low frequency lumped model. For more accuracy a high frequency model for the balun could be developed which would allow to more accurately predict performance and fine tune the circuit. Additionally, the transformer turns ratio could be optimized, for example increasing the turns ratio to increase the impedance seen at the primary of the balun and enhance the gain. Also, key connection lines should be modelled as transmission lines to ensure better simulation accuracy. This was not done due to lack of time. However it is felt that the demonstration was still very valuable as a proof of concept.

Observe also that the LO-IF isolation is only 25dB while the simulations done in chapter 5 predicted much larger values. This could be partly due to the package itself, which is a large package with 4mm wirebonds. Hence, even though the IF and LO wirebonds are approximately orthogonal to each other, there could still be significant coupling between them thus degrading the isolation.

7.5 Comparison of monolithic image rejecting front-ends

It is somewhat difficult to classify and compare the existing monolithic implementations due to the differences in fabrication technology, operating voltage, packaging and cost. In an attempt to compare the various existing designs a figure of merit (A) is proposed here. In a receiver front-end it is desired to have high conversion gain, very low noise figure, very high image rejection and naturally the lowest possible DC power consumption. Hence in a manner similar to Larson [1] who compares LNAs using the Gain in dB divided by the power consumption in mW, for our case a figure of merit could be:

$$A = \frac{Gain + ImageRejection - NF}{DCPower} \Rightarrow (dB/mW) \tag{7.3}$$

where the Gain, the Image Rejection and the Noise Figure are in dB while the power is in mW. This formula was used on the data obtained from Table 2-1 and our results in Tables 7-1 and 7-2. The following table resulted:

Table 7-7: Comparison of monolithic image rejecting front-ends

Part	Gain	NF	Image rejection	DC Power	A(dB/ mW)
McDonald [24]	7.6dB	18dB	14.1dB	59.4mW	0.06
Baumberger [26][27]	34dB	6.5dB	33dB	215mW	0.28
Pache [25]	17dB	n/a	25-35dB	60mW	n/a
UAA2077CM Philips [28]	23dB	4dB	38dB	135mW	0.42
jm_grx4	26.3dB	4.6dB	65dB	48mw	1.81
jm_grx5	26.7dB	5.6dB	75dB	25.8mw	3.72
jm_mrx6	24.6dB	9.5dB	50dB	21.5mW	3.03

This table clearly shows that based on the proposed figure of merit the integrated receiver front-ends presented in this work (versions jm_grx4, jm_grx5 and jm_mrx6) outperform the other designs. Hence exploiting the on-chip LC resonators and transformers to implement tuned circuits and filters results in receiver front-ends with a performance advantage.

Keep in mind however that the designs presented here require tuning to achieve the desired image rejection while the other designs use the conventional image reject mixer which does not, in principle, require tuning, although Pache [25] did use tuning to achieve very good rejection.

Die area has not been included in the above table. Our receiver version jm_grx4 requires approximately 1.1 x 1.5 mm^2 of active area, most of which is occupied by the inductors.

However an image reject mixer requires two mixers, various phase shifters and an adder which also increase die area. For example Pache's image reject mixer occupies $2mm^2$ of die area, as was shown in Table 2-1. Hence, the receivers developed in this work have similar die area to reported image reject mixer chips. However, to this area one would have to add the die area required for on-chip tuning circuitry.

Based on these results we conclude that the implementation of on-chip tuning circuit for the receivers presented here is justified and is recommended as a follow up to this work. Naturally, depending on the cost in terms of DC power required for the tuning circuitry the figure of merit will be affected. However note that our versions have sufficient margin to easily allow for say 10mW or 20mW of additional power while still being very competitive.

More recently, Rudell [57] reports a CMOS integrated receiver with 45dB image rejection coming from the mixer portion of the receiver. However its performance is suitable only for DECT, with a sensitivity of -90dBm, while GSM requires -102dBm sensitivity. This design uses 6 mixers to perform the image rejection and therefore the intermodulation products may be of concern. The power consumption is relatively large, with 41mW for the LNA alone and 51mW for the mixers, for a total of 92mW at 3.3V. This receiver was not included in the above Table as its noise figure was not known.

It is also important to compare our results with the hybrid receiver front-end using Long's BiCMOS ICs, previously presented in Table 2-3. Assuming that the off-chip passive filter provides 30dB image rejection, the figure of merit for Long's receiver would be 4.47, which is then superior to all the monolithic implementations presented in Table 7-7. Note however, that for the figure of merit developed for this work, the monolithic receivers of this thesis, particularly jm-grx5 in Table 7-7, compare well with Long's receiver.

Chapter 8 Discussion and conclusions

8.1 Review

A first milestone of this research was the development of a monolithic image reject filter. It was found that a notch filter with the notch placed at the undesired image frequency was an attractive solution for monolithic implementation due to low power and circuit simplicity. The notch filter requires "Q tuning" to obtain a deep notch. A 2.5GHz notch filter with 50dB image rejection was first demonstrated on a packaged chip fabricated on NORTEL's 0.8micron BiCMOS process. This result showed that at the present time the proposed notch filter is more attractive than a bandpass filter for monolithic implementation because the circuit is stable, even with very high Qs, and therefore very high image rejection can be obtained. As a following step, the notch frequency was then made tunable by means of an on-chip varactor in order to precisely center the notch frequency at the desired value and to compensate for process variations. The theoretical analysis, the design methodology and the criteria to ensure circuit stability of this notch filter were developed as part of the thesis work.

It is important to observe that an on-chip image filter need not be exclusive but can be complimentary to the image reject mixer approach. Hence, an on-chip image filter could be followed with an image reject mixer to obtain a very high on-chip image rejection. This would greatly alleviate, or possibly eliminate, the requirements of external image filtering.

Our next proposed milestone was to complete the integration of a 1.9GHz receiver front-end consisting of LNA, tunable image reject filter and mixer in one die. The receiver was designed for a 2.2GHz LO and 300MHz IF. This included analysis of the design trade-offs (such as noise figure versus linearity), impedance matching issues, and possible interference problems. Since no off-chip components are required there is no need for 50 ohm impedance levels between the various stages and therefore, to maximize voltage gain relatively high impedance levels (200-250 ohms) were used throughout.

Two receiver front-end implementations were explored in this work. The first one uses the well known Gilbert cell mixer and the second one a transformer coupled mixer previously

developed at Carleton University [5]. The receiver with Gilbert cell is more conventional and simpler to analyze but requires a 3V supply, (perhaps as low as 2.7V but not lower). The receiver with Gilbert cell has been enhanced by using on-chip inductors for the degeneration and it is relatively easy to model. On the other hand the transformer coupled mixer has been demonstrated to work at 1.9V and is therefore attractive for low power operation. However it is more difficult to understand, design and simulate. In the transformer coupled mixer the input differential pair has been removed and for this reason it is not straightforward to evaluate linearity. An accurate model of the transformer is required as well which is more complicated than an inductor model.

The chip measurements were done on packaged devices. The chips were packaged on a NORTEL's in-house package (44CQFP package) and in a commercially available plastic 20TQFP package which minimizes the wirebond lengths. The packaged devices were mounted on PCBs specifically designed for the test. The receiver front-end chips were tested with their input matched to 50 ohms whenever possible.

The basic measurements were Conversion Gain, NF, input IP3, image rejection and power consumption. Additional measurements included input reflection coefficient (S_{11}) and isolations (RF to IF, LO to IF and LO to RF). All the tested receiver front-end chips functioned well, with no oscillatory tendencies observed.

The receiver front-ends with the Gilbert cell mixer yielded excellent performance. The low noise version, referred to as jm_grx4, was tested with its input matched to 50ohms. A single ended conversion gain of 26.3dB and a noise figure of 4.6dB were measured, with a -19dBm input IP3 (which is 1dB away from meeting GSM requirements) and the image rejection was a substantial 65dB (for a 2.5GHz image) with 16.1mA current consumption at 3V DC, for a total power consumption of 48.3mW. The lower power version (jm_grx5) was also tested with its input matched to 50 ohms. Its measured single ended conversion gain was 26.7dB and the noise figure was 5.6dB with an input IP3 of -22dBm. The image rejection was still very good; an impressive 75dB rejection was measured. The supply current was only 8.6mA at 3V DC, for a total power consumption of 25.8mW. Note that although not as good as jm_grx4, this low power version meets DECT requirements.

The receiver front-end with transformer coupled mixer was more difficult to design due to the need for designing and modelling the transformer. Its performance was poorer than the Gilbert version due to lower gain before the mixer, as the input impedance of the transformer coupled mixer was lower than that of the Gilbert cell mixer, thus loading more heavily the image filter and degrading the gain. This chip was able to work with a 2.5V DC supply for a total power consumption of 21.5mW. The measured conversion gain without input matching was 24.6dB at 1.9GHz, with a 9.5dB noise figure and a 50dB image rejection for an image located at 2.46GHz. This performance is still sufficient to meet DECT requirements.

Generally, the measured data confirms the simulations (with some discrepancies) and thus validates the models used. Measured noise figure was always poorer than typical simulation but reasonably close. To improve simulations it would be necessary to accurately model the package parasitics. This information was not available at the time of this work and so it was not included in the simulations. The simulations did included bond wires which were approximated as 1nH inductors as their length in the TQFP package is approximately 1mm.

Simulated and measured results have shown performance trade-offs (such as NF versus linearity). Successful experimental measurements have demonstrated functionality and stability as well as good performance. Hence, this work demonstrates that the proposed notch filter technique works well for image rejection, very high Qs can be obtained and the circuit stability is guaranteed.

The measured isolations were very good, indicating that for these chips substrate coupling was minimal. At the beginning of this work there was a concern that the inductors (and transformer) could potentially pick up substrate interferers, especially in the presence of large signals such as the 2.2GHz local oscillator (0dBm). Another concern was that the amplified RF signal could feed back to the input stage and possibly create oscillations. This did not happen, indicating that the layout was satisfactory and that the mutual coupling between wirebonds and between package pins was minimal.

In summary, an important contribution of this work is the demonstration of a fully monolithic superheterodyne receiver front-end with performance suitable for portable radio applications. Our research indicates that this would be the first monolithic receiver front-end with on-chip filtering for the image rejection.

Previous monolithic realizations use various versions of the conventional image reject mixer, which typically yielded an image rejection of approximately 30dB, although a brand new Philips part (UAA2077CM) shows an impressive 38dB image rejection while meeting GSM requirements. A very recently reported CMOS receiver [57] exhibits an overall image rejection of 55dB, of which 8dB is contributed by the LNA and 45dB by their image reject mixer version, which uses 6 mixers. This receiver is only suitable for DECT due to limited sensitivity, because its noise figure is not very good.

In a completed receiver a passive bandpass filter is typically used before the LNA providing 20 to 30dB of image rejection. However to achieve performance suitable for cellular radio substantial additional image rejection is required. For example for DECT, 80dB would be required. Hence, a monolithic receiver front-end with a minimum on-chip rejection of 50dB would be desirable while at the same time having very low noise figure, high linearity and low power consumption. Ideally, performance suitable for GSM and with very low power consumption is desirable.

This research shows that using on-chip inductors and sub-micron processes such as NORTEL's 0.5 micron bipolar process (NT25), it is now possible to implement high performance RF integrated circuits previously realized only with discrete off-chip components. Hence, the work presented here will contribute to the increase of the integration level of portable radio receivers, as well as the understanding of the issues encountered in the realization of low power fully monolithic receiver front-ends.

8.2 Claims

A summary of claims is as follows:

- The circuits developed in this thesis have demonstrated that on-chip LC resonators and transformers can be effectively used to increase the level of integration of existing superheterodyne receivers.
- A comparison with state-of-the art monolithic image reject mixers shows that our receiver front-ends outperform the conventional image reject mixer in terms of image rejection and power consumption. This is due to the use of monolithic LC resonators and transformers. Therefore the development of on-chip filter tuning is justified.
- The integrated receiver front-end developed here provides an alternative to the well known image reject mixer. Additionally the monolithic image filter is perfectly compatible with the image reject mixer approach, so that both methods could be combined to realize very high monolithic image rejection.
- Demonstrated viable monolithic image rejection on silicon using a notch filter instead of a bandpass filter. This approach yields a stable filter with very high Q. The notch was realized using a series LC resonator and a negative resistance circuit to enhance the on-chip inductor Q. The filter transfer function was derived as part of this work.
- As part of the above demonstration, designed, fabricated and tested a 2.5GHz image reject filter in 0.8micron BiCMOS. This was the first time that a monolithic notch filter for image rejection was reported [31]. The circuit was stable and demonstrated more than 50dB of image rejection.
- Designed, fabricated and tested a 1.9GHz LNA with tunable image reject filter on Nortel's 0.5 micron silicon bipolar process (NT25). Simulated noise figure of the input matched circuit was 3.1dB, which was close to meeting the GSM requirement. On-wafer measured frequency response showed excellent passband gain of 25.1dB at 1.9GHz and with a deep notch tunable from 2.33GHz to 2.55GHz for a total rejection of 58dB. This tuning seemed adequate to compensate for process variations. Measured input IP3 was -12.5dBm which was sufficient to meet the GSM requirement.
- A 1.9GHz LNA with non-tunable image rejection was carefully studied to validate the simulations. The netlist was extracted from the layout and including capacitive as well

as inductive parasitics. Nine chips fabricated on Nortel's NT25 process were measured on-wafer. Our results show that the measured notch frequency (2.481GHz) was on average within 3.8% of the simulated notch frequency (2.58GHz). This experiment validated the simulations. showed the good quality of the process and demonstrated that for good accuracy inductive parasitics must be included.

- Demonstrated for the first time a 1.9GHz fully monolithic silicon superheterodyne receiver front-end with integrated image reject filtering. The first receiver version (jm_grx1) consisted of an LNA, image filter and Gilbert cell mixer in one silicon die. Measurements demonstrated that the proposed image filter worked very well, was stable and with excellent image rejection (65dB). This work was reported in [54] and the results have been accepted for publication in the IEEE Journal of Solid State Circuits.

- A second improved receiver with better linearity (jm_grx4) demonstrated excellent performance. Measured noise figure was 4.6dB, with 26.3dB single ended conversion gain, 65dB image rejection and -19dBm input IP3. Normally, a ceramic bandpass filter would be installed at the receiver chip input. Such a completed receiver would practically meet the GSM requirement (PCS1900).

- A third version (jm_grx5) also with Gilbert cell mixer demonstrated very low power consumption (25.8mW) for the whole receiver front-end while maintaining excellent performance. Noise figure was 5.6dB, with 26.7dB single ended conversion gain and -22dBm input IP3 and 75dB image rejection. This receiver meets the requirements for DECT operation.

- Additionally, a receiver front-end consisting of LNA, image filter and transformer coupled mixer was demonstrated. To implement this receiver Long's mixer was redesigned in 0.5 micron bipolar and with a new 4:2 on-chip balun transformer. This circuit yielded measured performance suitable for DECT operation and was able to function at 2.5V while consuming only 21.5mW, the lowest power of the versions developed here.

8.3 Future work

As mentioned above, the tunable image filter requires frequency and Q tuning, as would any continuous time filter in the GHz range. Others have looked in general at on-chip filter tuning [58][59][60]. The thrust of the present work has been to demonstrate a monolithic receiver front-end with performance good enough for portable radio applications and with viable sensitivity to tuning parameters. This then validates the effort of adding on-chip tuning.

In the following paragraph, we reflect on the possibilities for on-chip tuning. Various candidate approaches are briefly described.

Approach1: A master-slave approach. These schemes slave the performance of a filter to a master VCO which uses the same basic topology as the filter. Examples of successful high frequency implementations are the work of Aparin [58] and Katzin [59].

In Aparin's work the control circuit generates both the frequency control and the Q-factor control voltages which are used for the slave filter (the filter being tuned). Each control circuit contains a master VCO, which is identical to one of the sections of the slave filter, so its resonant frequency is equal to the slave filter center frequency. The oscillation amplitude is maintained at a level low enough to ensure small signal behaviour of the master oscillator and tuning varactors. As a result, its characteristics remain well matched to the slave filter resonators.

Katzin [59] applied the same concept to automatically tune a notch filter and demonstrated excellent results. A notch filter implemented with GaAs MESFET devices was automatically tunable from 8.2GHz to 10.9GHz. Furthermore, the measured performance of the notch filter over temperature showed that the control circuit virtually eliminated the temperature induced notch depth variation.

In the master-slave approach the master VCO is dedicated exclusively to the task of tuning the image filter. The control loop automatically keeps both the frequency and the Q of the filter tuned at all times. With this scheme when the receiver channel is switched the image filter could be immediately adjusted correspondingly for best image rejection. The penalty

is in the die area required to implement the master VCO and the control loop. which is essentially a phase lock loop (PLL).

Approach 2: Self tuning method as proposed by Plett [60]. This is also a master-slave approach in which a master filter is tuned for the desired transfer function and the tuning voltage or current is also applied to the slave filter which is carrying the signals to be filtered. In this approach, a voltage controlled filter (VCF) forms the master filter which is then phase locked to a reference signal. Plett demonstrates his approach by self-tuning a notch filter. He does not use the voltage-controlled notch filter output for the locking because the output signal is too small in amplitude to reliably lock. Instead Plett relies on a known phase shift (90^{o}) of an intermediate node so as to have a large signal to ensure good phase locking.

Approach 3: Undesired image IF amplitude measurement. This approach would consist of replicating the manual tuning procedure on-chip.

The image filter manual tuning procedure consisted of feeding the receiver front-end with a -40dBm 2.5GHz undesired image signal (and a 2.2GHz LO), observing the undesired 300MHz IF output in a spectrum analyzer and then adjusting the varactor voltage (V_{var} in the schematic of Figure 7-1) to center the notch while also adjusting the Q tuning current (I_3 in schematic Figure 7-1) to make the undesired IF output as small as possible. Usually this required two or three iterations, alternatively adjusting the Q tuning current, then the varactor voltage and so on until a very small IF was obtained.

To replicate the above tuning procedure on-chip the following elements would be needed: a 2.5GHz image signal, a way of measuring the 300MHz undesired IF, a means of adjusting the varactor voltage to center the notch filter and finally a means of adjusting the Q tuning current I_3 in order to minimize this undesired IF, that is, to obtain a deep notch at 2.5GHz.

The 2.5GHz image could be precisely generated by the upconversion portion of the transceiver and in such a case no extra cost would be required. This assumes that a separate VCO is being used in the transmitter.

The undesired 300MHz IF could then be measured by using the normal IF detection method to convert the IF signal into a digital number. This number would then be read by a microcontroller which would compare it to a threshold (a small value close to zero). If the IF signal is still too large the microcontroller would then send a digital number to a D/A converter in order to adjust the varactor voltage and/or the Q tuning current in the proper direction to reduce the IF. After a few iterations the minimum IF should be obtained. This operation could be done once during power-up or cyclically if required.

Another approach could be to use the master-slave approach to only tune the center frequency of the image filter. That is, only the varactor control voltage of the VCO would be used while for the Q tuning the IF measurement approach could be used.

The above paragraphs clearly show that electronic tuning is feasible and that there are various ways of implementing it. However, the development of the on-chip electronic tuning is a significant task well beyond the scope of this work, due to time constraints, and will be left to future workers.

Chapter 9 References

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IMAGE EVALUATION
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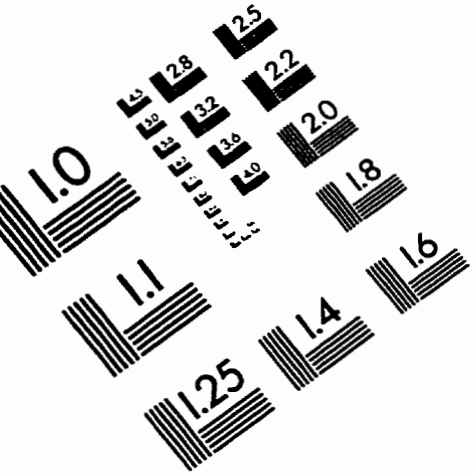

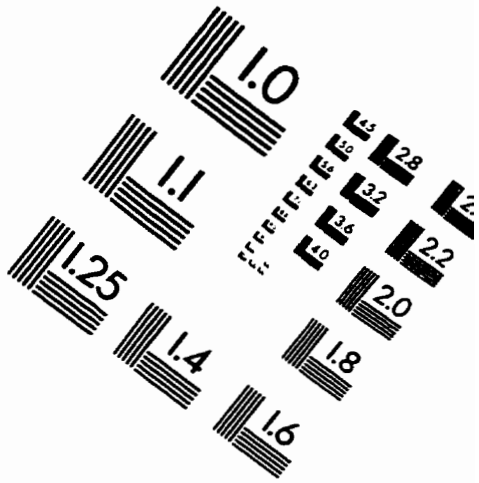

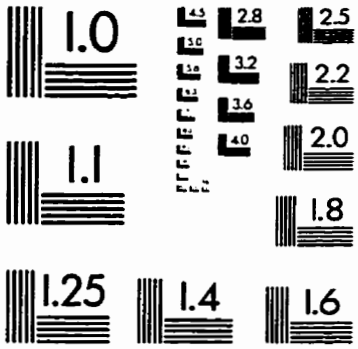

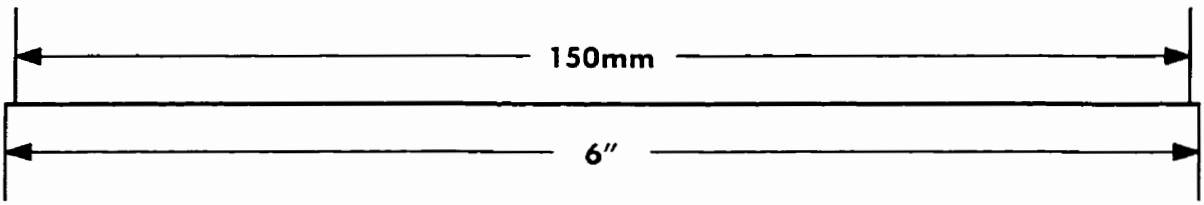

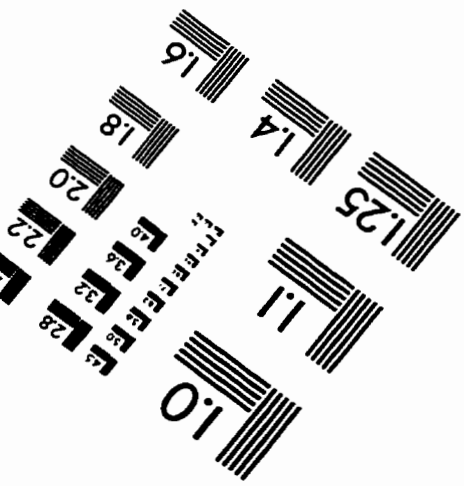

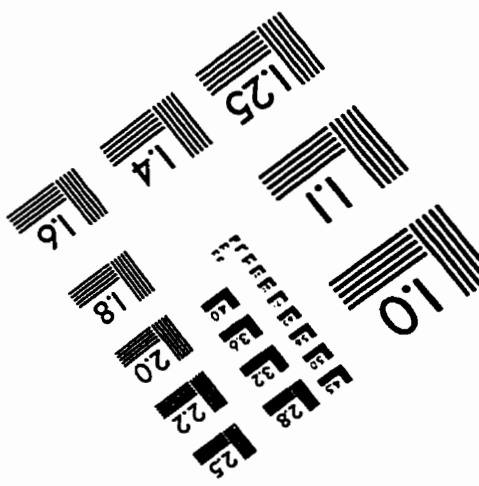

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