ANALYSIS OF MANUFACTURABILITY FACTORS FOR ANALOG CMOS ADC BUILDING BLOCKS

by
Rachelle Deanne Ockey
B.Sc. (Honours Physics), University of Victoria, 1996

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Abstract

Design for manufacturability (DFM) traditionally has been concerned with the design of robust digital circuits. Yet, as technology moves deeper into the submicron gate lengths, the design of robust analog circuits is becoming critically important. New sub-micron CMOS technologies are characterized for digital circuits only. Thus, the DFM of analog circuits in a sub-micron digital CMOS processes is becoming an increasingly complex task. DFM of analog circuits must include exploration into statistical CMOS processes variations and circuit layout design to ensure design robustness.

A class of analog circuits which have a multitude of uses in signal processing are analog-to-digital (ADC) converters. Due to their wide spread use and popularity, analog-to-digital converters are an excellent test vehicle to explore the DFM factors for analog circuits designed in a digital CMOS process. ADCs for high speed applications are the circuits of interest in this thesis. The ADC is a complex circuit with several building blocks, thus to investigate the manufacturability of an ADC, the manufacturability of the building blocks must first be examined.

This thesis investigates the dependence of the performance of ADC building blocks on statistical process variations and layout variations for a process characterized only for digital integrated circuits. The ADC building blocks chosen for this work were a latched comparator and a 4bit flash ADC. Three different layout styles were designed for the latched comparator and these different layouts were used to implement two different layouts of the flash ADC. The digital CMOS process used for fabrication of the different layouts was

0.35μm TSMC CMOS technology. In this work, the performance of the different layout styles for the comparator and flash ADC will be compared through both HSPICE simulation and bench-top measurements.

Acknowledgments

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Chapter 1

Introduction

1.1 Design for Manufacturability (DFM)

Traditionally, design for manufacturability(DFM) has only been considered for digital integrated circuits. The manufacturability of digital CMOS circuits is concerned with the statistical variation of a process that influences the ultimate yield of an ICs. The yield of interest is the catastrophic yield resulting from catastrophic faults, such as stuck-at-one or stuck-at-zero faults. Known methods have been established to investigate these faults and locate where in the circuit the fault has occurred [1]. Because the occurrence of catastrophic faults is strongly related to point defects, such as missing or extra spots of metal, the yield of a digital process can be described by the defect density and defect size distribution.

In contrast, there has been a lack of efficient investigation into the manufacturability considerations for analog circuits. Unlike digital circuits, under the statistical variations of a process, an analog circuit will experience performance faults. Several methods have been proposed to investigate these performance faults but these methods are either not efficient or not practical. To encompass the needs of analog CMOS circuits, the classical approach to design for manufacturability must consider new realities of the design process. DFM of analog circuits must include exploration of statistical CMOS processes variations and circuit layout design to ensure design robustness in sub-micron CMOS.

For a given sub-micron digital CMOS process, a foundry can guarantee a specific yield for

digital circuits, yet there is no assurance that an analog circuit will even function. For fabless design companies who rely on the lower cost of digital CMOS processes to manufacture analog circuits, it is important to investigate factors that influence the design for manufacturability of analog circuits.

In the past, statistical variations in the process have been the major concern for analog designers. However, as technology moves deeper into the submicron gate lengths, circuit layout is becoming an increasingly important factor that cannot be overlooked. As a result, proper layout design, a feature that has been of no importance for digital CMOS designs, may be one of the most important manufacturability criteria for CMOS analog blocks.

1.2 Analog-to-Digital Converters for DFM Study

A class of analog circuits that are integral in the increasingly important area of signal processing are analog-to-digital converters. Analog-to-digital converters (ADC) provide the interface between the analog signal domain and the binary digital computational domain. ADCs are extremely important for digital signal processing of physical signals such as temperature, pressure, sound and light. Therefore, the design for manufacturability of ADCs becomes critically important in deep sub-micron technology.

A wide range of ADC's exist today, each with varying degrees of resolution and speed which are targeted to meet a specific application. One such ADC is a pipelined ADC. The pipelined ADC is a medium resolution(8 - 14 bits), high speed ADC(>10MHz) that provides a high throughput rate and occupies a small die area. This converter has been extensively described in the literature [2-7].

Applications requiring the use of a pipelined ADC are always concerned with the yield and cost of such a device. As technology advances and MOS transistor dimensions shrink, it becomes more and more crucial for the design of the pipelined ADC's to be optimized for manufacturability. To optimize the design of pipelined ADCs, a designer must first consider and optimize the building blocks of the ADC. An important building block of a pipelined ADC is a low-resolution analog-to-digital subconverter (ADSC). This low resolution ADSC is connected in parallel with several identical ADSCs to produce a medium resolution pipelined ADC.

The ADSC is usually implemented as a high-speed flash analog-to-digital converter. The central component of the flash ADC is the comparator. To design a robust pipelined ADC, that will be insensitive to variations in the fabrication process, a designer must first identify the DFM factors important in the design of the comparator and flash ADC in submicron CMOS.

1.3 Research Focus

A comparator and a flash ADC are used as representative analog building blocks to explore several design for manufacturability factors for analog circuits. The optimization of the two analog blocks is conducted by investigating the effects of process-related parameter variations and layout-related design styles on the circuit performance. A comparators dependence on process and layout limits the manufacturability of high-speed flash ADC's in CMOS technology.

We believe that studying the effects of process variations and layout design styles on the DFM of analog CMOS blocks will facilitate the evaluation of design robustness. In addi-

tion, this research will assist in formulating principles for high-performance analog IC design in sub-micron digital CMOS processes. It is important to stress that this DFM approach is for analog ICs fabricated in a process that has been optimized for the design of digital ICs.

1.4 Research Methodology

Optimization for the design for manufacturability of a comparator and flash ADC was conducted in three areas: circuit architecture, CMOS technology factors (including CMOS process type and statistical process variations) and circuit layout. The first step in the DFM phase selected an architecture for both the comparator and the flash ADC. Next, the design optimization of both circuits was targeted for 0.35µm TSMC CMOS technology. The circuits were designed taking into account statistical process variations to ensure circuit robustness. After design of the transistor geometries, several circuit layout styles were created and implemented for the comparator and ADC. The layouts were evaluated on a simulation and measurement level. During HSPICE simulation, effects of statistical process variations were accounted for by using corner models. All layout styles generated for the comparator and ADC were fabricated in 0.35µm TSMC CMOS technology. After fabrication, the devices were tested and the simulation and testing results were compared leading to comparative analysis of the importance of technology-related versus layout-related DFM factors.

1.5 Organization of Thesis

This thesis presents and discusses the design for manufacturability criteria important in the design of analog building blocks for high speed analog-to-digital converters. Chapter 2

covers the features and limitations of a standard digital CMOS processes used for the design of the analog ADC building blocks. In addition, Chapter 2 discusses origin of process variations and how these variations are accounted for in the design of analog circuits. Chapter 3 is devoted to the layout of analog circuits. The layout design styles used in this research are covered in detail. Chapter 4 examines the comparator and flash ADC building blocks and presents insight into their integration into a high speed pipelined ADC. Chapter 5 provides comprehensive coverage on the transistor-level design of the comparator and flash ADC. Chapter 6 is devoted to the simulation and extraction of analog circuits for accurate performance data. Chapter 7 presents the measurement method for the fabricated circuits. Chapter 8 is devoted to presenting and analyzing the measured data and correlating the measured data and the simulation data. Finally, this thesis will conclude with a summary and remarks on directions for future work.

Chapter 2

Analysis of IC Manufacturability Factors

The first important design for manufacturability criteria is the technology used to create a circuit. A robust, optimized design not only matches circuit design style to the architecture and function to be implemented, but also to the CMOS technology in which the design is to be manufactured. The most favorable case would result in a process configured to target electrical parameters preferred by the specific design styles that will be used. Unfortunately, for each vendor there are differing process details and thus a variety of parameter spaces. To design a robust circuit, a designer must not only consider the types of CMOS technology but also account for the tolerance of the variation in process conditions. To help in with the design for manufacturability of analog circuits, statistical models that represent process variations can be employed to simulate circuit behaviour under unfavorable processing conditions. This chapter will discuss the type of digital CMOS process used for the building blocks design and the main process variations that contribute to performance variations of an analog design. In addition, statistical process models used to simulate process variations and layout considerations will be presented.

2.1 CMOS Process Used for DFM Study

New CMOS technologies with smaller geometries are emerging very rapidly. In this work, 0.35µm TSMC CMOS technology was used which is provided through the Canadian Microelectronic Corporation (CMC). The 0.35µm TSMC CMOS technology is a four metal layer and two polysilicon layer process with a minimum drawn gate length of 0.35µm. The 0.35µm technology is designed to operate from a power supply of

VDD=3.3V. This process is optimized for digital ICs. The digital parameters of importance, such as threshold voltage, are monitored and known, yet important analog design parameters, such as subthreshold currents, transconductances and transistor matching, are not specified. Therefore, the design of analog circuits becomes complex and thorough analysis and optimization of analog ICs is needed.

For the thesis work, several versions of comparators and flash ADCs were designed in 0.35μm technology. The circuit performance is dependent on a chosen technology and investigating circuit performance in a leading edge sub-micron process is an important area in design for manufacturability.

2.2 Process Variations

Fluctuations in a fabrication process that cause circuit performance variations can be grouped into two categories: front-end-of-line (FEOL) and back-end-of-line (BEOL) processing variations [8]. The FEOL variability affects the response of discrete electrical components such as transistors, resistors and capacitors. BEOL aspects of the process are concerned with the metal layers that are used to connect the electrical components together. Performance variations resulting from these two fabrication areas will be discussed in detail in the next two sections. It is important to stress again that this approach is for digital circuits.

2.2.1 Front-End-of-Line Process Variations (FEOL)

The performance of a transistor is strongly influenced by variations in its effective channel length(1), polysilicon gate length(2), spacer widths (3), gate oxide thickness(4) and device

width/edge effect variations(5). Figure 2.1 shows the relationship between each of these dimensional sources of variation and the basic transistor layout.

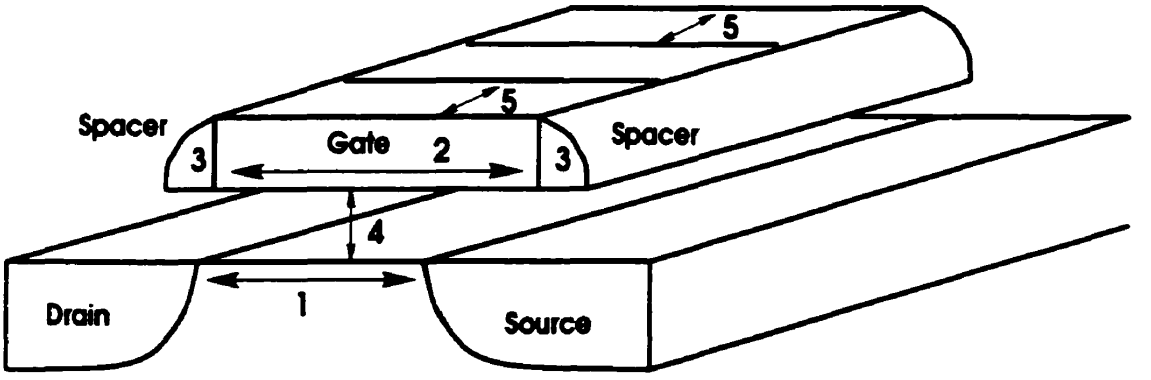

Figure 2.1: Sources of Variations for a Transistor Layout [8]

In most digital CMOS designs, the channel length is minimized since the device on-resistance and the gate capacitance are determined by the channel length. However, at these shorter channel lengths there arises a lower device threshold voltage and an increased dependence of the threshold voltage on drain voltage. These phenomena, labeled *short-channel effects*, result from a lower potential barrier between the source and drain due to the reduced distance between the source and drain [8]. Thus, shorter channels are more susceptible to threshold variations than larger channels, yet, a short channel length is required to achieve high speeds. Therefore, for analog applications requiring low threshold variability, longer transistor channel lengths are preferable. However, for high speed applications, a careful optimization must be completed to assure proper balance between high speed operation and threshold variability. This optimization must take into account all possible factors affecting circuit manufacturability, including statistical process variations and layout design style.

Physical processes that give rise to short channel effect are the size of the mask defining the gate, the angle of the etched polysilicon gate sidewall, the thickness of the spacer and the temperature at which the implants are activated. These subtle fabrication characteristics cause substantial changes in device characteristics. Therefore, the channel length has a 1st order influence on the performance of a transistor [8]. *Short-channel effects* can be reduced by ensuring that device gates are oriented in the same direction, are close to each other, have the same nearest neighbor distance and are placed in areas with similar overall pattern density [8].

Another concern in semiconductor processing is the variation between NMOS and PMOS gate lengths. This phenomena results from variation in the dose, energy and out-diffusion tolerances of the dopants associated with the n+ and p+ doping. This affect, called *NMOS to PMOS length tracking [8]*, must be added to the short channel effect to determine the total variation from NMOS to PMOS transistor. To reduce the affects of *NMOS to PMOS length tracking* a designer should ensure that the NMOS and PMOS transistors are in close proximity and relative NMOS and PMOS pattern/layout density, orientation and nesting are similar [8].

A second order process variation of note is *narrow channel width effects*. Channel width effects take a back seat to short channel effects, however, they are of concern for circuit topologies using minimum width devices. Devices with a minimum width experience higher threshold voltages than wider devices with the same length. In addition, the device can be treated as three devices in parallel where the two outer devices have different threshold voltages than the central device. Designers using small devices sizes for high

performance circuits should anticipate width dependence.

The FEOL variations discussed above are the only considerations for digital designs. However, there are several elements not mentioned that are unique to and are require for analog ICs. An important parameter for analog circuits is the matching of threshold voltage and I-V characteristics for a transistor pair such as a differential pair. Poor transistor matching degrades circuit performance drastically.

2.2.2 Back-End-of-Line Process Variations (BEOL)

Traditionally, BEOL variation was not a primary design concern, but due to scaled down device geometries and alternative high speed circuit topologies, variation in interconnect resistance and capacitance must be considered. The total on-chip wiring delay variation results from line width, line space and metal layer thickness.

Interconnect sheet resistance bounds the signal propagation speed by limiting the rate at which a capacitive load can be charged or discharged through a long wire. If the load of the wire is that of an active gate, the delay to charge the gate becomes key to the overall performance of the circuit. The sheet resistance is affected by variations in the metal layer thickness which can be controlled by keeping the interconnects in the proximity of field oxide. This can be accomplished by either defining a maximum wire width or by inserting oxide plugs in wide wires. The placement of the field oxide supports the polishing pad and helps prevent the dishing of the metal lines during CMP[1].

Metal interconnect width and space is an important parameter in resistance and capaci-

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1. Chemical Mechanical Polishing (CMP) is a technique which planarizes silicon dioxide insulator after the fabrication of each interconnect layer.

tance variation. Wider wires decrease connection resistance, but increase lateral line-to-line capacitance. Since wire width and space vary across a chip, the designer must consider the impact of variations in the resistance and capacitance. Wire width and space variations can be reduced by restricting the wire width and by maintaining a tight density range on all wiring levels.

The final BEOL variation of note is contact resistance. With the scaling down of technologies, the contact area must be scaled down by the square of the scaling factor yet the interlayer dielectric thickness is not scaled accordingly due to performance demands [8]. This results in a contact with large aspect ratios of etch depth-to-contact dimension, making contact and via formation more difficult. Several problems can arise during the building of contacts and vias such as non-ohmic connections, large contact resistances and etching residues in the contact hole. Each of these effects result in a poorly produce contact or via and therefore, it is a good design practice for designers to incorporate redundant contacts and vias in their designs to safeguard against high resistance or open connections.

Most of the BEOL variations will only affect large digital designs. Analog blocks are smaller and the resistance of the interconnect lines is of less importance in most designs, except those requiring a very large area and thus several interconnects. However, the resistance of contacts and vias is still an important factor for small analog circuits.

2.3 Simulation of Statistical Process Variations

Variations in the manufacturing process, such as small changes in the temperature of a diffusion furnace or the pressure in a reactive ion etch, inevitably lead to statistical variations

in the electrical behavior of devices. It is important to take these variations into account to ensure the ultimate manufacturability of a circuit. One methodology that has been developed to help simulate these variations in digital circuit design is worst case analysis [9].

Worst case analysis is the simplest and most commonly used technique to perform statistical circuit analysis [10]. A statistical model that has been developed to represent digital device operation is employed in the worst case statistical simulations. To determine the worst-case circuit performance, digital circuit simulations are performed at points in the parameter space which are called process corners. The process corners are defined as three standard deviations, $\pm 3\sigma$, above and below the mean values of a representative digital device characteristic. Usually, the drain saturation current at a given bias is chosen to be the representative characteristic because of it's relation to the propagation delay through a digital gate. Models are then generated for both NMOS and PMOS representing the $+3\sigma$ deviation and the -3σ deviation. The $+3\sigma$ deviation results in both NMOS and PMOS devices switching faster than in the normal case. Moreover, the -3σ deviation results in both NMOS and PMOS devices switching slower than in the normal case. Therefore, to simulate the extreme case-propagation delay of a digital gate, four circuit simulations are required, as listed in Table 2.1, in addition to simulation of the typical circuit behavior.

To create these corner models, MOS device parameters such as gate oxide thickness, etching effects of channel length and width, junction and sidewall capacitance and gate/source and gate/drain overlap, are varied to give $I_{dsat} = \pm 3\sigma$. Simulation of a digital circuit throughout all corners of a process will ensure a robust digital circuit operation.

Similarly, in the design of analog circuits, simulation at the corners of the digital process is

Table 2.1: List of Corner Models for a CMOS Process

Names of Corner Models
Typical - Typical (TT)
Fast - Fast (FF)
Fast - Slow (FS)
Slow - Fast (SF)
Slow - Slow (SS)

also used. However, the corner models are defined by digital circuits figures of merit and do not provide adequate information to accurately determine various analog parameters crucial for robust analog design. This is an area in need of exploration but is out of the scope of this thesis. For this thesis, we will rely on corner analysis as an accurate tool to model CMOS process variability. Therefore, these models can be used to obtain an indication of circuit and layout performances but it should keep in mind that the operation of an analog circuit might not be exactly as predicted by the corner models.

2.4 Layout as a DFM Factor

Traditionally, for analog designs employing geometries much larger, three to four times, than the minimum of a technology, process variations and not layout design has been the important concern. However, to exploit the high speed operation of a sub-micron digital CMOS process, it is desirable to create analog circuits with minimum dimension gate lengths. In this case, the layout of analog circuits may be equally or more important than process variability.

Chapter 3

Analog Layout Design Styles

An important DFM factor is minimization of parasitics through layout optimization. Careful planning of analog circuit layout must be conducted to realize high quality circuits. Several techniques can be used to reduce layout generated parasitic capacitances. Furthermore, these techniques can be implemented to reduce a circuits dependence on variations in a semiconductor fabrication process. Some of these techniques include transistors splitting, common centroid geometry, source and drain sharing, guard rings and complete source and drain contact coverage [11]. Three layout design styles are proposed which consist of combinations of the aforementioned layout techniques to investigate the dependence of circuit performance on layout. This chapter will cover analog layout techniques used to minimize layout generated capacitances/resistances. The chapter will conclude with a discussion and analysis of the layout design styles postulated in this thesis.

3.1 Analog Layout Techniques

CMOS analog circuit layout must be unique for each circuit designed because the performance of an analog circuit is degraded by parasitics. Additionally, a circuit is susceptible to performance variations caused by fabrication fluctuations. These degradations can be reduced by following several layout design guidelines. To illustrate the different layout techniques a simple analog building block, a differential pair with an active load, will be used. A schematic of the differential pair is shown in Figure 3.1. In this design, the gate lengths are approximately 3 times the minimum dimension of the process, which is standard in the majority of analog designs. The differential pair is widely used in analog cir-

cuits as an input stage. It is important to note, that while not depicted in the figure, the bulk

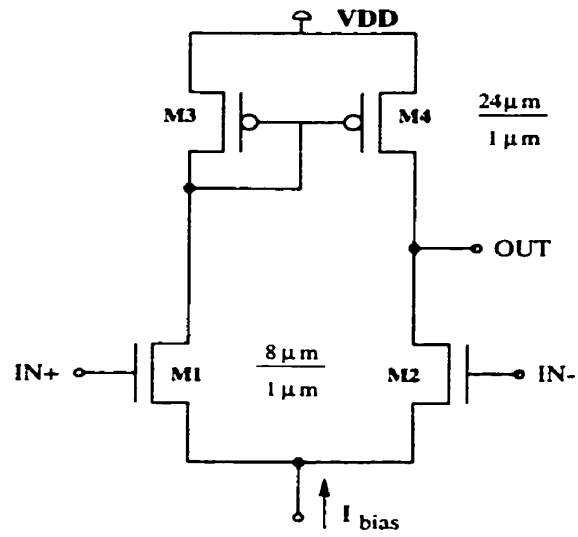


Figure 3.1: Analog Building Block: Differential Pair

nodes of all transistors are connected to the appropriate power supplies.

3.1.1 Transistor Splitting

One strategy that reduces the impact of parasitics on circuit performance is to require at least one split of a transistor channel into two as shown in Figure 3.2. This splitting of the transistor reduces the drain area by a factor of 2. The parasitic capacitance of the drain-to-substrate reversed biased p-n junction has a significant impact on the performance of the device. Therefore, reducing the area of the drain by a factor of 2 also reduces the parasitic capacitance at that particular drain node by 2.

Subsequent splitting of the transistor, by a factor of 2, further reduces the drain capacitance but only by a few more percent[11]. However, splitting a transistor into an odd number of portions, for example, three gate fingers, results in equal source and drain areas and therefore, no minimization of the drain area.

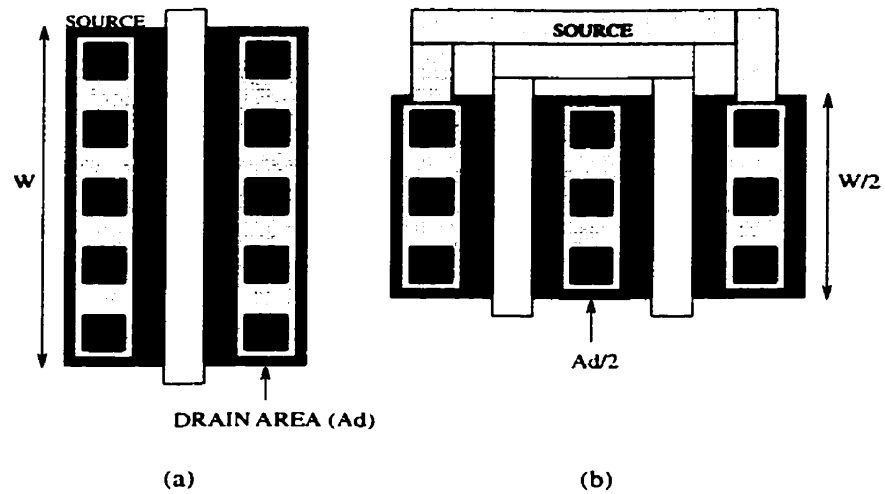


Figure 3.2: Example of transistor splitting. (a) transistor of width W, (b) split transistors of width W/2 [11]

3.1.2 Source/Drain Sharing

Another strategy to optimize circuit performance is to minimize the area of source and drains of MOS transistors by allowing separate devices to share the same diffusion region (source or drain). The main goal of the sharing is to reduce the diffusion parasitic capacitance. In addition, the source/drain sharing reduces of the total area of the cell.

3.1.3 Common Centroid Geometry

Another important aspect of analog design is transistor matching. Improper matching of two transistors that are critical to circuit operation, such the differential pair, M_1 and M_2, in Figure 3.1, will drastically affect the circuit performance. When precise matching between two transistors is required, the most accurate matching method is to split the transistors into the parallel connection of smaller transistors and then place the transistors in an alternating, or common-centroid geometry, as shown in Figure 3.3. Splitting transistors improves a device's immunity to mismatches caused by gradient type parameter variations

introduced by the fabrication process. The common-centroid geometry places the transistor components in close proximity reducing the process variation effects such as *short-channel effects* and *NMOS and PMOS length tracking.*

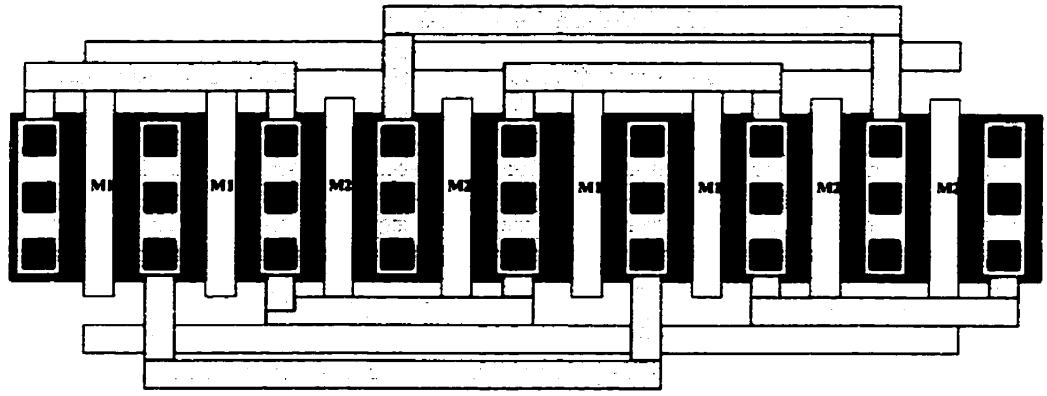


Figure 3.3: Example of the common-centroid geometry for transistors M1 and M2 of a differential pair [11]. This configuration also minimizes the area by utilizing source/drain sharing.

3.1.4 Full Stacked Technique

The full stacked technique involves choosing transistor aspect ratios to make the layout regular [12]. The size of a few critical transistors influence a circuits performance and for the remaining transistors, the size is not as critical. Therefore, it is possible to change, within limits, the size of these less-critical transistors to achieve a more regular layout for which design automation methods can be more easily applied. Changing the width of such transistors allows them to be stacked with other transistors. Stacking of the transistors reduces the parasitics due to source/drain sharing and makes it easier to achieve matching. The full stacked technique results in NMOS and PMOS transistor stacks with the same crystallographic orientation of gates, similar pattern and layout density and nesting. These characteristics contribute to a reduction in process variations, namely, *NMOS and PMOS length tracking* and *short-channel effects.*

3.1.5 Dummy Transistors

One final method to reduce mismatch in transistors is to match the boundary conditions at the ends of each transistor array. The etching of polysilicon is more aggressive in the free space around the pattern to be created than in the narrow spaces between neighbouring gates. As a result, the gates of edge transistors are overetched, as displayed in Figure 3.4a. This effect can be compensated for by using dummy transistors [11]. Dummy transistors are placed at both ends of a transistor array providing edge transistors with etching conditions identical to all of the interior transistors. Figure 3.4b depicts the benefits of dummy transistors. The dummy transistors are not used electrically and are purely for matching boundary conditions at the edges of transistor arrays. The gate of a dummy transistor is connected to the appropriate rail voltage, keeping the dummy transistor permanently off.

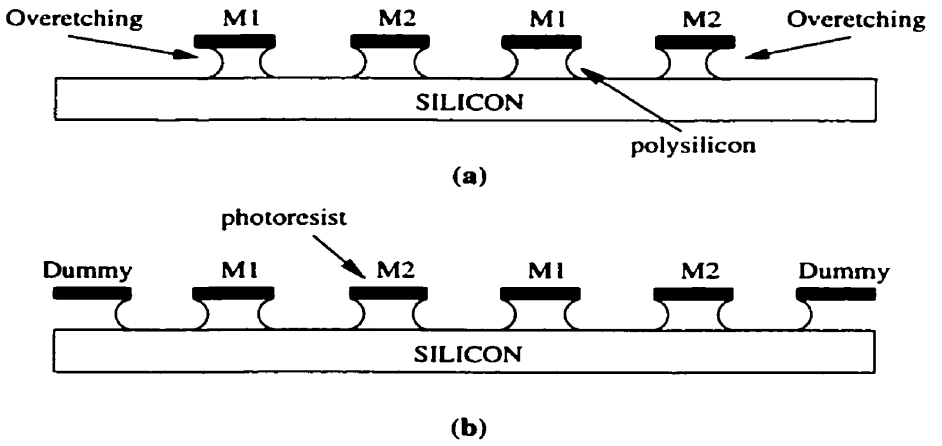


Figure 3.4: Cross-section through a common-centroid transistor pair. (a) effects of polysilicon overetching. (b) use of dummy gates to eliminate polysilicon overetching effects. [11]

3.1.6 Source/Drain Contacts and Guard Rings

Other important guidelines for analog layout are the placement of source/drain contacts and the connection of the bulk to the appropriate power supply. To ensure minimization of

source/drain resistances the maximum number of contacts allowable by the design rules of a process should be placed in the source and drain areas. Multiple contacts also ensure that effects of faulty contacts due to process variations are alleviated. In addition, *guard rings*, which are connections of the power rails to the appropriate bulk node, should be placed around NMOS and PMOS transistors. These guard rings protect the device from noise injection from other circuits on the chip. Figure 3.5 depicts the placement of guard rings,

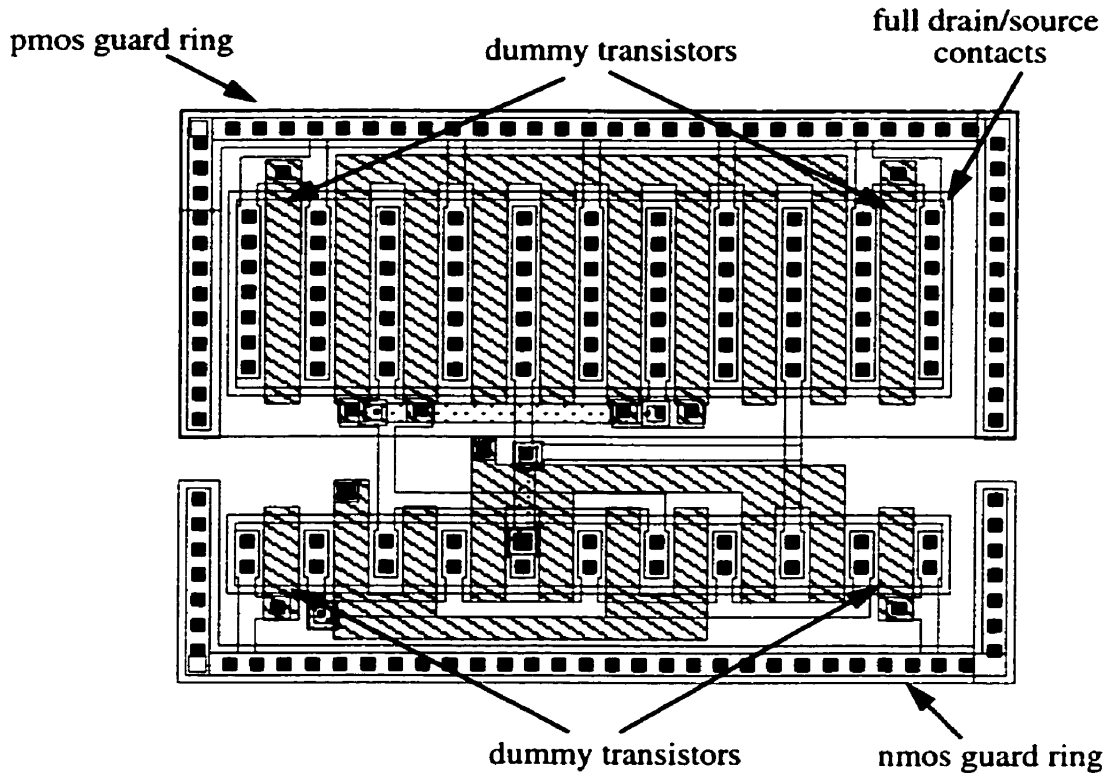


Figure 3.5: Layout of a CMOS differential pair demonstrating dummy transistors, full contact coverage, and nmos and pmos guard rings.

full source and drain contacts and dummy transistors on the layout of a CMOS differential pair with an active load.

3.2 Analog Layout Styles Proposed for DFM Study

Using various combinations of the above mentioned analog layout guidelines, three unique analog layout design styles were created. The layout styles were used to determine which factors are most important when designing for manufacturability. Analog circuit are susceptible to performance fluctuations due to process variations. The three layout design styles are discussed below.

3.2.1 Full-Analog Layout

The first proposed layout design style was the *full-analog layout style*. This layout style follows all of the guidelines discussed above. An example of a typical layout for the differential pair using the *full-analog layout style* is shown in Figure 3.6. In this example, tran-

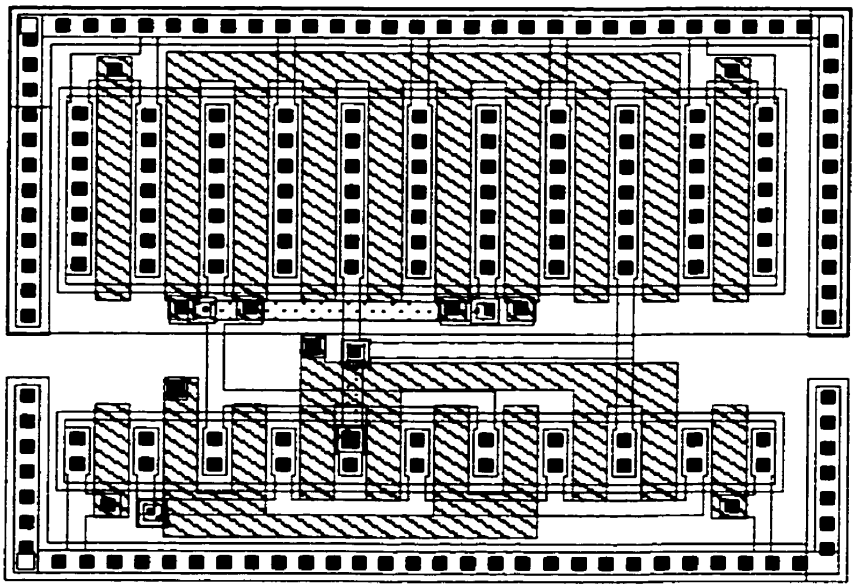


Figure 3.6: Example of the *full-analog layout style* for the differential pair.

sistors have been split and matched using the common-centroid geometry technique and the full stacked method. Dummy transistor can be found at the ends of the PMOS and

NMOS transistor stacks and there is a full coverage of source/drain contacts as well as VDD and VSS guard rings. This layout style will eliminate affects of process variations, such as *short channel effects* and *PMOS and NMOS length tracking*.

3.2.2 Partial-Analog Layout Style

The second layout style designed was the *partial-analog layout style*. This layout style ignores all of the guidelines presented above. There was no transistor splitting and no dummy transistors. This design style did include full drain/source contacts, guard rings and some source and drain sharing. The *partial-analog layout* of the differential pair is shown below in Figure 3.7. Due to a lack of transistor splitting and use of the full stacked

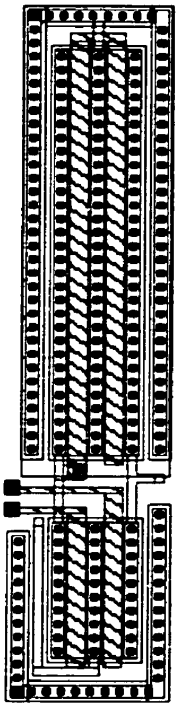


Figure 3.7: Example of the *partial-analog layout style* for the differential pair.

technique, this layout style will be more susceptible to transistor mismatch in the form of *short-channel effects* and *PMOS and NMOS length tracking* process variations.

3.2.3 Digital-Like Analog Layout Style

The *digital-like analog layout style* has been used to describe layouts for the analog circuits that have been designed using some digital layout concepts. The *digital-like analog style* included the use of transistor splitting and the common-centroid arrangement for transistor matching but neglected the use of dummy transistors, full guard rings and full contacts to the drains/sources of transistors. An example of this type of layout for the differential pair is shown in Figure 3.8.

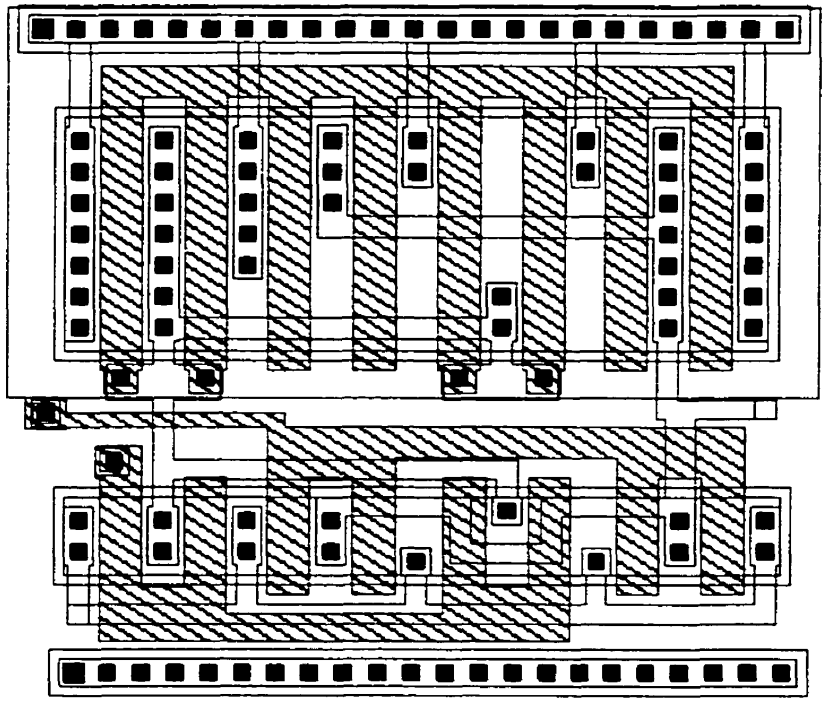


Figure 3.8: Example of *digital-like analog layout* style for a differential pair.

The *digital-like analog style* allows for a more compact design. Furthermore, this style facilitates easier routing of metal 1 lines and reduces the need for metal 2. The absence of dummy transistors will result in overetching of the edge transistors. However, a layout can be designed so that transistors not requiring matching are placed at the ends of each array.

Therefore, overetching effects should not affect the overall performance of the circuit. But, the reliance, in some cases, of only one or two contacts per source or drain region could lead to performance degradations if there are faulty contacts due to process disturbances.

3.3 Discussion of Layout Parasitics Versus Performance

Each of the three layouts previously mentioned for the differential pair were extracted to investigate the performance effects of the parasitic capacitances attributed to each layout. These parasitics are listed and compared in Figure 3.9. The majority of capacitors

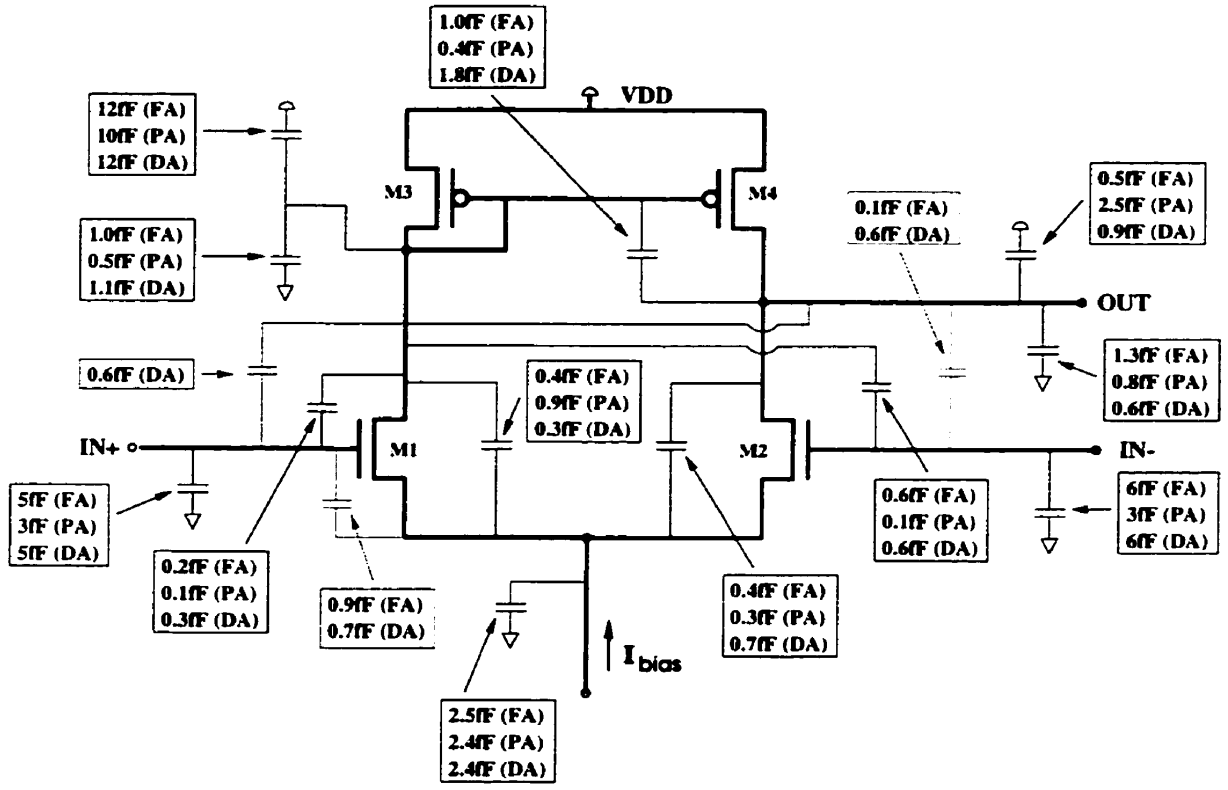


Figure 3.9: Parasitics generated from the three layout styles full-analog (FA), partial-analog (PS) and digital-like analog (DA).

extracted from the layout are common to each layout style however, there is a definite difference in the values of these capacitors, indicating that the layout style is of importance.

The variance in the capacitance values does not follow a trend from layout to layout and there are some capacitors that are only found in the *full-analog* and *digital-like analog* layouts. Thus to analyze the impacts of these parasitics on the circuit performance, a careful methodology was established. The effects of the parasitic capacitors on the circuit performance were evaluate through HSPICE simulations of the extracted layouts. Three methods of analysis were used to determine which parasitics, if any, had a strong influence on the operation of the differential pair amplifier.

The first method was to identify parasitic capacitors with a > 50% variation between layouts. Of these capacitors, one was chosen and a circuit netlist was constructed consisting of only the amplifier and the capacitor of interest. The capacitance of the selected capacitor was varied for several HSPICE simulations and the output characteristics of the differential amplifier were monitored. Results of varying the value of only one capacitor yielded no noticeable performance difference in the operation of the amplifier. Several other capacitors were used in turn and still no effect on the performance of the differential amplifier was observable. This suggests that considering changes in only one parasitic element is not sufficient enough to affect the operation of this test circuit.

The second method was to include all of the parasitic capacitors for one layout style and then vary the value of only one parasitic capacitor. This method also produce no noticeable difference in the output characteristics of the differential amplifier.

The third method was to determine if the results in the first method used was valid not only for the typical model but also for all corner models. Possibly, the parasitics capacitors only affect circuit performance under non-ideal device formation. For the differential pair, no

performance degradation was observed by fluctuating the parasitic capacitances and evaluating the performance for the different corner models.

Thus, for a differential pair designed with gate lengths ~3 times larger than the minimum dimension, parasitic capacitors have no effect on the simulated performance. This indicates, that for an analog circuit with a large L, the layout style does not have a large effect on the simulated circuit performance.

3.4 Parasitics Not Accounted for by Circuit Extractor

There are parasitics that result from process features which are not considered by the extractor tool. Some examples of these parasitics are the overetching of MOSFET gates located at the end of a stack and the gradient type non-uniformities of process parameters. These parasitics can only be modeled by a deliberate adjustment of the MOSFET dimensions or model parameters. Since most of these effects can be minimized by using the full-analog layout style, it is expected that these effects will be most noticeable in the other two layout styles. The extent of these parasitics on the performance will depend on the process features. This issue will not be explored further here due to lack of process feature data which are not included in digital CMOS process specifications.

Chapter 4

ADC Building Blocks for Manufacturability Study

In this chapter, the ADC building blocks, the comparator and flash ADC, used in this manufacturability study will be discussed in detail. The pipelined ADC will be covered briefly.

4.1 Pipelined Analog-to-Digital Converter Operation

The concept of pipelining, often used in digital circuits, can also be applied in the analog domain to achieve higher speeds where several operations are performed serially. Figure 4.1 shows a block diagram of a general pipelined analog-to-digital converter.

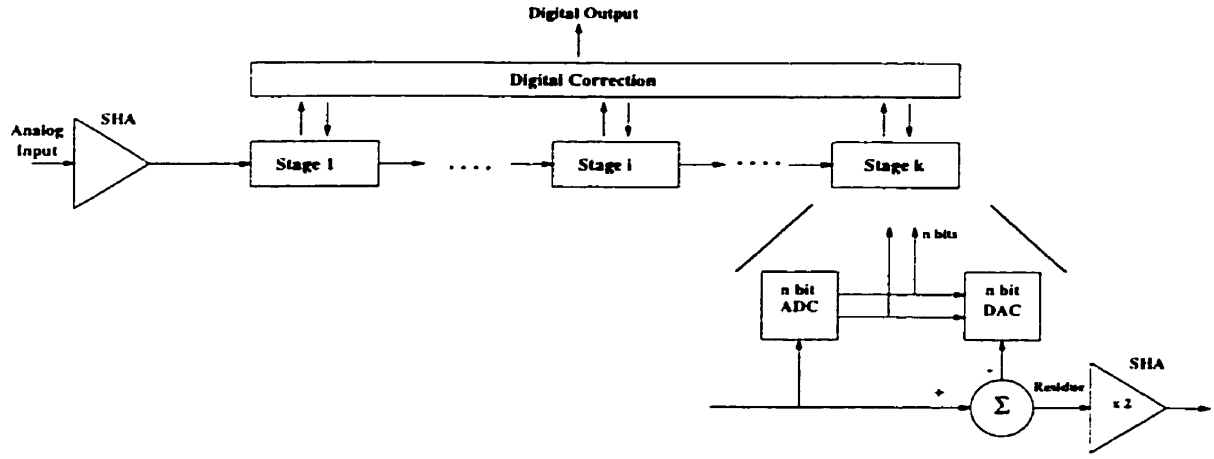


Figure 4.1: Generalized block diagram of a pipelined A/D.

The architecture consists of N stages, each including a sample and hold amplifier (SHA), an ADC, a digital-to-analog converter (DAC), a subtractor and an amplifier. A full description of the conversion process can be found in [13], therefore only a brief discussion will be given here. In operation, each stage initially samples and holds the output from the pre-

vious stage. Each stage then does a low-resolution ADC conversion on the held input, and the code produced is converted back into an analog signal by a DAC. Finally, the DAC output is subtracted from the held input, producing a residue that is amplified and sent to the next stage. Because each stage incorporates a sample-and-hold function, the analog data is preserved, allowing different stages to process different samples concurrently. Thus, the conversion rate depends on the speed of only one stage.

The number of bits resolved in each stage and hence the number of stages of a pipelined ADC depend on various considerations such as overall resolution, speed and technology. Practical implementations vary from multi-bit flash stages[2-4] to 1-bit-per-stage topologies[5-7], each of which has its own merits and drawbacks. For low resolution pipelines it is common to use a 1.5 bit per-stage resolution to reduce the loading on the op-amp. However, for higher resolution pipelines, 12 bits and larger, the optimum per-stage resolution increases to 2-4 bits which decreases power consumption.

For this research, a per-stage resolution of 4 bits was chosen. The 4 bit sub-converter was implemented using a flash ADC. The benefit of using a flash-subconverter is that the pipeline architecture only needs two main clock phases per conversion; therefore, the maximum throughput rate can be high. Also, since the stages operate concurrently, the number of stages used to obtain a given resolution is not constrained by the required throughput rate.

4.2 Flash ADC Building Block

4.2.1 Flash Converter Operation

Conceptually the simplest and potentially the fastest, flash architectures employ parallelism and "distributed" sampling to achieve a high conversion speed. The circuit, shown in Figure 4.2, is a block diagram of a 4bit flash subconverter which consists of a resistor ladder, comparators and encoding logic. The resistor ladder subdivides the main reference, V_{ref}, into 2^4-1=15 equally spaced voltages, and then the 15 internal comparators must amplify the small voltage differences into logic levels. The reference voltage at any comparator can be stated as [13]:

$$V_{ri} = (i / 2^n) * V_{ref} \qquad (4.1)$$

where n = number of bits
i = comparator number

Any comparator connected to a resistor string node where V_{ri} is larger than V_{in} will have a 0 output while those connected to nodes with V_{ri} less than V_{in} will have 1 outputs. The output from the 15 comparators is commonly referred to as a thermometer code since it looks quite similar to the mercury bar in a thermometer. At this point, logic is enabled to encode the thermometer code outputs of the comparators into a 4 bit binary word. Most flash converters utilize voltage comparison, rather than current comparison, because distribution of a voltage to a large number of comparators is easier [14].

Depending on the algorithm used, the encoding process can often be pipelined with the comparator function. Since the encoding process is faster than the comparator function, the maximum conversion rate for the flash converter is limited by the response times of its

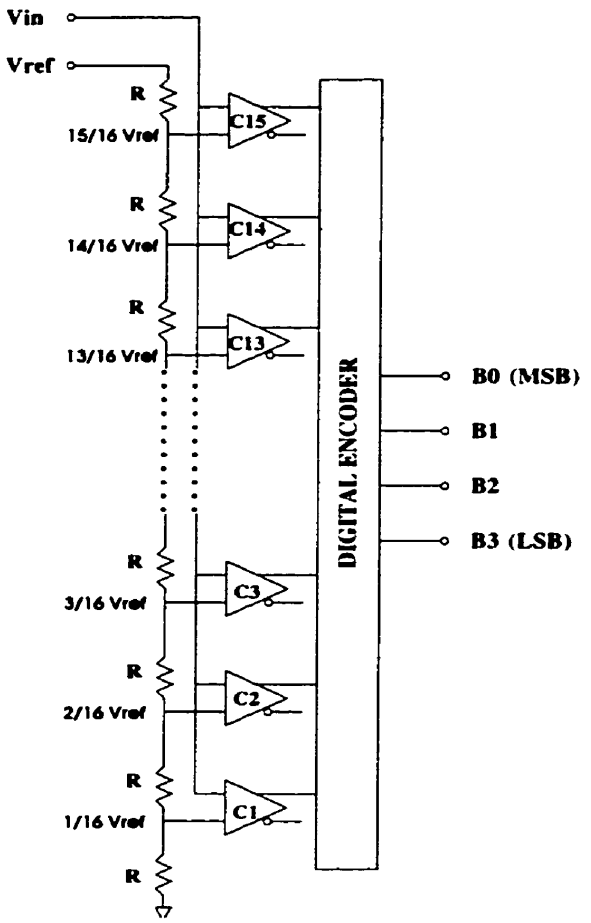


Figure 4.2: 4bit flash sub-converter for pipelined ADC [16].

comparator. Therefore, the design and optimization of the comparator is critically important [15].

4.2.2 Important Flash ADC Performance Metrics

An ADC produces a digital output, D, that is a function of an analog input, A. Since the

$$D = f(A) \tag{4.2}$$

input of an ADC can have a continuous range of input amplitude levels and the output has only a finite set of digital words, the ADC must approximate each input level. To charac-

terize an ADC's operation a transfer function, as shown in Figure 4.3, is created. For sim-

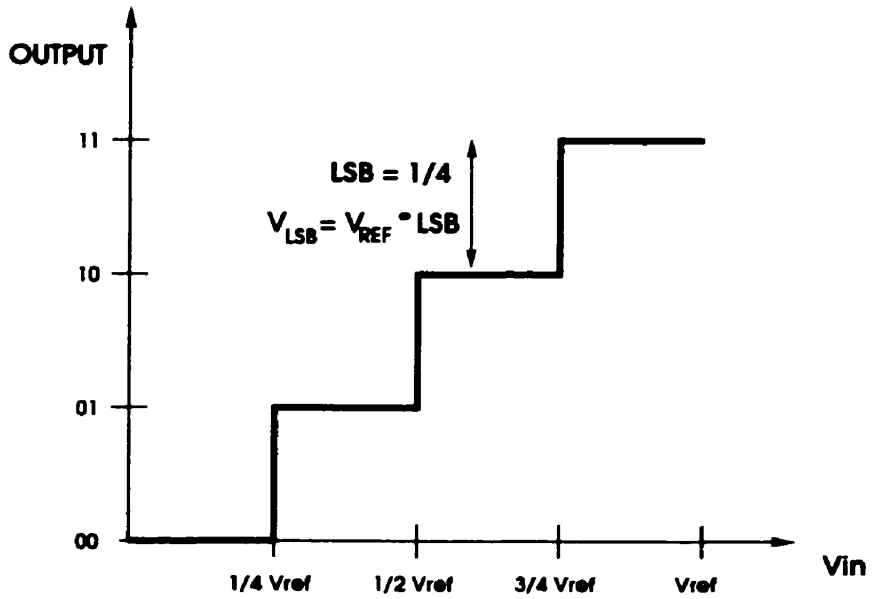


Figure 4.3: Ideal output of a 2-bit ADC.

plicity, this figure shows the ideal output of a 2bit ADC, instead of the 4bit ADC of interest, to illustrate the characteristics of an ADC. For an ideal transfer function, the output word should increase by one bit, a least significant bit (LSB), when the input increases by the value of one LSB. The voltage of the LSB is given by [16]:

$$V_{LSB} = V_{ref} * LSB \tag{4.3}$$

where

$$LSB = 1/2^n, \; n = \text{number of bits}$$

In reality, the transfer function of an ADC can deviate from the ideal due to imperfections in the fabrication of the circuit.

There are several performance metrics that describe the performance of an ADC, for a complete list refer to [17] [18] [19]. However, only a few of these performance measures

need to compare the performance of different ADC designs. To illustrate these characteristics of interest, Figure 4.4 depicts a comparison between an ideal ADC transfer curve and that of an imperfect ADC. These four characteristics are the most common characteristics

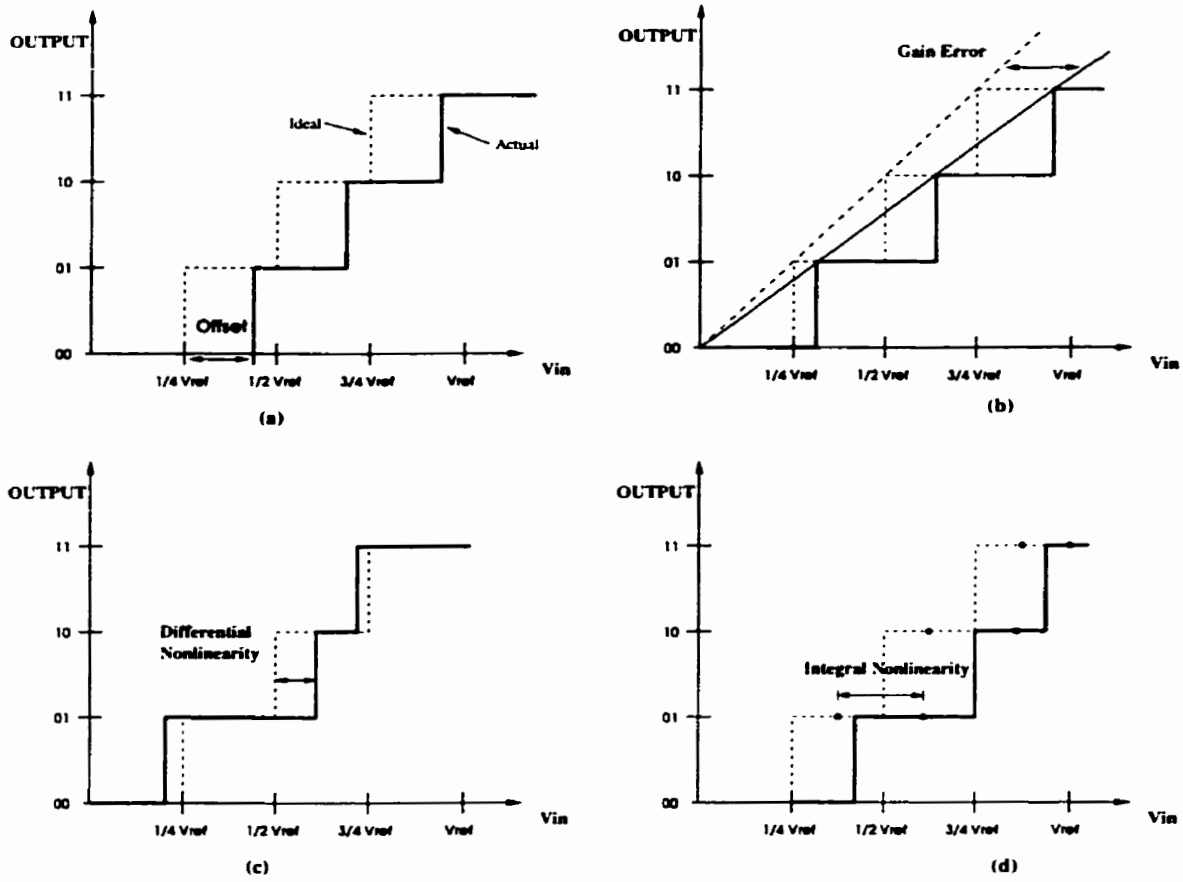


Figure 4.4: Graphical presentation of the performance metrics for an ADC. (a) offset error, (b) gain error, (c) differential non-linearity, (d) integral non-linearity. The dotted line is the ideal transfer function of a ADC and the solid line represent measured, non-ideal data for an ADC.

used to describe the behavior and a data converter. These figures of merits are described below:

- *Offset* is deviation from the ideal location of the lowest transition level on the ADC transfer function.

- *Gain Error* can be specified as the deviation from the ideal location of the highest transition level on the ADC transfer function. The gain error is found after the offset is removed and is given by the equation [19]:

$$\text{Gain Error} = V_f - V_{ideal} \qquad (4.4)$$

where

V_f = highest transition level voltage
$V_{ideal} = V_{ref}$ - 1.5 LSB - offset error

- *Differential Nonlinearity (DNL)* is the maximum variation in analog step size between two consecutive code transition points on the input axis from the ideal value of 1 LSB. An ideal ADC has a DNL of 0 whereas a converter with a maximum DNL of 0.5LSB has its step size varying from 0.5LSB to 1.5LSB. In this work, the DNL will be computed as the maximum magnitude of the DNL values.

- *Integral Nonlinearity (INL)* is the deviation of code midpoints from their ideal locations. As in the DNL case, the INL will be calculated as the maximum magnitude of the INL values.

The last converter performance metric of interest is the *ADC Conversion Time*. The conversion time is measured as the time taken for the converter to complete a single measurement.

Each of these converter characteristics will be influenced by process variations. Measurement of these parameters for several devices can determine which designs are more suitable for a given technology.

4.3 Comparator for Flash Sub-Converter

In high speed flash analog-to-digital converters, comparator design has a crucial influence

on the overall performance that can be achieved. Converter architectures that incorporate a large number of comparators in parallel, such as the flash converter, to obtain a high throughput rate impose stringent constraints on the delay, resolution and input voltage range of those comparators. Moreover, the relatively large device mismatch and limited voltage range that accompany the integration of comparator circuits in low-voltage scaled VLSI technologies severely compromises the precision that can be obtained [20]. However, in the pipeline architecture, the error from a large comparator offset in the flash ADC section of each pipeline stage can be easily compensated with digital correction.

A comparator architecture that lends itself well to the constraints imposed by the flash ADC is a latched comparator. A latched comparator consists of a preamplifier and a cross-coupled latch that has two modes of operation: tracking and latching. In the tracking mode, the latch is disabled and the preamplifier is enabled to amplify the input difference and track the input. In the latching mode, the preamplifier is disabled and the latch is enabled so that the instantaneous output of the preamplifier is repeatedly amplified and logic levels are produced at the output. The track-and-latch stage minimizes the total number of gain stages required, even when good resolution is required, and, therefore, is faster than a multi-stage comparator. In typical dynamic cross-coupled latches, process variations and mismatches can result in large offset voltage which can easily fall within the tolerance of digital error correction.

Latched comparators, implemented in the voltage and current domains, are widely used in analog-to-digital converters and as sense amplifiers for DRAMS. Because of their popularity, numerous latched comparator designs can be found in the literature [2-7]. Due to

the broad range of latched comparator designs, further redesign was not attempted. Instead, an architecture was chosen from the literature and various transistor geometries and layout designs were developed. The architecture of the latched comparator was a folded cascode design with a dynamic latch as the load [6]. This particular comparator was chosen for its simplicity, use of n-channel transistors in the signal path and its high speed operation.

4.3.1 Latched Comparator Circuit

Figure 4.5 shows the schematic of the latched comparator [6] building block used in the flash ADC. The latched comparator consist of a folded cascode differential amplifier (M_1-M_7) in which the load is replaced by a dynamic latch (M_8-M_{10}). The circuit operates as follows: when M_{10} is on, the comparator outputs, the voltage signals at the drains of M_4 and M_5, are shorted together and connected to the gates of M_8 and M_9. In this configuration, the differential current flowing from the cascodes flows through M_{10} equalizing the voltages at the drains of M_4 and M_5. When M_{10} turns off, the comparator outputs are separated, leaving M_8 and M_9 connected in a positive-feedback configuration. As a result, differential current coming from the cascodes charges the output-node parasitics and the output is latched; that is, one output is pulled up to the positive supply and the other pulled down toward ground. Transistors M_{11}-M_{14} provide the bias voltages for the gates of M_3-M_7.

4.3.2 Latched Comparator Performance Metrics

The following parameters are commonly used as figures of merit for comparator circuits [13].

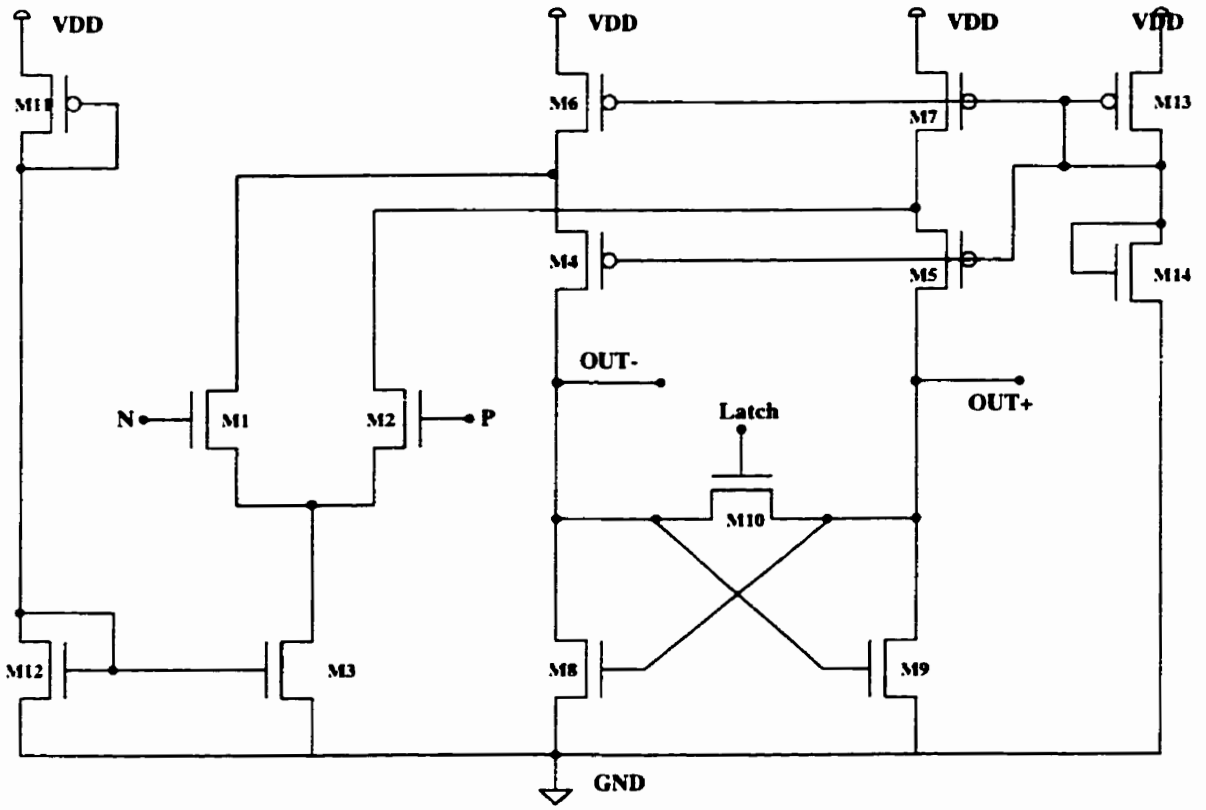


Figure 4.5: Latched comparator schematic [6].

- *Resolution* is the minimum difference between the input voltage and the reference voltage that yields a correct digital voltage output.

- *Comparison rate* is the maximum clock frequency at which the comparator produces an output. This rate is limited by the recovery time of the preamplifier as well as the regeneration time constant of the latch.

- *Dynamic range* is the ratio of the maximum input swing to the minimum resolvable input.

A diagram depicting the timing of the latch and output signals is shown in Figure 4.6. For an input signal larger than the reference signal, the positive output of the comparator goes high and the negative output of the comparator goes low when the latch is low. However, when the latch is switched to high, the positive and negative outputs drops to 1/2 VDD as

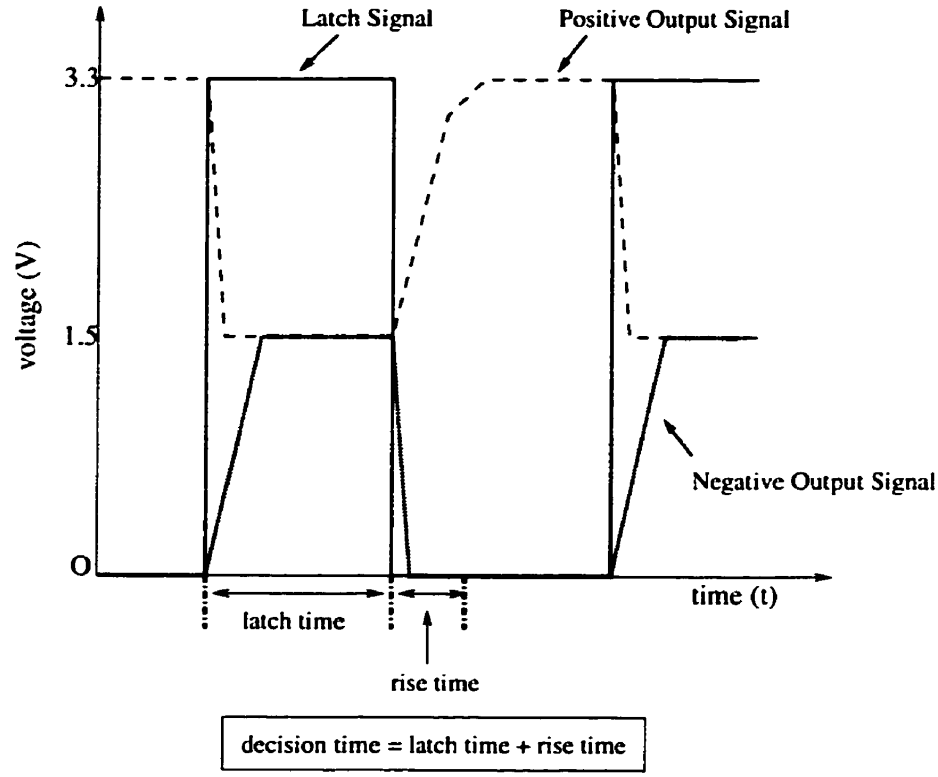


Figure 4.6: Typical comparator output.

the differential current flowing through the latch is equalized.

Chapter 5

Design of ADC Building Blocks

The design of the comparator and flash ADC building blocks is critically important to the operation of a pipelined ADC. This chapter discusses the important issues involved in optimizing the design of both the comparator and the flash ADC.

5.1 Design Considerations for the Latched Comparator

Several factors must be considered in the design of the latched comparator. After having chosen an appropriate architecture for the comparator, the remaining tasks include designing the transistor dimensions, special considerations for transistor matching and comparator layout design.

5.1.1 Transistor Matching

For the design of the latched comparator, it is important to match the dimensions of transistors M_1 and M_2 as well as M_6 and M_7, refer to Figure 4.5. For perfect operation the current through M_3 should be split evenly between M_1 and M_2. Application of a positive voltage difference between inputs N and P, should result in a decrease in the current through M_2 and an identical increase in the current through M_1. Any mismatches in a transistor pair will cause and imbalance in current division resulting in a decrease in comparator resolution. In addition, the current must also be split evenly between M_6 and M_7. These two transistors provide current for the cascode stage. Therefore, both pairs of transistors must be designed with exceptional matching properties otherwise the resolution and

dynamic range will suffer.

To match two transistors, the transistors must have the same gate length and width. Secondly, to ensure good matching, the transistors should be placed in close proximity to each other to reduce effects originating from gradient-related process variations. Ideally, matched transistors should be configured in a common-centroid geometry as discussed in Section 3.1.3.

5.1.2 Transistor Design

The comparator was design in 0.35μm TSMC digital CMOS technology. All transistors were designed with the minimum gate length dimension of L=0.35μm and operate from a single 3.3 volt power supply. Use of a minimum dimension gate length will facilitate a high speed device operation but will open the device up to *short-channel* effects (Section 2.2.1). One of the goals of this thesis is to push analog designs to the limits of the digital technology to exploit the advantages of high speed operation.

The transistor channel widths for the comparator were designed with the aid of HSPICE. In the initial phase of design, the channel widths were set to be wide. The performance of the circuit was simulated with HSPICE and the channel widths were adjusted to improve the performance of the comparator. Channel widths that resulted in a high resolution and high speed performance were used for the final fabricated devices and are shown in Figure 5.1.

The widths of the transistors were chosen to be at least 3 times the minimum dimension to eliminate the possibility of *narrow channel width* effects (Section 2.2.1). In addition, the

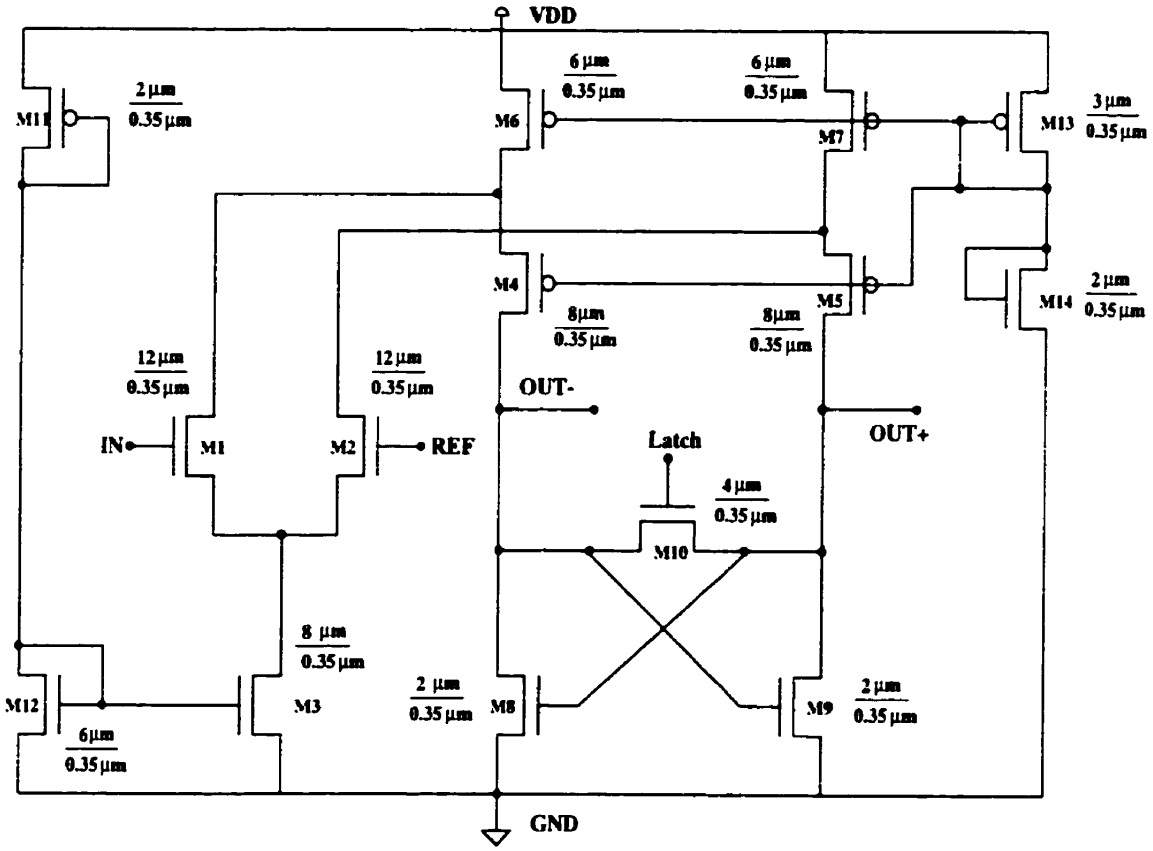


Figure 5.1: Schematic diagram of latched comparator.

transistor dimensions were designed such that a full stacked technique could be used. The full stacked technique involves choosing transistor aspect ratios to make the layout more convenient for splitting. For the comparator, the size of a few critical transistors, namely, M_1, M_2, M_6, M_7, M_{10}, influence the comparator performance. For the remaining transistors, the size is not as critical. Therefore, it is possible to change, within limits, the size of these less-critical transistors to achieve good layout. Changing the width of such transistors allows them to be stacked with other transistors in the comparator. Stacking of the transistors reduces the parasitics and makes it easier to achieve matching.

5.1.3 Latched Comparator Layout Design

The next step in the design of the comparator was to design the layout of the circuit. Three different layout design styles were used for the latched comparator in 0.35μm CMOS. The similarities between these layouts include matching of transistors M_1, M_2 and M_6, M_7, the same crystallographic orientations of each channel and VDD and VSS guard rings.

The first layout style, the *full-analog* layout, is shown in Figure 5.2. This layout features

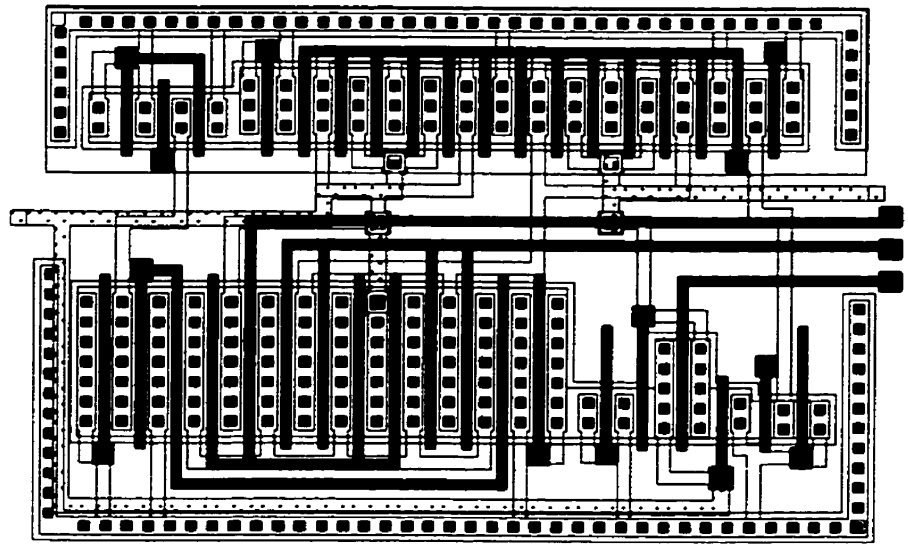


Figure 5.2: *Full-analog* layout of latched comparator.

common-centroid geometry, dummy transistors, source/drain sharing and full contacts to source and drain regions. The area occupied by the *full-analog* layout is 20.9μm x 31.4μm or 656μm^2.

The second layout, the *partial-analog* layout, is displayed below in Figure 5.3. This layout has no transistor splitting and no dummy transistors and there is minimal source/drain region sharing. The area occupied by this layout is 46.6μm x 17.8μm or 830μm^2.

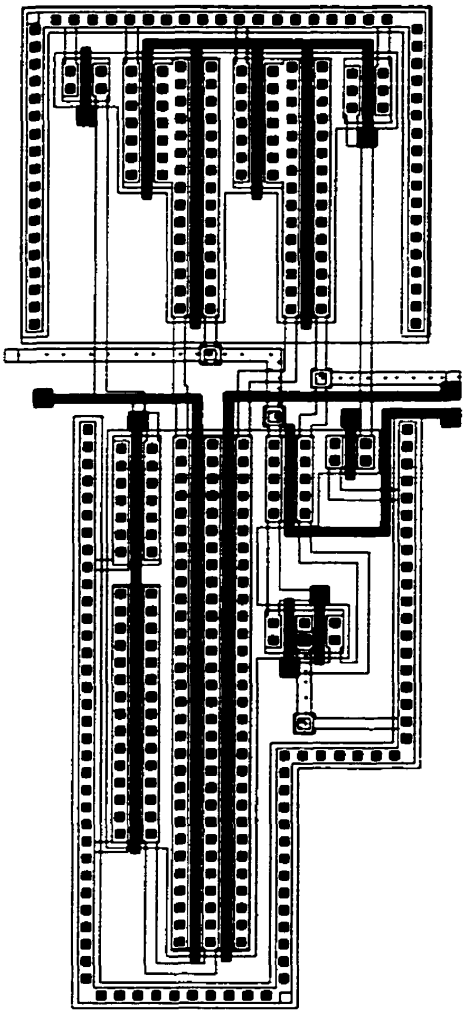


Figure 5.3: *Partial-analog* layout of latched comparator.

The final layout, the *digital-like analog* layout, included the use of transistor splitting and the common-centroid arrangement for transistor matching but neglected the use of dummy transistors, full guard rings and full contacts to the drains/sources of transistors. The layout for the latched comparator can be viewed in Figure 5.4. The area occupied by the *digital-like analog* layout is 22.8μm x 18.4μm or 420μm^2.

The *digital-like analog* layout occupies the smallest silicon area due to the lack of full

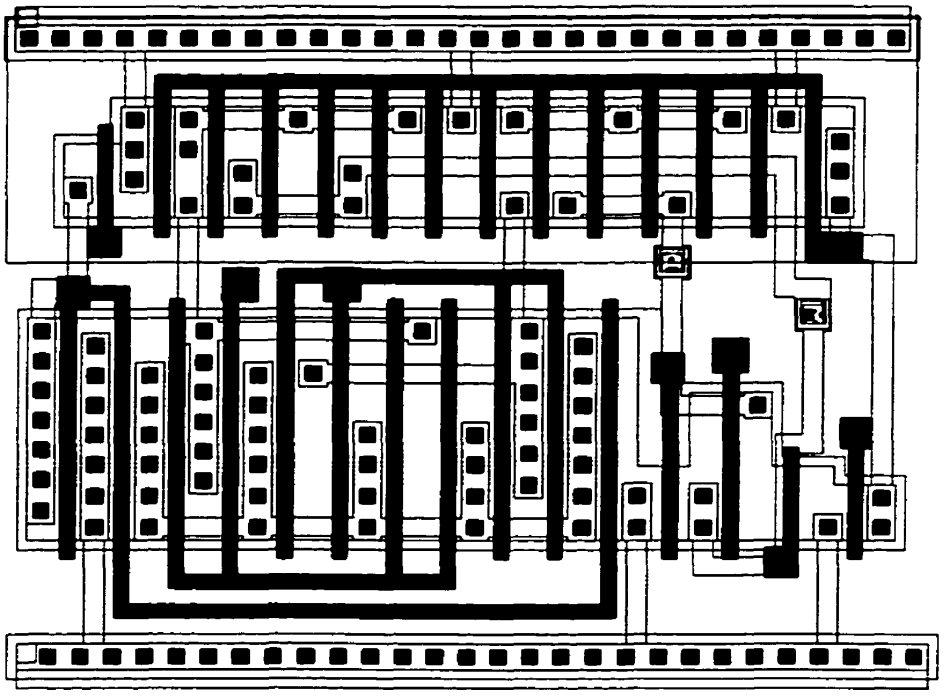


Figure 5.4: *Digital-like analog* layout style of latched comparator.

guard rings, dummy transistors and less complex metal interconnects. The next largest in silicon area coverage is the *full-analog* layout followed by the *partial-analog* layout.

Since the *full-analog* layout follows all of the recommended design guidelines, it should be less susceptible to process variations. In contrast, the *partial-analog* and *digital-like analog* layouts neglect some of the layout guidelines and thus, should experience some performance fluctuations.

5.2 Design Considerations for the Flash ADC

The flash ADC, shown in Figure 4.2, consists of three main sections, the resistor string, comparator bank and the encoding logic. Each of these sections were designed separately and then placed together to create the overall flash ADC.

5.2.1 Resistor String Design

The resistor string for the 4 bit flash ADC consists of 16 resistors as shown in Figure 5.5. The resistors are of equal value, R, and subdivide V_{REF} into 15 equally space reference voltages. For the resistor string to produce 15 equally spaced voltages, the resistors must be matched extremely well.

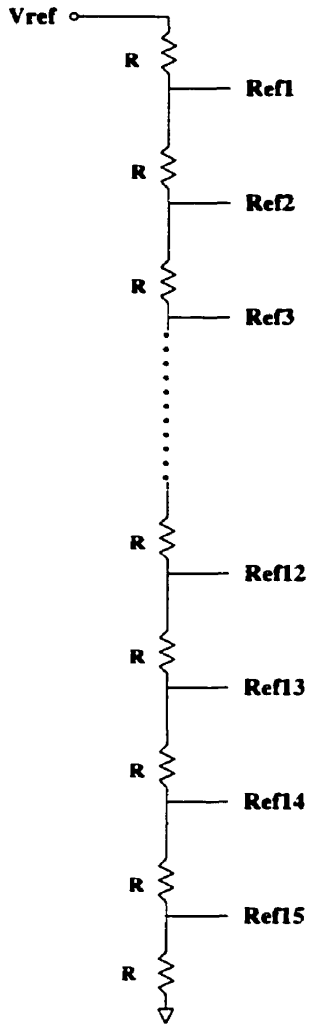


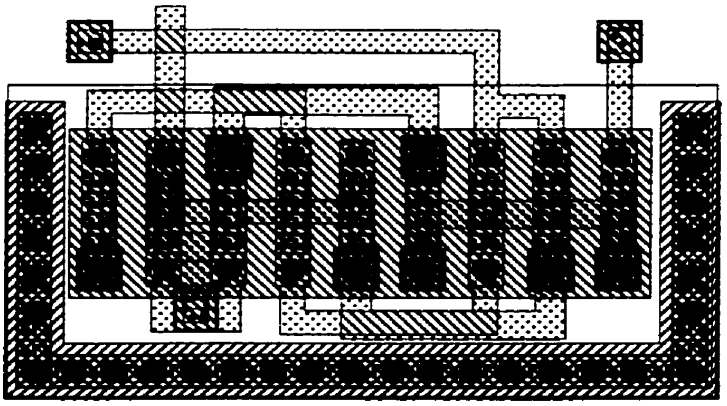
Figure 5.5: Schematic of resistor string for flash ADC.

An integrated resistor can be fabricated by using one of several highly resistive layers available in CMOS technologies. The choice of layers is either p^+, n^+, or nwell diffusion

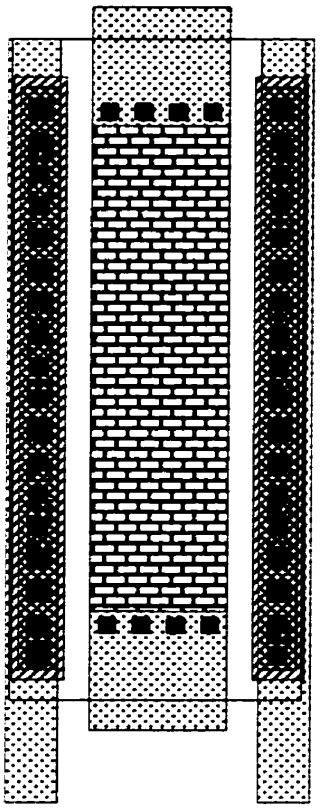
and polysilicon. All of these layers have a specific sheet resistance, R_S, which defines the resistance for a square of the layer. In wells, the sheet resistance is on the order of kΩ/ square, whereas for highly doped diffusion or polysilicon it is typically tens of Ω/square. The absolute accuracy of integrated resistors is less than 30% yet the mismatch between resistors can be as low as 0.1% with careful design [11]. The typical structure of an integrated resistor consists of a resistive layer connected at either end by metal ohmic contacts. For good matching, an interdigitated arrangement, is commonly used. The interdigitated configuration places portions of the devices to be matched in an interdigitated fashion helps reduce the main source of mismatch, process gradients.

Resistor strings designed for the flash ADC were of both types: rectangular and interdigitated. Since the main goal for the design of the resistors is not the absolute resistance value but the matching between the resistors, both types of resistor layout were designed to explore the performance effects on the flash ADC. In both cases, p^+ diffusion was used to create the resistors. Examples of both resistors are shown in Figure 5.6.

The interdigitated resistor consisted of three resistors inter-twined together. Three resistors was the maximum number that could be interdigitated in one unit. Interdigitation of more than three resistors created several problems with the placement of the interconnect metals. Each group of three interdigitated resistors were placed in close proximity to the other resistors to improve the matching. All of the interdigitated resistors were connected in series in accordance with Figure 5.5.



(a)



(b)

Figure 5.6: P^+ Diffusion resistor layouts, (a) three interdigitated resistors, (b) rectangular resistor.

5.2.2 Floorplan for Comparator Blocks in Flash ADC

To build a 4-bit flash ADC, 15 latched comparators were required. There are several ways in which the comparator blocks could be placed on the chip. Two configurations of comparators were created in this research. The first layout consisted of the comparators being placed one below the other. This placement respects the symmetry of the flash circuit that was displayed in Figure 4.2. One drawback of this configuration is the large silicon area that is required. A more compact alternative was also designed that used the digital-like analog layout of the comparator. The comparators are arranged in five rows of three comparators. A block diagram, displayed in Figure 5.7, shows the relative placement of the

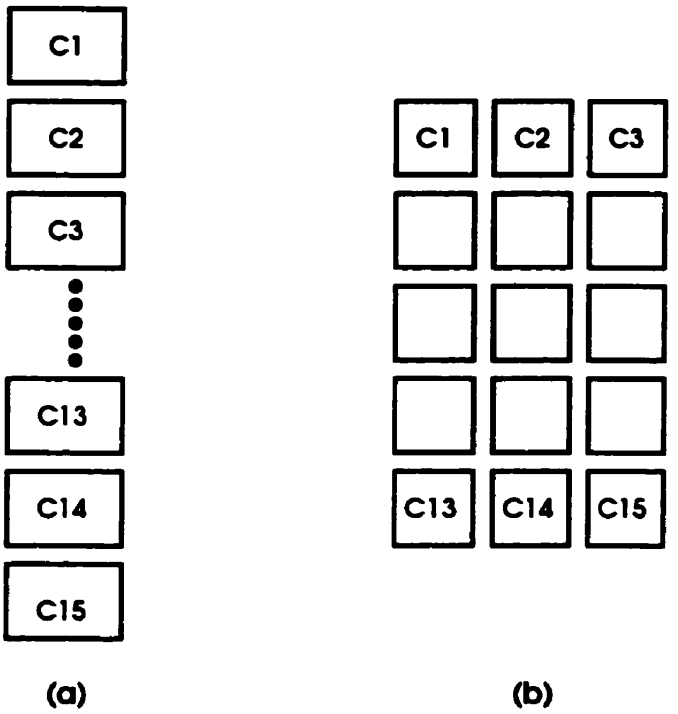


Figure 5.7: Placement of comparators for flash ADC.

comparators in each of the configurations.

5.2.3 Design of the 4-Bit Encoding Block

The encoding block is used to convert the output thermometer code of the 15 comparators into a 4-bit output word. If the outputs of the 15 comparators are labeled A through O, the logic equations for the conversion are as follows in Figure 5.8. The logic equations were implemented with multiple input AND and OR gates and inverters. The logic gates were custom designed using minimum dimension geometries.

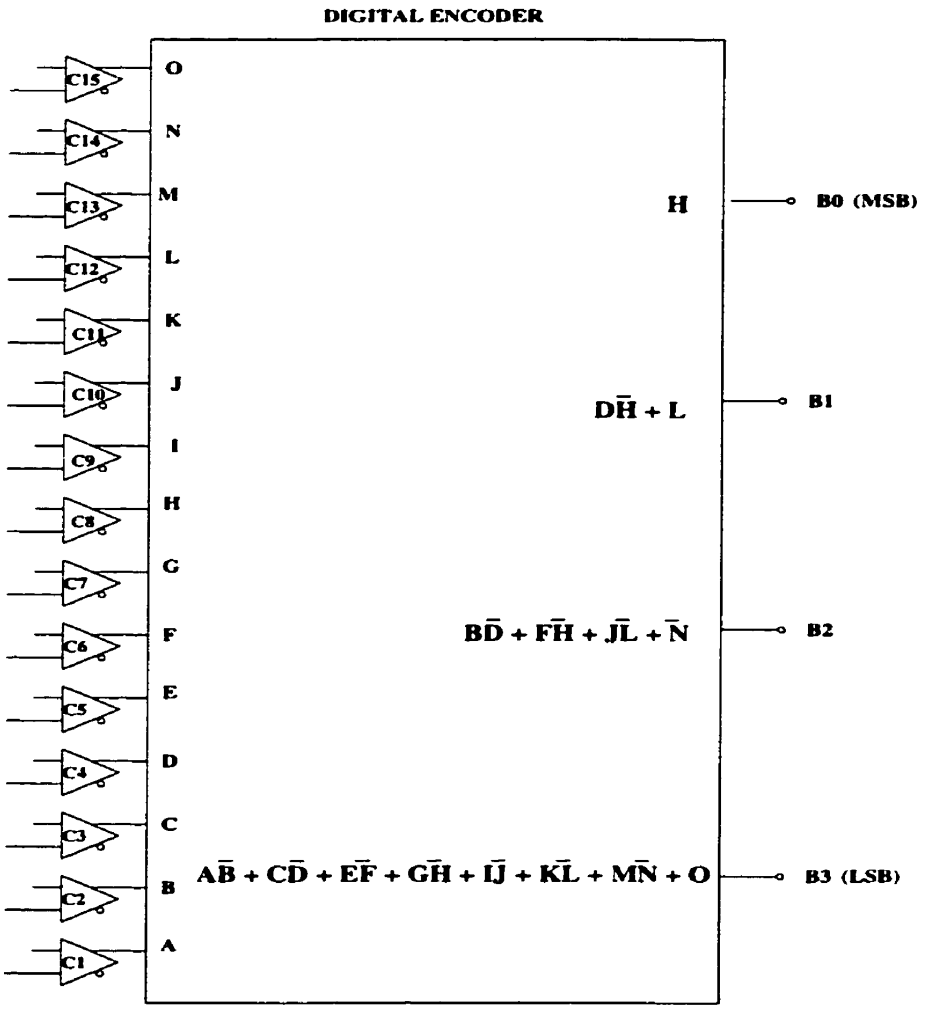


Figure 5.8: Logic equations for conversion of thermometer code into 4-bit word.

5.2.4 Floorplan for the Flash ADC

The floorplan for the entire flash ADC involved connection of the resistor string, the comparator block and the encoding logic. Two different floorplans for the flash ADC were constructed. The main difference between the layouts is resistor string type, the arrangement of the comparator block and the individual comparator layout. Two floorplans of the ADC were designed and subsequently fabricated in 0.35μm TSMC CMOS. The first floorplan, called ADC-1, used the *full-analog* layout of the comparator with each comparator block was placed below the other. As well, this layout used the rectangular resistor string block. The area occupied by this layout was 80,000 μm^2 and the layout is displayed in Figure 5.9. The second floor plan, labeled ADC-2, used the *digital-like analog* layout style of the comparator and placed the comparators in five rows of three devices. The resistor string used in this design was of the interdigitated type. This layout, shown in Figure 5.10, is more compact, only 15,000 μm^2, and thus occupies 5 times less silicon area than ADC-1.

5.3 Ensuring Testability of Building Blocks

Careful design of the comparator and flash ADC circuits is not enough to ensure a functional device after fabrication. A designer must consider how the circuits will be measured and evaluated. For bench top measurements, the circuit outputs will be measured using probes which will have a load capacitance. This capacitance will affect the circuit output and in some cases swamp the circuit such that no output is measurable. To reduce the effects of capacitive loading, the outputs of a circuit can be buffered. Another important consideration for testability, is to ensure that test structures are included on the chip to

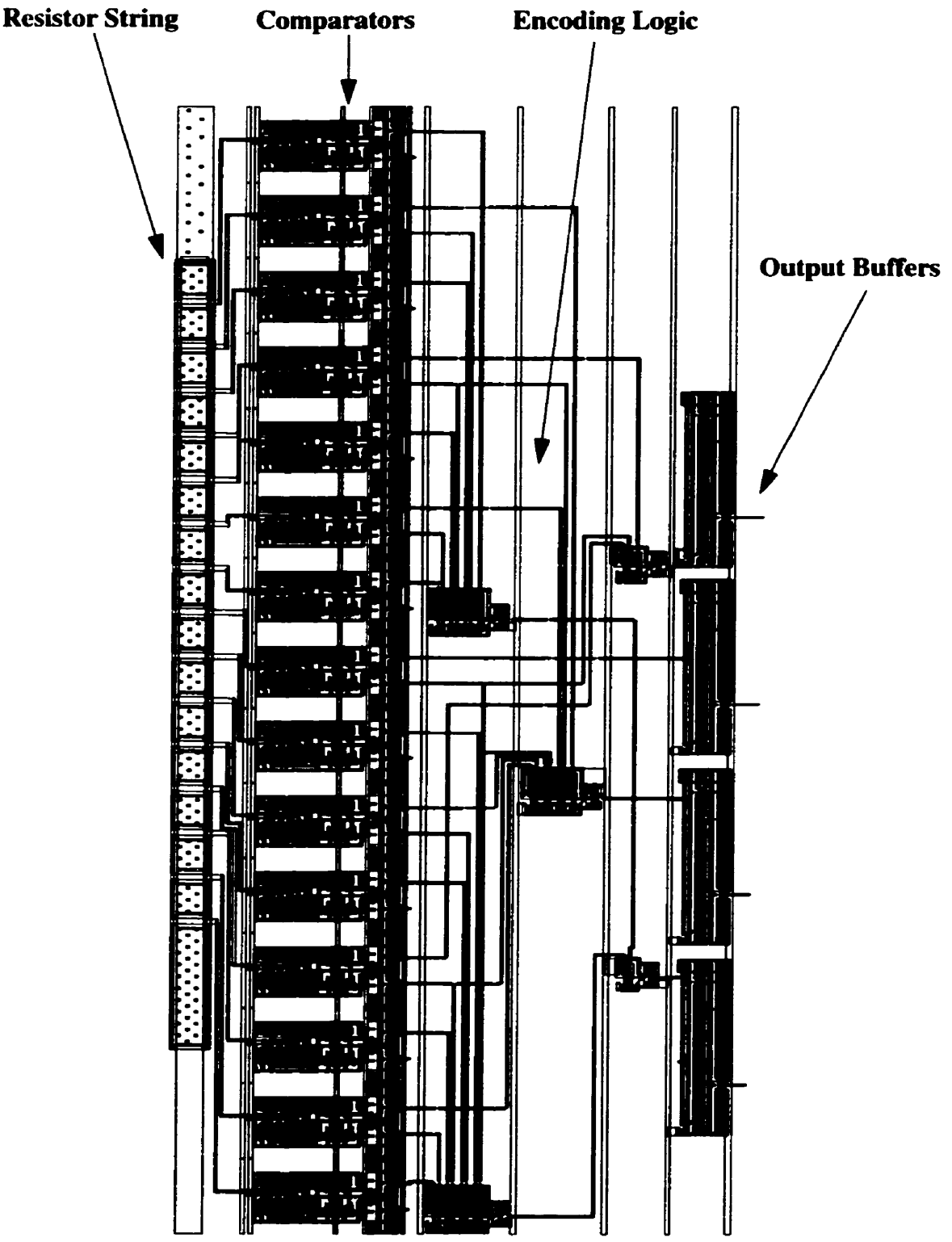


Figure 5.9: Layout of ADC-1.

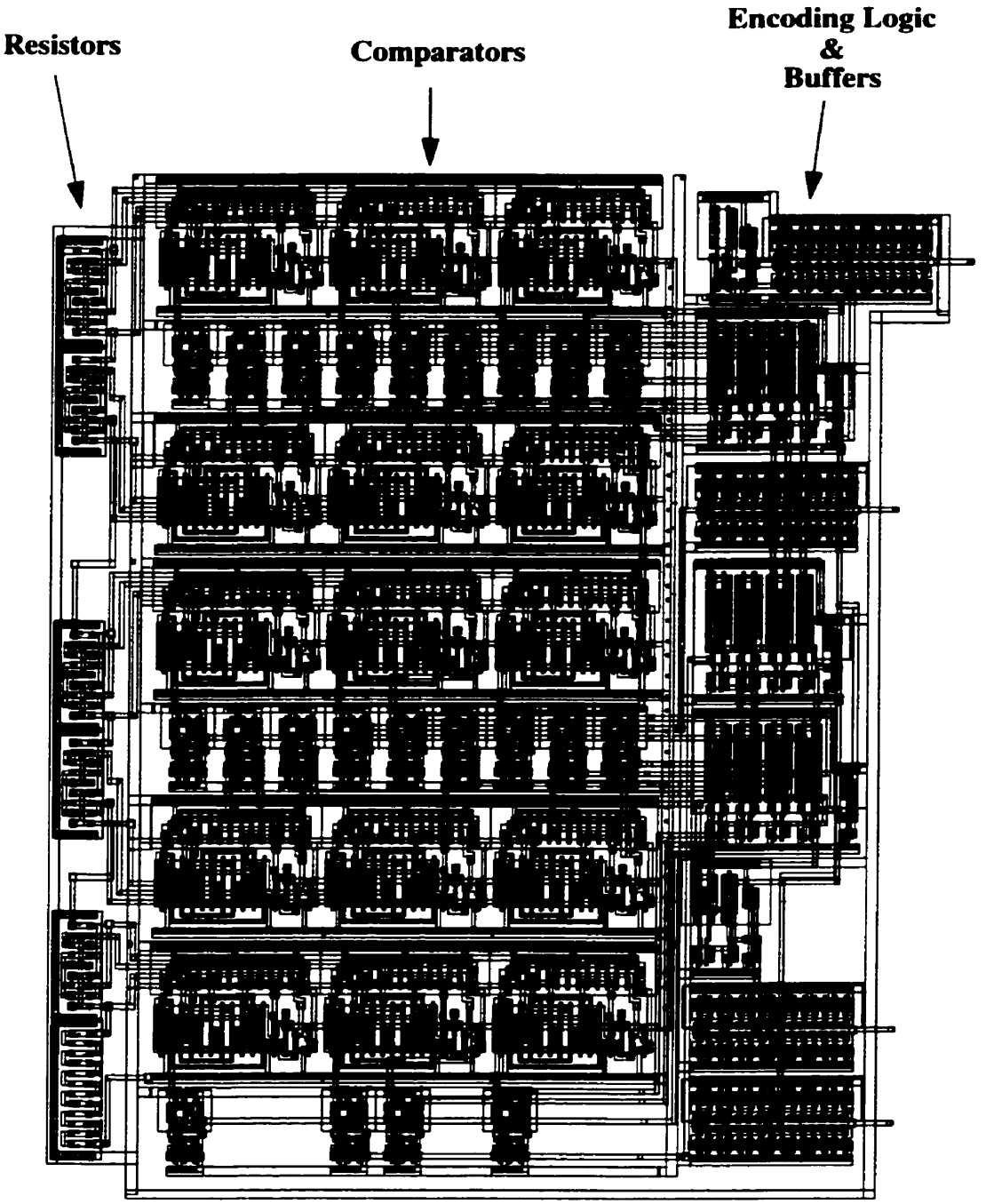


Figure 5.10: Layout of ADC-2

allow for circuit debugging in the event of a malfunctioning circuit.

5.3.1 Output Buffer Design

A digital output buffer has a high input impedance and a low output impedance which makes it useful for driving large capacitive loads. A simple buffer can be constructed from a single inverter. To increase the driving capacity of the buffer, a design can connect as many as four inverters in series to increase the output drive [21].

The buffer used for the buffering all of the outputs for all circuits designed in this thesis was constructed from the series connection of four inverters, as shown in Figure 5.11. The

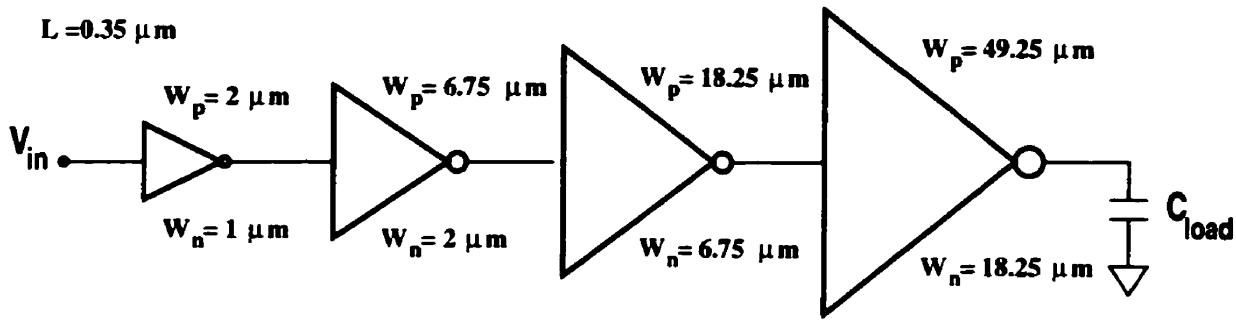


Figure 5.11: Output buffer consisting of four inverters.

buffer design scales the transistor dimensions of consecutive stages in an exponential fashion, by a factor of e^1=2.72. A multiple stage buffer is used to increase the switching speed of a buffer when a high capacitive load is at the output. The factor of e^1 is the optimal ratio between stages providing fast switching of the buffer [21].

To design the buffer, dimensions for the transistors of the first inverter must be selected then the dimensions of the following inverters are calculated by multiplying by the factor 2.72. The dimensions for the four inverters are noted on Figure 5.11. The length for both

the PMOS and NMOS transistors was 0.35μm and the corresponding widths are denoted with a p-subscript for PMOS transistors and with an n-subscript for NMOS transistors.

5.3.2 Test Structures for Flash ADC

Several test structures were constructed to help with interpretation of measurements results. The first test structure built was a stand alone resistor string which was used to determine the accuracy of the reference voltages generated from the different types resistor strings. The second test structure was a flash ADC without the decoding logic. With this structure, the comparator outputs to be directly measured through buffers, bypassing the encoder, which will facilitate circuit debugging should it be required. The final test structure was flash ADC that did not have an on-chip resistor string. With this structure, reference voltages for the fifteen comparators can be generated accurately off chip and input into the ADC. Using this method, it will be easy to pinpoint ADC operational errors due to improper reference levels. Each of these test structures, created for both ADC-1 and ADC-2, will be measured in the event of improper operation of the flash ADC to pinpoint errors in the device.

Chapter 6

Simulation of Layout-Related and Process-Induced Performance Variations

Before a circuit is sent for fabrication, the performance of the circuit can be evaluated on the layout level. Simulation of the layout performance involves two steps. First, a circuit extraction tool is used to transform the physical layout into a circuit netlist[1]. The circuit extraction not only includes the transistors contained in the layout but also includes parasitic capacitances resulting from the placement of conducting layers in the layout. The second step in the evaluation of circuit layout is to simulate the netlist generated from the extractor with a circuit simulator such as HSPICE. The netlist can be simulated using HSPICE for all process corners and an estimate of a circuit operation can be determined. Simulation of an extracted circuit layout is an important step in determining circuit characteristics because extraction provides information of how the layout design will affect the performance.

6.1 Circuit Extraction from a Layout

The circuit extractor used in this research was the DIVA Layout Parasitic Extractor, iLPE. iLPE extracts physical devices, complex parameters and parasitics from most technologies. To extract a layout, the DIVA must be supplied an extraction rules file that contains specific instructions about which devices and parasitics are calculated for a given technology. The extraction rule files for 0.35μm TSMC technology were provided by Canadian

1. A netlist is a list of semiconductor devices contained in a circuit and defines the connections of the devices to one another and to the power supplies.

Microelectronic Corporation (CMC). These extraction rules for 0.35µm TSMC extracts only active devices and vertical parasitic capacitances. The rules provided do not include calculations of parasitic resistances, lateral capacitances or account for reduced contacts in the source and drain region.

For all comparator and flash ADC designs, the layouts were extracted and simulated using HSPICE for each corner of the process. An example of a comparator circuit extracted from the layout is shown in Figure 6.1.This schematic has been generated from the extrac-

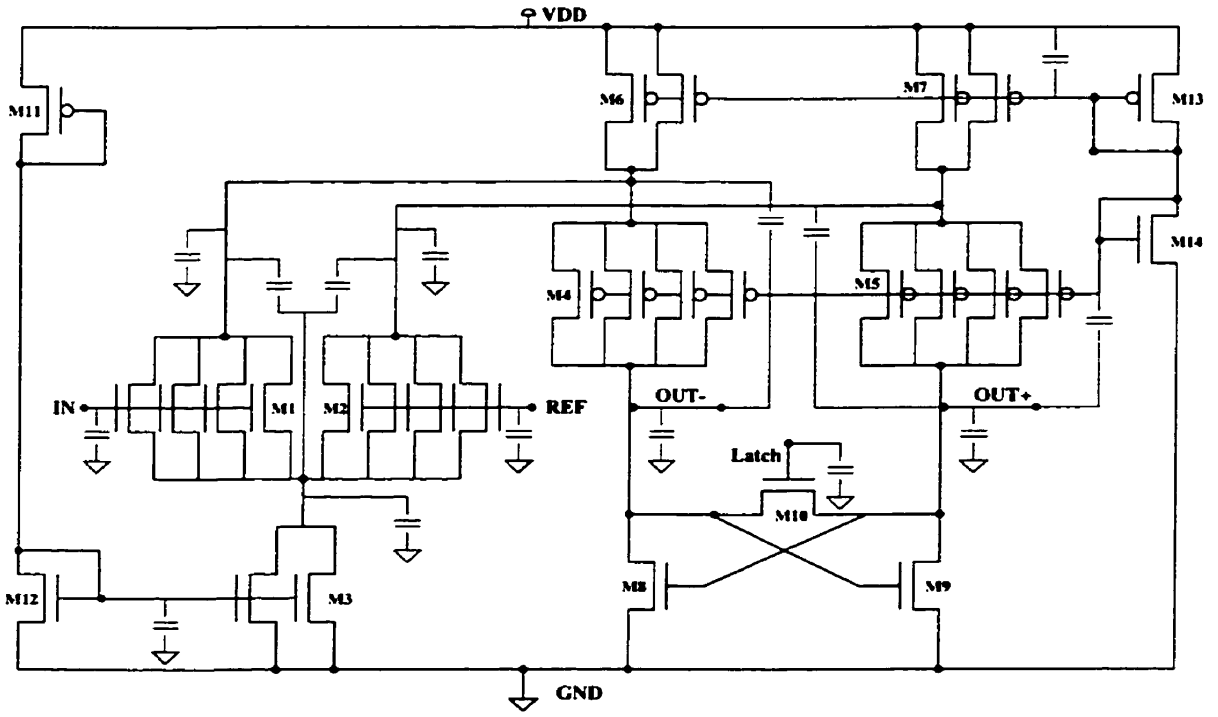


Figure 6.1: Extraction schematic for the full-analog layout of a latched comparator.

tion of the *full analog* layout of the latched comparator. Illustrated in this schematic is the splitting of transistors for matching and stacking as well as the parasitic capacitances generated from the layout. The quantity, value and placement of the parasitics is solely dependent on the placement of the conducting layers, metals, diffusions and polysilicon, in the

layout.

6.2 Considerations for Circuit Simulation

To obtain a good estimate of circuit performance, the HSPICE simulations of a circuit must include extraction of the layout, simulation through all process corners and the inclusion of circuits that will be needed for bench-top measurements of the fabricated device. For the comparator simulations, the netlist will need to include the extracted netlist for the digital buffers described in Section 5.3.1 as well as the models that describe the parasitic effects of the device packaging chosen.

All of the comparator circuits were packaged in a high speed 44pin ceramic quad flat package (CQFP). This package was chosen for its high frequency operation ability due to its low parasitic capacitances. Even though this circuit is designed for high speed applications it still has internal parasitics associated with it. Moreover, it is important that the package parasitics be incorporated in the simulations to produce figures of merit that are as accurate as simulation allows. Unfortunately, a simulation model for this 44pin CQFP was not available, however, a model was available for a similar type 44pin ceramic package from BNR. The model for the 44pin BNR package is supported by CMC and includes LRC network models for the bonding wires connecting the chip to the bonding pads of the package and for the connection of the package bonding pads to the external pins of the package.

For the simulation of all comparator circuits the netlist included the extracted layouts for the comparator and buffers, models for the package and a load capacitance. All simulated

outputs were measured at the output pins of the package. Using this method provides more realistic simulation results that will better represent the characteristics of the final fabricated device.

The flash ADC layouts were extracted and simulated to ensure functionality before fabrication, but the performance of the ADC was not measured. The resistor layouts can not be extracted for simulation, thus resistors must be manually entered into the SPICE netlist to simulate the ADC. These ideal, perfectly matched resistors provide simulation results that are not representative of the final fabricated device and thus, are not included here.

6.3 Simulation Configuration for the Comparator

Due to the dynamic latch in the comparator, transient simulations were the only type of simulation that could be conducted to determine the comparator's operational characteristics. The netlists generated from the extracted comparator layouts, including extracted buffers, were simulated using HSPICE. In addition to the comparator and buffers, HSPICE models for the parasitic effects of the IC packaging were added to all of the inputs and outputs. A block diagram, in Figure 6.2, illustrates the method used in simulation of the comparator circuit. More detail on the simulation netlist can be found in Appendix A.

The reference and inputs of the comparator were simulated using a step function. The input voltage was stepped through a range of voltages while the reference remained constant. Then, the reference voltage was increased and the input was stepped through the range of voltages again. This combination of input and reference variation facilitated the

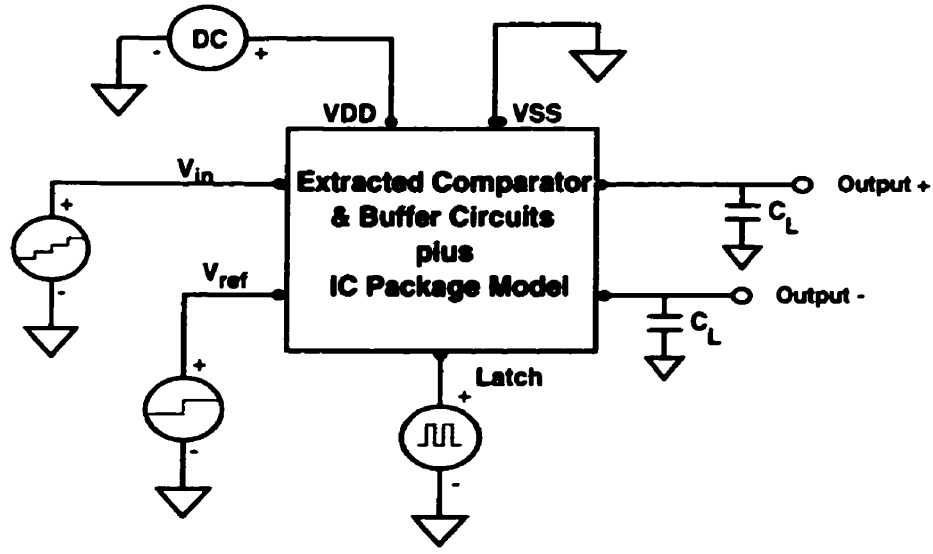


Figure 6.2: Block Diagram of simulation setup for the latched comparator.

measurements of the comparator resolution and input range. Constant dc sources were used to supply VDD = 3.3V and VSS = 0V. The latch signal was controlled by a square wave pulse function with V_{low}=0V and V_{high}=VDD. The frequency of the latch was synchronized with the input and reference step functions. For simulations of resolution and input range, all of the signals were set at a low frequency of 1kHz. After the input range and resolution were determined, the frequency was increased until improper output codes were identified. This measurement procedure was repeated for each process corner. A load capacitor of 1pF was attached to both outputs to simulate measurement using active oscilloscope probes. The outputs of the simulation were viewed and measured using the AWAVES graphical simulator interface.

6.4 Latched Comparator Simulation Results

The simulation measurements of interest for the latched comparator were the resolution,

comparison rate and the dynamic range. Table 6.1 lists the simulation results for the three layouts for the typical-typical corner model. The largest difference between the three lay-

Table 6.1: Comparison of comparator performance for different analog layout styles.

Parameter (worst case)	Analog Layout Style		
	Full	Partial	Digital-Like
Resolution	27 mV	31 mV	21 mV
Comparison Rate	156 MHz	118 MHz	110 MHz
Dynamic Range	3.1 V/V	3.1 V/V	3.1 V/V

out styles is seen in the comparison rate. A decrease in comparison rate can be attributed to increased capacitance in a circuit. Since the *digital-like analog* layout possessed the largest number of parasitic capacitors, the dramatic decrease in the comparison rate can be accounted for. The dynamic range, which is calculated from the input range of the comparator was found to be the same for all three devices. There is a small variation in the resolution of the three layout styles, with the *digital-like analog* layout presenting the best resolution. In general, the are definite performance variations visible in comparing one layout style to the next.

In addition to the simulations for the typical-typical model, the comparator circuit was simulated at all other corners of the process. The variation in comparator resolution over the corners is listed in Table 6.2.The resolution of the comparator is strongly affected by the corner analysis. The *digital-like analog* layout has the largest variation of resolution values followed by the *partial-analog* layout and the *full-analog* layout. These corner analysis simulation results indicate that the circuit performance is dependent on layout

Table 6.2: Comparison of comparator resolution for each layout at the different process corners.

Corner Model	Resolution (mV)		
	Full Analog	Partial Analog	Digital-Like Analog
Typical-Typical	27	31	21
Fast-Fast	15	0.5	14
Fast-Slow	22	22	3
Slow-Fast	40	46	49
Slow-Slow	55	39	62

under unfavorable processing conditions. For the *partial analog* and *digital-like analog* results, there was more than an order of magnitude difference in the resolution values for the different corners. This is most likely the result of the inability of the corner models, characterized for a digital process, to describe the operation of an analog circuit.

From these simulation results, it is possible to postulate that the *full-analog* layout has the best overall performance. This layout style has the high decision speed and is less affected by process variations. While the *digital-like analog* layout does have a promising lower resolution, it is important to remember that the extractor used to generate the netlists does not recalculate the drain or source resistance caused by the absence of reduced number of drain/source contacts. Recall that the *digital-like analog* layout does not have full contact coverage on the source and drain regions. As a result, it can be expected that the simulation results are somewhat optimistic and the actual measured circuit performance may be degraded. In general, a designer can't expect the measured results from the fabricated devices to be in complete agreement with the simulation results because the corner models represent $\pm 3\sigma$ statistical variations, however, it is conceivable to expect that the trends

exhibited in the measured layout performances will be in close agreement with the trends seen in the simulation results.

Chapter 7

Measurement Method for Fabricated Building Blocks

To completely investigate the dependence of analog circuit performance on layout design style, actual circuits must be fabricated and tested. Both the flash ADC and latched comparator were fabricated in 0.35μm TSMC CMOS technology available through the Canadian Microelectronics Corporation (CMC). In this chapter, the measurements techniques used for testing the fabricated building blocks will be described.

7.1 Description of Test Fixture

Both the fabricated comparators and ADC's were measured to compare the performance of the different layout design styles. Testing of the chips involved constructing a custom test board to allow easy measurement of the fabricated devices. The test board, depicted in Figure 7.1, consisted of a 44pin socket that the chips under test were inserted into. The

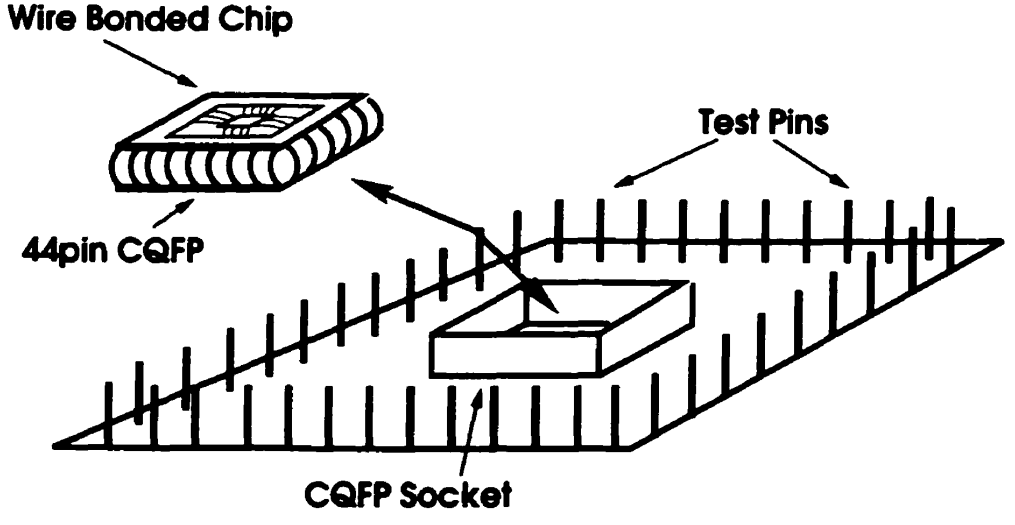


Figure 7.1: Diagram of testing board for all devices.

socket was connected via wire and solder to the test pins located around the periphery of the test board. It is important to note that the simulation results presented earlier, only accounted for the package parasitics and did not consider the parasitics associated with the socket and the soldered wires.

7.2 Latched Comparator Measurement Procedure

The goal of the latched comparator measurements was to measure and compare the resolution and maximum operation speed for all three layout design styles. The measurement configuration for the latched comparator is shown in Figure 7.2. The measurement

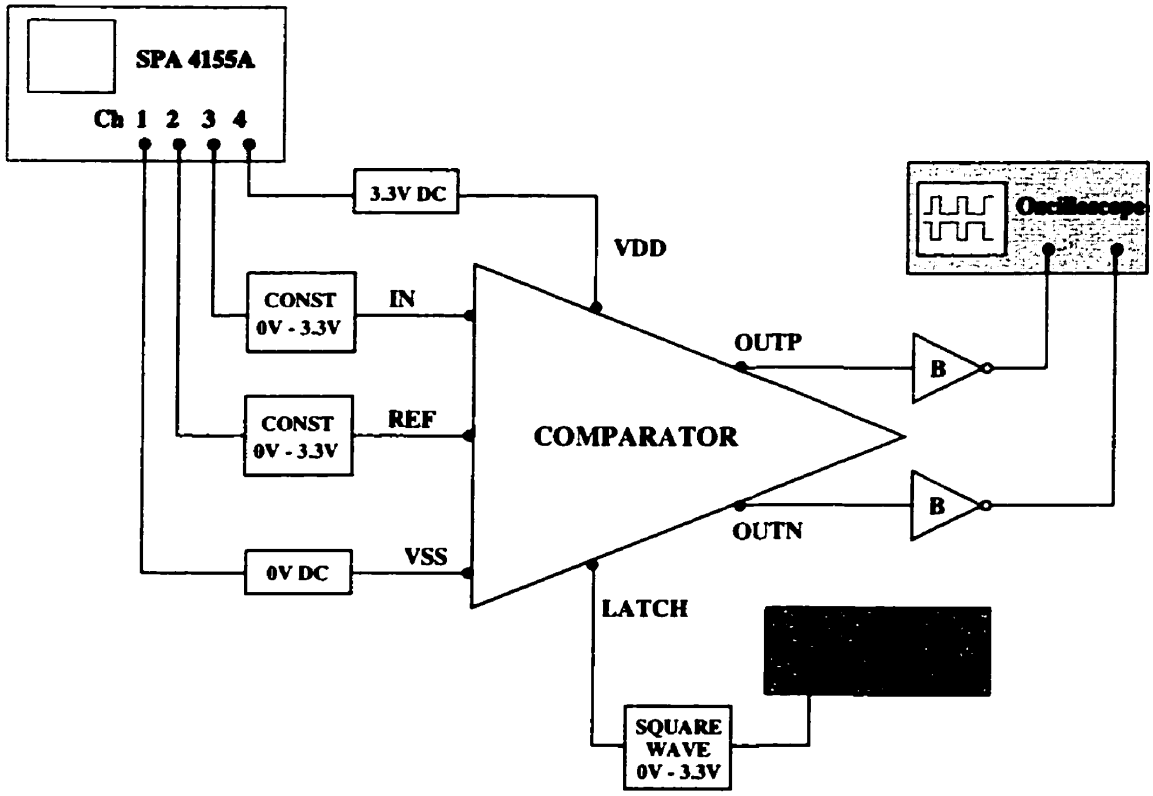


Figure 7.2: Measurement setup for the comparator in 0.35µm CMOS.

method was a static measurement where only one constant voltage was applied to the

inputs at a time. While this measurement process was time consuming, the measurements were performed as such to mirror the HSPICE simulation environment thus ensuring accurate results. The VDD and VSS power supplies and the constant DC voltages for the two inputs of the comparator were delivered by a semiconductor parameter analyzer (SPA4155). A 50MHz Wavetek function generator was used to control the latch signal with a square wave pulse. The outputs of the comparator were observed on a 500MHz Tektronix digital storage oscilloscope (TDS 3054). The oscilloscope probes used were 1GHz Tektronix active probes (P6243) with a capacitive loading of <1.0pF.

The Wavetek function generator used to measure the comparator and ADC had a degraded performance in the upper (>20MHz) frequency ranges. As the frequency of the generator was increased beyond 20MHz, the square wave became more sinusoidal-like and the amplitude increased. Unfortunately, this was the best function generator available thus, the measurements of the comparator and ADC still proceeded. The increase in amplitude of the latch signal beyond VDD could damage the latch gate oxide. In addition, the increased gate voltage could cause the latch transistor to move out of the saturation region of operation and into the linear region. However, during the measurements the increased amplitude and the sinusoidal-like square wave did not appear to have any effect on the performance of either the comparator or flash ADC.

The measurements of the comparator were carried out in three stages. First, the input gate currents were measured to determine if there was any damage to the gate oxide of the input gates. The gate oxide of the input transistors may posses defects that were generated during fabrication. Additionally, the gate oxide may have been damaged during packaging

or during measurement from exposure to an ESD[1] event. Damage to the gate oxide results in a high gate current conduction and affects the performance of the device under test. A damaged input gate was defined as one that exhibited a high gate current (>2μA) through an input voltage range of 0 - 3.3V. For an ideal transistor, the input resistance is on the order of 10^{15} and therefore, the gate current should be in the range of 10^{-15}A. The noise floor of the SPA was in the range of 5-10pA, thus typical devices with an undamaged gate oxides possessed gate currents in this range. However, some devices did exhibit gate currents in excess of micro and milli amps. Devices with gate currents >2μA were found to have degraded performance and in some cases no circuit operation was observable. The gate current measurement was accomplished by grounding VDD, VSS and both outputs and ramping the voltage on the input terminal of interest from 0V to 3.3V. When the voltage ramp was applied to one input, the other two input terminals were left floating. Any devices exhibiting gate currents of >2μA were not tested further.

Next, the comparator was characterized for low frequency. The low frequency measurements facilitated the measurement of the resolution and input range of the comparator under test. For these measurements, the latch frequency was set to 1kHz and the resolution was measured by manually reducing the difference between the input and reference voltages until improper comparator operation was observed. Through this measurement technique, the input range of the device could also be measured.

The final step in the measurement of the comparator was to measure the maximum operat-

1. Electro-Static Discharge: high voltages result in large electric fields and high current densities in small geometry silicon devices which can lead to breakdown of insulators and thermal damage in the IC [22]

ing frequency. Constant dc values of V_{in} and V_{ref} were applied and then the latch frequency was increased from 1 MHz to 50MHz in steps of 1MHz. The upper limit of 50MHz was set by the function generator available. The latch frequency was increased systematically until improper comparator operation was observed. The frequency at which the comparator was still working was recorded as the maximum frequency of operation. All three comparator layouts were measured using this same technique.

7.3 Flash ADC Measurement Procedure

The evaluation of the two flash ADC layouts, ADC-1 and ADC-2, was needed to determine the effects of comparator layout on system performance. The measurement configuration for the flash ADC is shown in Figure 7.3. The equipment used to measure the flash ADC was the same as the equipment used for comparator measurements and has been mentioned above in Section 7.2. In addition to the comparator setup, two extra oscilloscope probes were required to measure the four outputs of the ADC. Unfortunately, only two active probes were available therefore, two outputs of the ADC were measured using 500MHz Tektronix passive probes (P6139A) with capacitive loadings of 8.0pF. The probes, used to monitor B1 and B2, did introduce some minor delays on the output signals but did not affect the overall circuit performance.

Several measurements were required for the flash ADC. First, measurements of the reference voltages generated from the resistor strings were measured. The reference levels produced by the resistor string are important in determining the transfer function of the ADC. Next, the functionality of the logic blocks was tested. Testing of each block involved simple verification of the logic block's truth table. After verifying that the resistor and logic

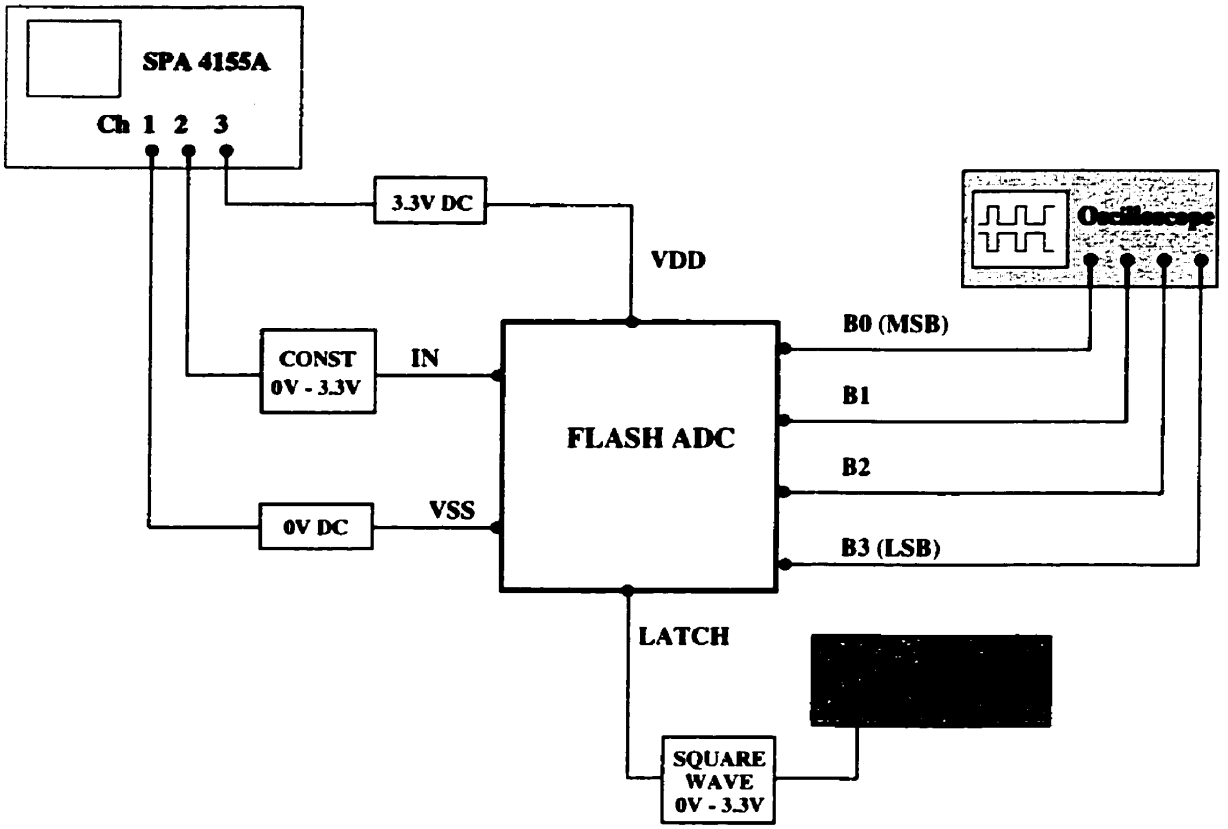


Figure 7.3: Block diagram of testing configuration for flash ADC.

building blocks were functional, the transfer function of the flash ADCs were measured.

The first step in the transfer function measurement of the ADC was to check the input gate currents to determine if the device was operational and suitable for testing. Next, the transfer function of the ADC was measured at low frequency. This was accomplished by manually sweeping the input range to determine the output code transition levels. Once the transfer function was determined, the maximum operating frequency of the converter was measured. To determine the maximum output rate of the ADC, the input voltage was set at a constant level to produce one output code, i.e. 1011. At this point, the latch frequency was increased until improper operation of the ADC was observed. Both ADC layouts were subject to the same measurement techniques.

Chapter 8

Measurement Results and Analysis

This chapter presents the measurement result for the all the latched comparator and flash ADC layout design styles. In addition, the measurement results are analyzed and compared with the simulation results.

8.1 Measurement Results for Different Comparator Layouts

Six chips from one fabrication run, each containing a *full-analog*, *partial-analog* and *digital-like analog* comparator layout, were measured as described previously in Section 7.2. Chip number three was unmeasurable due to a lack of output response from any of the layouts. Some of circuits from chips numbers four and five had high input gate currents and thus the data was not collected. Measurement data for the functioning layouts with gate currents <2μA is listed in Table 8.1. These measurement results indicate that the *full-analog* layout, on average, has a higher resolution than the *digital-like analog* layout. The *partial-analog* layout does exhibit some promising resolution measurements, however, there are also some resolution values that are grossly out of range. This drastic variation in the resolution of the *partial-analog* layout could indicate that this layout is more susceptible to process variations which can cause large fluctuations in the performance parameters. The dynamic range is similar for all three layouts indicating that the input range of the comparator is not affected by layout design style. As well, the majority of chips measured were functioning up to the maximum frequency supplied by the function generator. The *partial-analog* layout, on average, has a lower comparison rate than the other two layouts styles. However, the frequency of operation fluctuates for this layout

Table 8.1: Measurement results for three latched comparator layouts.

Layout Style	Chip Number	Comparator Parameter		
		Resolution (mV)	Frequency (MHz)	Dynamic Range (V/V)
Full Analog Layout Style	1	80	48†	3.2
	2	40	50	3.1
	4	65	45	3.0
	6	130	45†	3.1
Partial Analog Layout Style	1	100	40	3.0
	2	500	30†	2.9
	5	40	41†	3.1
	6	45	50†	3.2
Digital-Like Analog Layout Style	1	140	50	3.0
	2	130	29†	3.0
	4	130	50	2.9
	5	110	47†	3.0
	6	70	50	3.1

† coupling of positive and negative outputs observed.

style possibly as a further indication of the susceptibility of the layout to process variations.

The trend of these measurement is similar to the conclusions drawn from the simulation results that the *full-analog* layout provides the best performance in resolution and speed. However, all of these layouts exhibit some discrepancies in all parameters suggesting that all the layouts are potentially susceptible, to a varying degree, to process variations. To

provide more concrete conclusions a larger sample base is needed.

During the high frequency measurements of the comparator an interesting phenomena was observed on several chips for different layouts. This phenomena resulted in the coupling of the positive and negative outputs during a certain frequency range producing non-complementary outputs. This coupling tended to disappear at a higher frequency. As well, the coupling was also affected by repositioning of the leads from the function generator and the oscilloscope, hence, we concluded that the coupling was due to measurement technique and not the circuits under testing. The frequencies measured and listed in Table 8.1 correspond to the frequency at which the comparator stopped functioning properly and if the coupling was observed at some lower frequencies, generally around 20MHz, it was noted in the table.

Measurement data for the high frequency measurements were downloaded from the oscilloscope. For each layout, the latch signal and both outputs were recorded for three frequencies, 10MHz, 30MHz and 50MHz. Each of the layout styles exhibited similar outputs at these test frequencies and thus only one example, the *full-analog* layout, is shown here. As an example, the outputs of the full analog layout, chip # 2, are shown in Figures 8.1, 8.2 and 8.3, respectively. These three figures also display the simulation data for the same latch frequencies. The simulation data was obtained from HSPICE simulations of the extracted comparator layout, the extracted buffer layouts and the model for the chip packaging as described in Appendix A. For the measured data V_{in} = 1.2V and V_{ref} = 1.0V and the resulting proper operation of the comparator shows V_{out+} = high and V_{out-} = low when the latch signal is low. As the frequency of the latch is increased, the comparator is

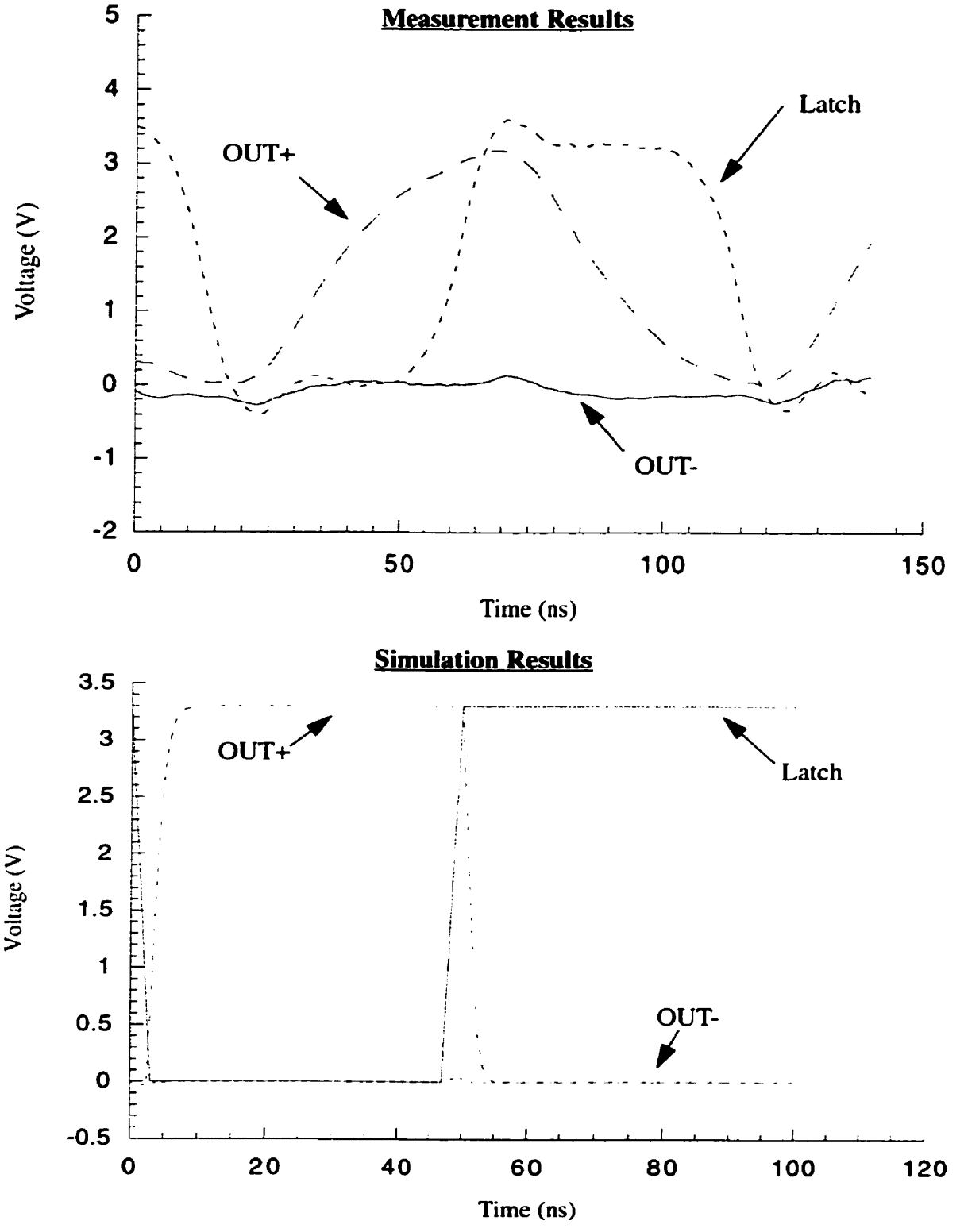


Figure 8.1: Measured and simulated outputs for latch frequency = 10MHz for the *full-analog* comparator.

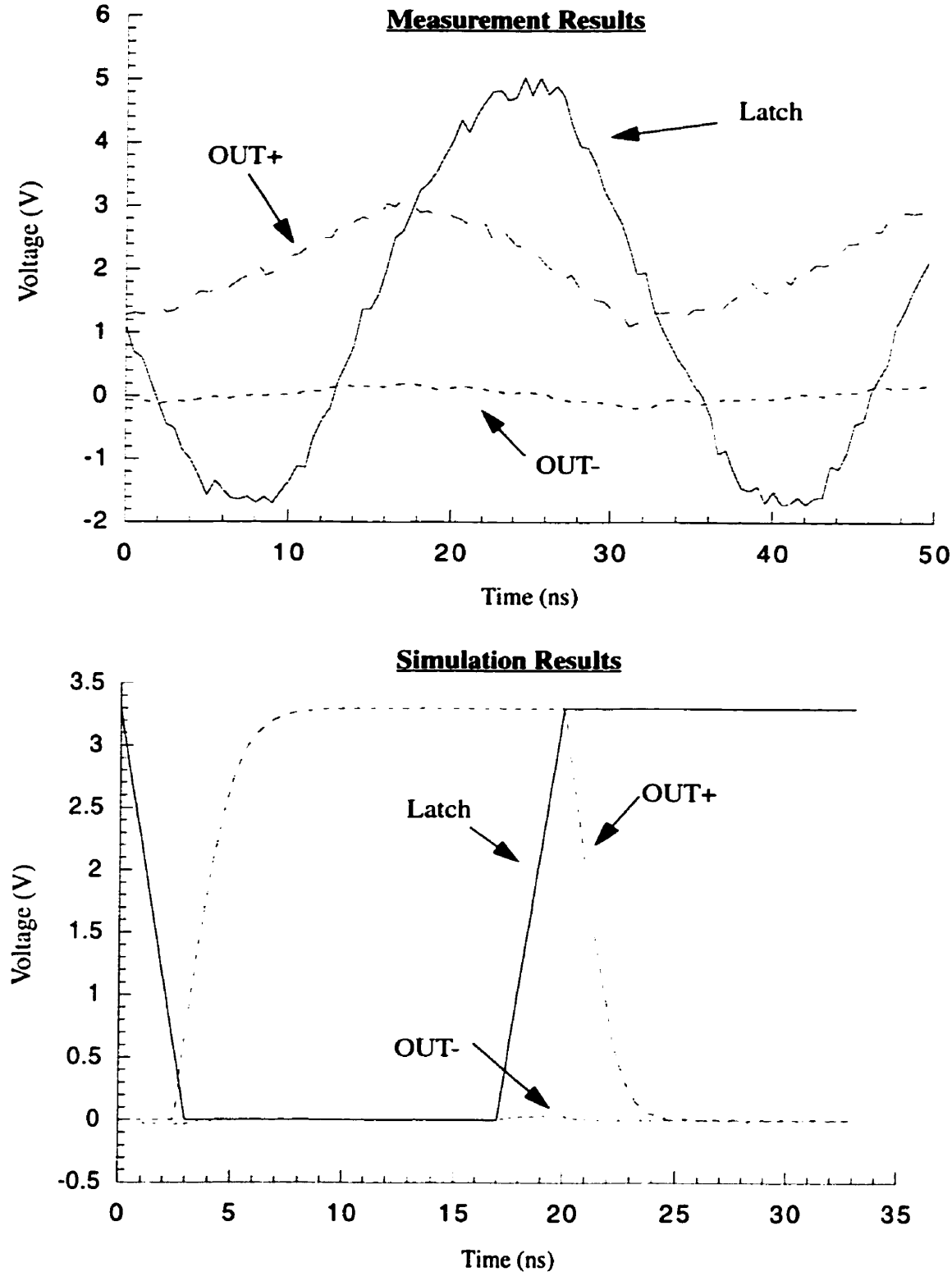


Figure 8.2: Measured and simulated outputs for latch frequency = 30MHz for the *full-analog* comparator

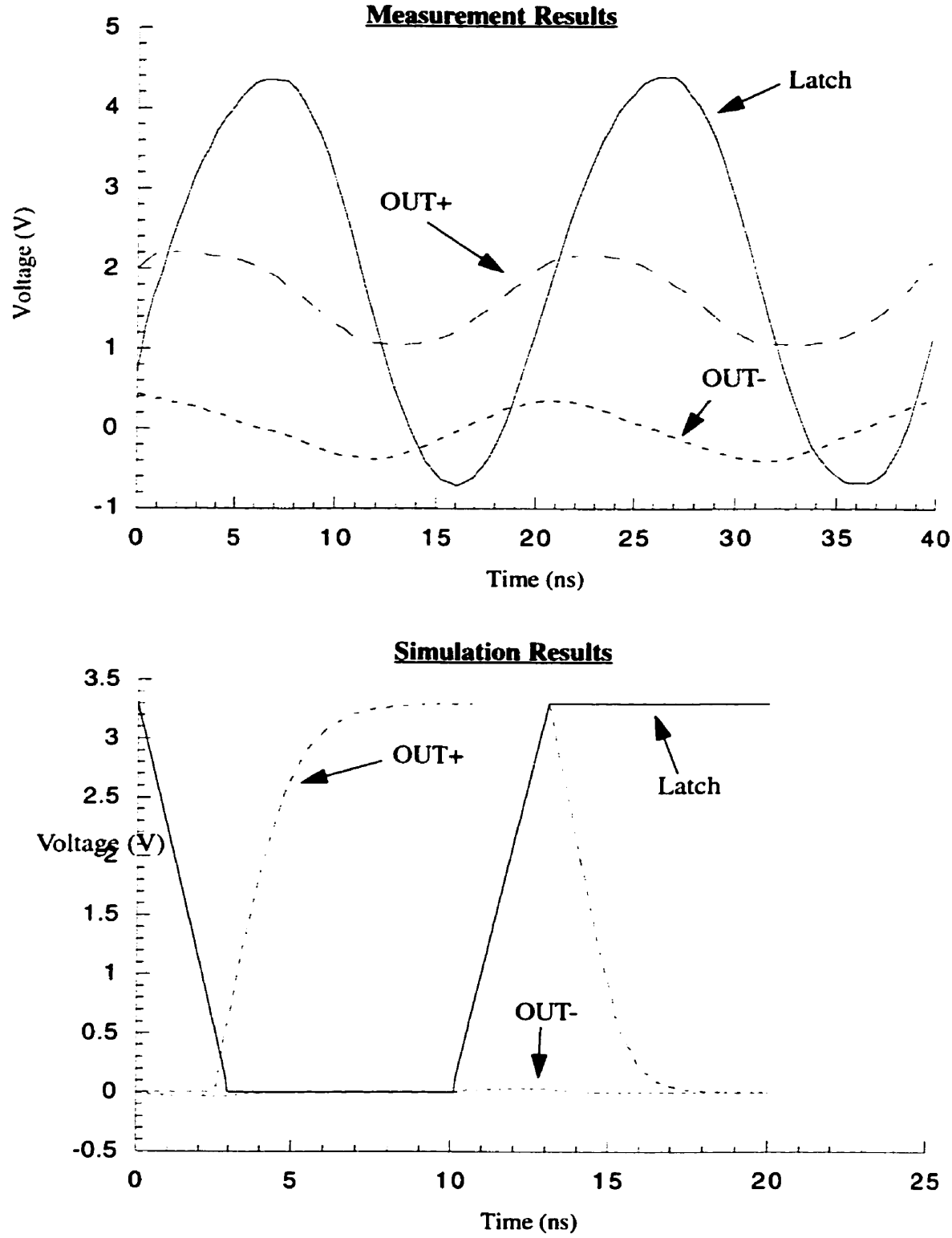


Figure 8.3: Measured and simulated outputs for latch frequency = 50MHz of the *full-analog* comparator.

still functioning properly but the positive output does not have enough time to reach full VDD or full VSS. This sluggish-ness in the output is most likely not a true characteristic of the comparator but is a measurement of a delay introduced by the test fixture. This conclusion can be further supported by comparing the simulated results to the measured results. The rise and fall times of the positive output is much shorter in the simulation results. Since the simulation included the buffers and the parasitics of the 44pin CQFP package and not the parasitics associated with the test fixture, it can be concluded that the test fixture parasitics are overwhelming the signal at high frequencies. This phenomena of limited output voltage swing was observed for all three layout styles at the high frequencies. To avoid this problem and to measure the true comparison rates of the comparators, an on-chip testing system is needed. However, the buffers and the test fixture were the same for all layout styles measured and thus, the comparison between the layout styles is still valid.

8.2 Flash ADC Measurement Results

Two flash ADC structures were designed and fabricated, ADC-1 and ADC-2, in 0.35μm TSMC CMOS technology. ADC-1, as described in Section 5.2.4, consisted of a rectangular resistor string and full-analog layout comparators. Moreover, ADC-2 was comprised of an interdigitated resistor string and digital-like layout comparators. The first step in measurement was to test the functionality of the resistor string and the logic blocks, then proceed with the measurement of the ADC's.

8.2.1 Measurements of the Resistor String

Test structures of the resistor string were included on each chip to measure the reference

voltages produced by each resistor string. This measurement not only will be used in the plotting of the ADC transfer function but also can be used to determine how well the resistors were matched. Measurement of the resistors was accomplished by connecting the nwell and the terminal of the first resistor to VDD and connecting the end of the last resistor to VSS, as previously shown in Figure 5.5. Then an oscilloscope was used to measured the reference voltages produce at each point in the ladder. This procedure was identical for both the rectangular and interdigitated resistor strings. Several resistor strings were measured and an sample of the results is listed in Table 8.2. This table lists the values of the fifteen different reference voltages generated from each of the resistors strings. The column labeled LSB is calculated as the difference between two consecutive reference voltages. For the ideal case, the LSB value, or the amount the input voltage must increase to increases the output by one bit, should be constant. A larger deviation between the reference levels generate indicate a lower degree of resistor matching.

From the data, the rectangular resistor string has a superior matching between resistors than the interdigitated string. From the theory, it was expected that the interdigitated resistor string would have superior matching qualities. The results here are to the contrary and are most likely the result of mismatches cause overetching of the edge resistor fingers. As in the case with edge transistor gates, the edge resistor fingers should also be protected by dummy strips. The dummy strips eliminate boundary etching effects and improve the resistor value.

In addition, the value of the resistor depends on the edge terminations and the contacts between the resistor strips and the metal lines [11]. Both the interdigitated resistor and the

Table 8.2: Voltage reference values for two resistor strings.

Voltage Reference	Rectangular Resistors (V)	LSB Value (V)	Interdigitated Resistors (V)	LSB Value (V)
1	3.05		3.13	
2	2.88	0.17	2.96	0.17
3	2.72	0.17	2.79	0.17
4	2.56	0.16	2.62	0.17
5	2.39	0.17	2.45	0.17
6	2.22	0.18	2.27	0.18
7	2.04	0.19	2.08	0.19
8	1.88	0.16	1.91	0.16
9	1.71	0.17	1.74	0.16
10	1.53	0.16	1.53	0.21
11	1.37	0.19	1.40	0.13
12	1.19	0.16	1.24	0.17
13	1.03	0.16	1.05	0.19
14	0.86	0.17	0.85	0.20
15	0.69	0.17	0.67	0.18
	Mean	0.17	**Mean**	0.18
	Deviation	0.01	**Deviation**	0.02

rectangular resistor were designed to have the same nominal value but the interdigitated resistor was divided into three separate sections. The three sections of each resistors were interconnected with vias, metal1 and metal2 layers whereas for the rectangular resistor each resistor was connected only with metal1 and contacts. The poor performance of the interdigitated resistor string can also be attributed to a mismatch in resistances of contacts from the diffusion to metal1 and the vias from metal1 to metal2. In an interdigitated group of three, each resistor has a different contact configuration and slightly different metal

lengths. These design differences contribute to the resistor mismatch.

8.2.2 Testing Functionality of Digital Encoding Logic Blocks

There were four digital building blocks that were designed for the digital encoding block, an 8 input AND/OR gate, a 7 input AND/OR gate, a 3 input AND/OR gate and a simple OR gate. Each gate was cycled through its truth table to ensure proper output states. All blocks were found to be functional and all reproduced their appropriate truth tables. After verifying the functionality of the resistors and encoding logic, the next step was to measure the flash ADCs.

8.2.3 Measurement of Flash ADC-1

Six chips, from one fabrication run, with the ADC-1 layout were measured. The first measurements were to check the input gate and latch gate currents. Only one chip, chip #3, was unable to be tested due to high gate current. Next, the transfer function of the comparator was measured. The input voltage was ramped across the input range to determine the values of input voltage which cause a change in the output word. The transfer function provides information on the offset error, gain error and integral and differential non-linearity. The transfer function of the measured comparators is plotted along with the expected transfer function derived from the measurements of the resistor string in Figure 8.4. There is a noticeable deviation of the measured transfer curve from the expected function. To quantify the error of the transfer function measured, ADC parameters offset and gain error and the differential and integral non-linearity were used. These values can be extracted from the ideal and measured transfer functions. The four ADC parameters were measured for all 5 chips and averaged. The average of these measured values are summarized in

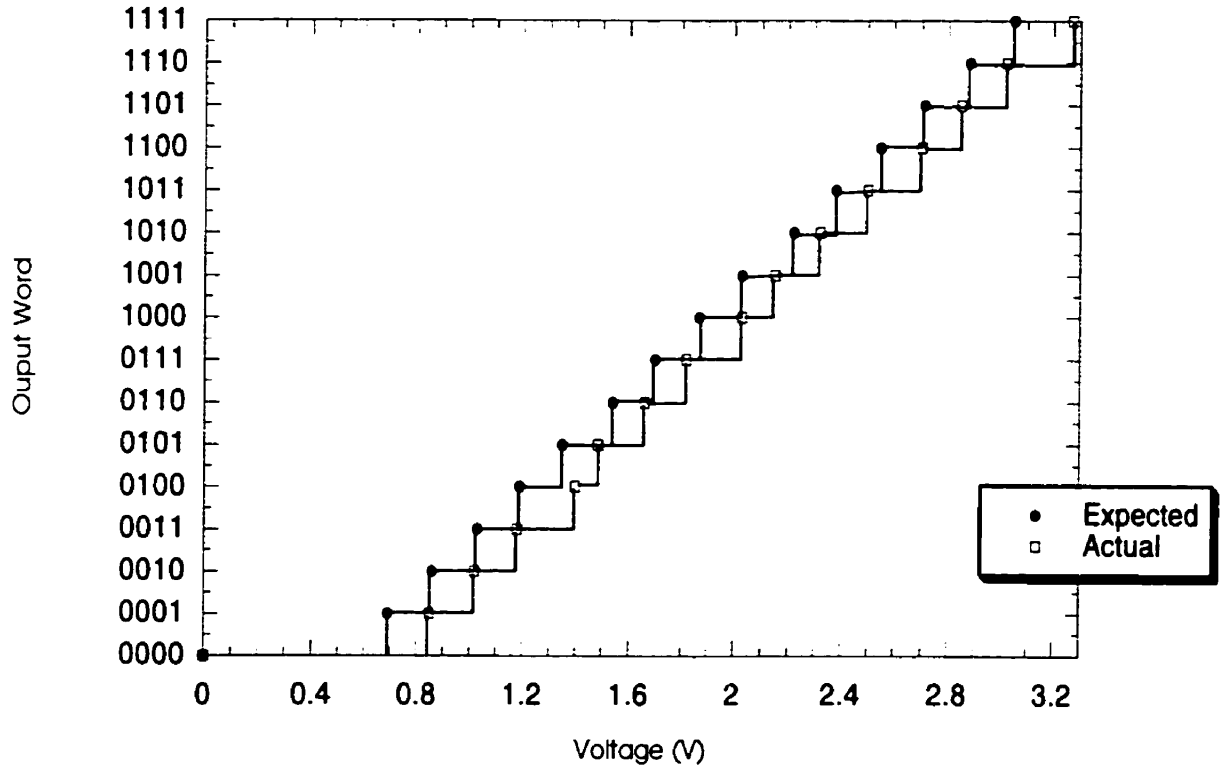


Figure 8.4: Transfer function for ADC-1.

Table 8.3. along with silicon area the layout occupies.

Table 8.3: Average performance specifications for ADC-1.

Resolution	4 bits
Offset Error	0.16 V
Gain Error	0.39 V
Integral Non-Linearity	± 1 LSB
Differential Non-Linearity	± 0.5 LSB
Conversion Frequency	46 MHz (max)
Power Supply	3.3V
Silicon Area	80,000 μm^2

Next, the maximum frequency of operation for ADC-1 was measured. The input voltage of ADC-1 was set to 2.6V which produced a corresponding output word of 1011. The latch frequency was then slowly increased until improper output codes were observed. From the measurement of the 5 chips, the average maximum frequency of operation was found to be 45MHz ± 1MHz. Operation of ADC-1, chip #2, at the maximum frequency of 46MHz is presented in Figure 8.5. These graphs were created from data downloaded off of the oscilloscope. The figure depicts a 1011 output, when the latch signal is low, corresponding to the applied input of 2.6V. The ADC-1 has sufficient time during the latch = low cycle to reach full VDD and VSS outputs. ADC-1 is not limited by the testing board as was the case for the latched comparators. Finally, some output coupling that was seen when measuring the comparator was also visible during the measurements of ADC-1. Again, the coupling was concluded to be the result of the measurement method.

8.2.4 Measurement of Flash ADC-2

Six chips, from the same fabrication batch as ADC-1, with the ADC-2 layout were measured. The first measurements were to check the input gate and latch gate currents. Only one chip, chip #3, was unable to be tested due to high gate current. After gate current verification, the transfer function of the ADC was measured. The input voltage was ramped across the input range to determine the values of input voltage that caused a one bit increase in the output word. The transfer function provided information on the input range of the device, gain and offset errors and the integral and differential non-linearity. The transfer function of the measured comparators is plotted along with the expected transfer function derived from the measurements of the interdigitated resistor string in Figure 8.6. Comparing the measured and expected transfer functions, it is easy to see that there is a

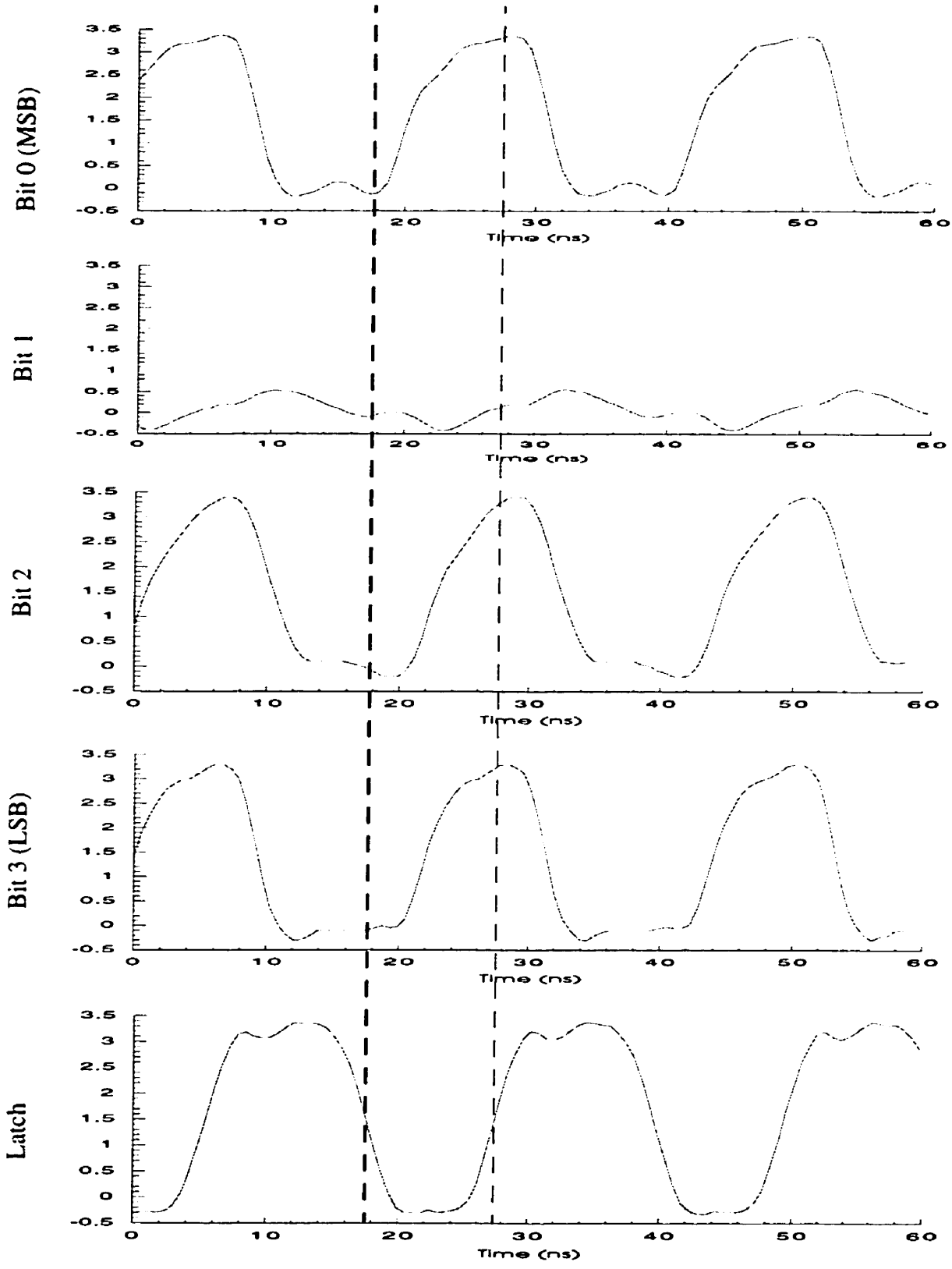


Figure 8.5: Measurement results of ADC-1 for Vin=2.6V with the latch frequency = 46MHz.

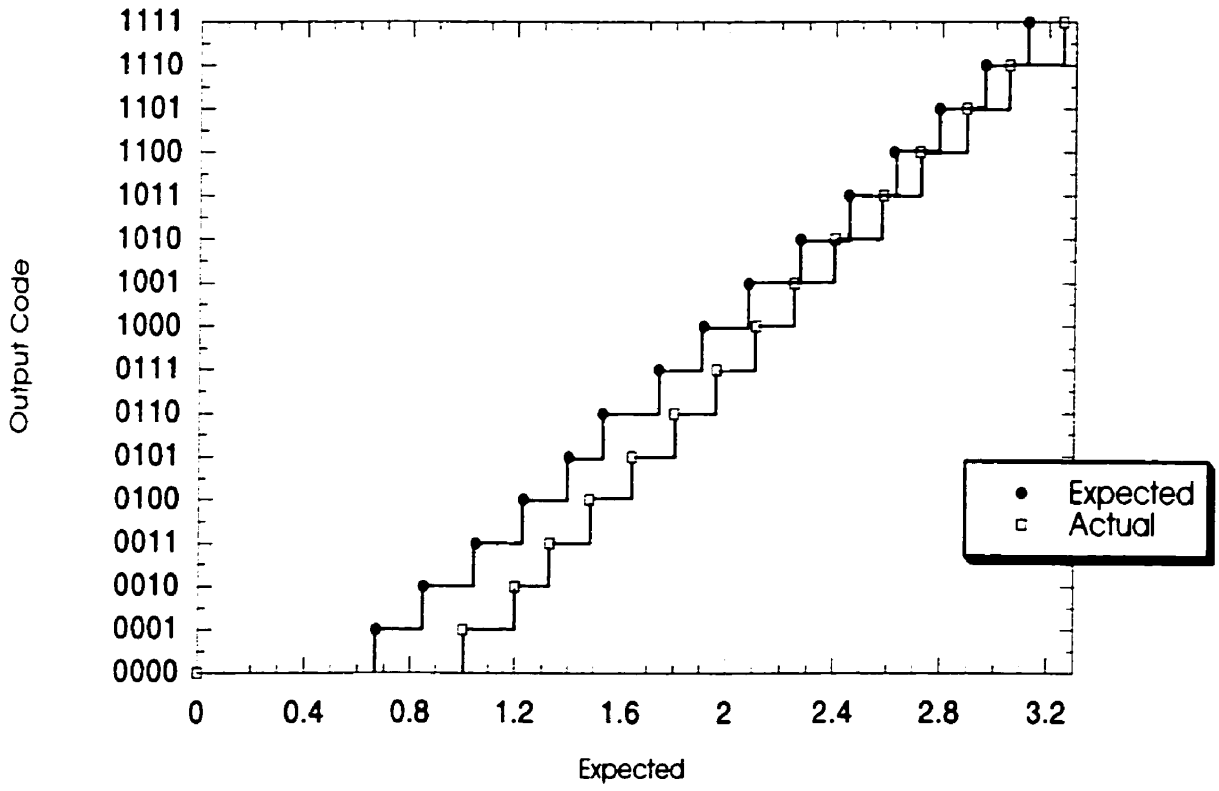


Figure 8.6: Transfer function for ADC-2.

much larger deviation between the two than was the case for ADC-1. Averaged measurement results for the 5 chips are listed in Table 8.4. All of the calculated values, offset error,

Table 8.4: Average performance specifications for ADC-2.

Resolution	4 bits
Offset Error	0.35 V
Gain Error	0.57 V
Integral Non-Linearity	$\pm$ 2 LSB
Differential Non-Linearity	$\pm$ 0.25 LSB
Conversion Frequency	33 MHz (max)
Power Supply	3.3V
Silicon Area	15,000 μm^2

gain error and integral nonlinearity are much larger than in the case of ADC-1. Only the differential nonlinearity is lower than that found in ADC-1. The differential non-linearity is a measure of the maximum deviation in step size of the transfer function from the expected size of one LSB. ADC-2 has smaller variation in step size than that of ADC-1.

Next, the maximum frequency of operation for ADC-2 was measured. The input voltage was set to 2.6V which produced an output word of 1011. The latch frequency was then slowly increased until improper operation was observed. The average maximum frequency of operation was found to be 31MHz $\pm$ 2MHz. Figure 8.7 depicts the operation of one instance of ADC-2, chip #2, at 32MHz. The input voltage was 2.6V and the corresponding output word of 1011 is displayed in the outputs when the latch signal is low. Output cross coupling that was seen when measuring the comparator was also visible during the measurement of the ADC.

Comparing the performance of ADC-1 and ADC-2, ADC-1 has a higher decision rate and a lower gain, offset error and integral non-linearity. Measurements of the latched comparator layouts indicate that the *full-analog* layout has a superior performance over the *digital-like analog* layout style and this is further supported by the noticeable variation in operation of the two ADC layout styles. However, ADC-2 does rely on the interdigitated resistor string to provide its reference voltages. This resistor string was found during measurements to have a poor matching quality, which might have had an effect on the performance. However, this effect was minimized because the expected transfer function was derived from direct measurement of the test interdigitated resistor string.

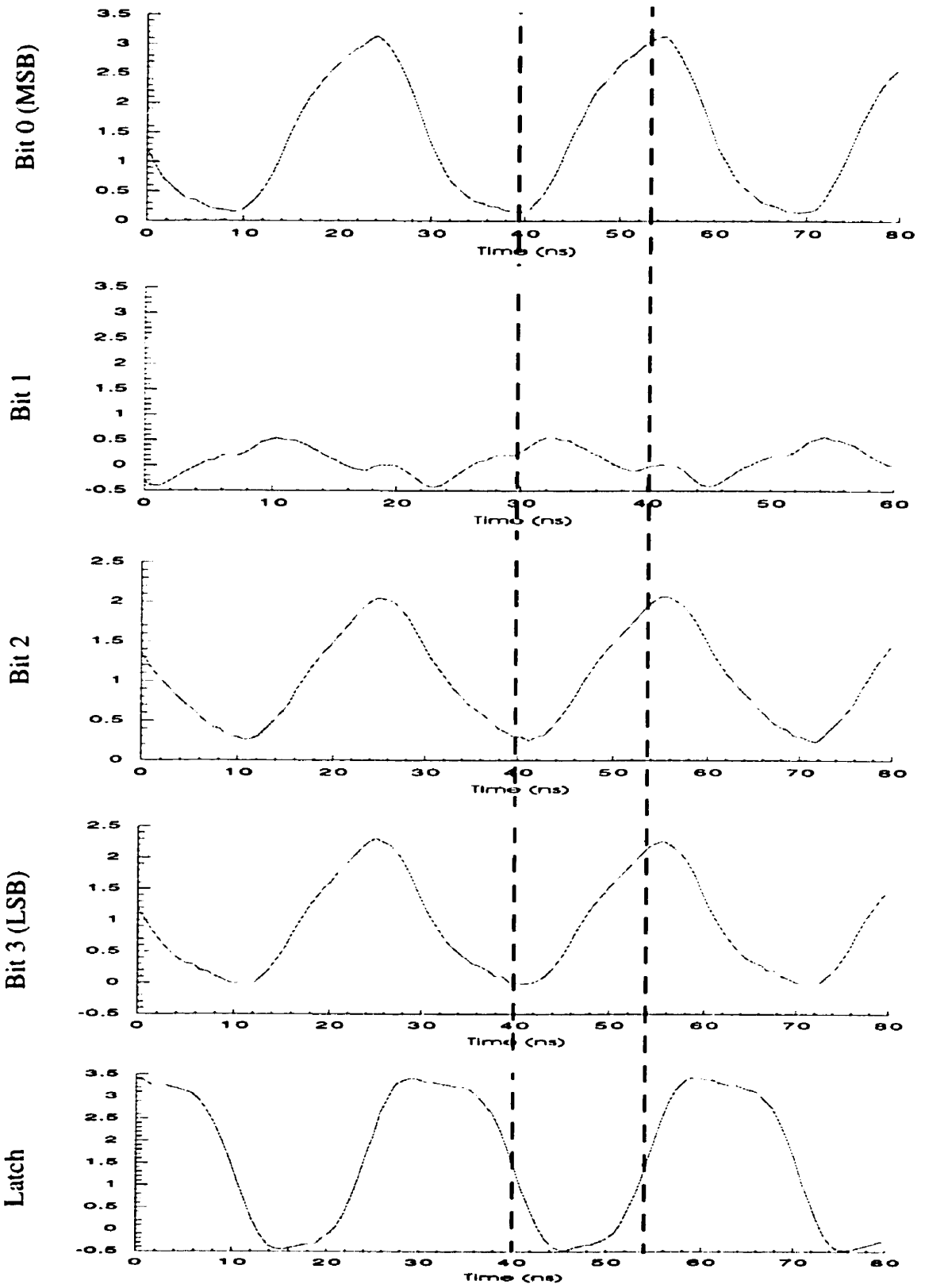


Figure 8.7: Measured output of ADC-2 with Vin = 2.6V at latch frequency = 33MHz.

Chapter 9

Conclusions and Future Research

The design for manufacturability of analog integrated circuits was investigated in this thesis. Building blocks for high-speed data converters, namely a latched comparator and a 4bit flash ADC, were used as test vehicles for exploring factors that can affect the manufacturability of an analog circuit. The main area of interest was to examine the effects of layout design style on the performance of a latched comparator and a flash ADC. Three layout design styles were created for the latched comparator which were subsequently utilized in two layout designs of the flash ADC. All of the layout designs were fabricated in 0.35μm TSMC CMOS technology available through Canadian Microelectronic Corporation. The layout performances were compared through circuit measurement and by HSPICE simulation.

Simulation results of the latched comparator showed a small variation in the resolution for each layout style and a much larger difference in the comparison rate for each layout style. The simulation results indicated that the *full-analog* layout style provided the best operation. When compared with the measurement results, the *full-analog* layout also proved to have the best performance overall. The *partial-analog* layout did exhibit promising performance results. However, there was a large variability in the resolution and decision speed for the *partial-analog* layout indicating that this layout was more susceptible to process variations. The *digital-like analog* layout had fairly reproducible measurement results, yet the resolution was high and the comparison rate was low.

In addition to the comparators, two flash ADCs were designed using the *full-analog* and *digital-like analog* layout styles. The first ADC, labeled ADC-1, used the *full-analog* layout of the comparator and a rectangular resistor string in addition to the digital logic. Measurement of ADC-1 revealed a converter with a 4bit resolution, ± 1 LSB, integral non-linearity and ± 0.5 LSB differential non-linearity. In addition, ADC-1 had a maximum operating frequency of 46MHz. In contrast, ADC-2, which used the *digital-like analog* layout style and an interdigitated resistor string, had ± 2 LSB integral non-linearity, ± 0.25 LSB differential non-linearity and a maximum operating frequency of only 33 MHz.

From the combination of measurement and simulation results, it can be concluded that the performance of minimum geometry latched comparators and a 4bit flash ADCs designed in a digital CMOS process is affected by layout design style. Therefore, layout design style seems to be an important manufacturability factor that must be taken into account for the robust design of minimum geometry analog integrated circuits.

There are several areas of future work to continue this research. First, a larger sample population of fabricated comparators and ADC's is required to precisely determine layout effects on short channel length analog circuits. While the measurement results display performance trends for the various layout styles, there are some anomalies that need to be investigated further.

Secondly, the comparator and flash ADC circuits need to be tested at higher frequencies (>100MHz). The circuits are designed for high speed operation and the simulation results indicate that the circuits could function as high as 160MHz. To fully investigate the affects

of layout on circuit performance, the high speed testing needs to be taken to the next level.

Appendix A

A.1 Schematic of Simulation Configuration

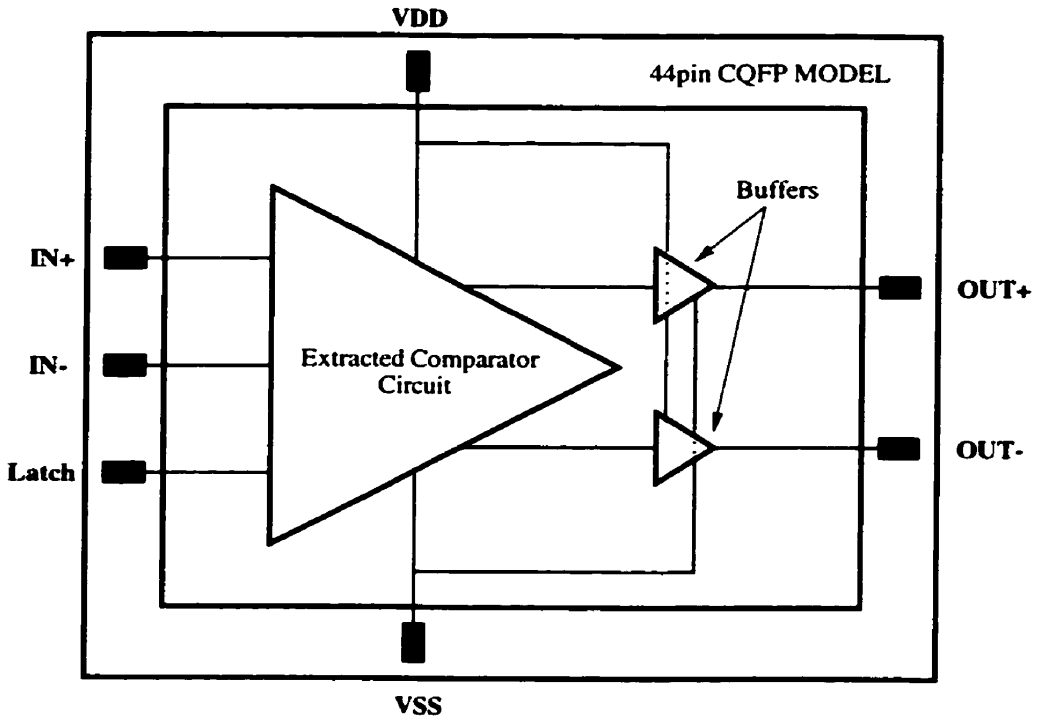


Figure A.1: Schematic of simulation configuration showing the connection of the extracted comparator layout to the extracted buffers and then finally to the model for the 44pin CQFP package.

A.2 Netlist Example for Full Analog Layout

* # FILE NAME: /ENSC/CMC9/ROCKEY/CADENCE/SIMULATION/FULLANALOGPKG/HSPICES/
* schematic/netlist/fullanalogpkg.c.raw
* Netlist output for hspiceS.
* Generated on Jun 14 10:55:21 1999
* global net definitions
.GLOBAL VDD!
* File name: packagesim35_fullanalogpkg_schematic.s.
* Subcircuit for cell: fullanalogpkg.
* Generated for: hspiceS.
* Generated on Jun 14 10:55:25 1999.

```
* bondwire Instance I8 = hspiceS device XI8
* Instance of Lib: package, Cell: bondwire, View: schematic
XI8 NET108 NET80 BONDWIRE_1
* bondwire Instance I7 = hspiceS device XI7
* Instance of Lib: package, Cell: bondwire, View: schematic
XI7 NET109 NET82 BONDWIRE_1
* bondwire Instance I6 = hspiceS device XI6
* Instance of Lib: package, Cell: bondwire, View: schematic
XI6 NET110 NET84 BONDWIRE_1
* bondwire Instance I5 = hspiceS device XI5
* Instance of Lib: package, Cell: bondwire, View: schematic
XI5 NET112 NET86 BONDWIRE_1
* bondwire Instance I4 = hspiceS device XI4
* Instance of Lib: package, Cell: bondwire, View: schematic
XI4 NET106 NET88 BONDWIRE_1
* bondwire Instance I3 = hspiceS device XI3
* Instance of Lib: package, Cell: bondwire, View: schematic
XI3 NET107 NET90 BONDWIRE_1
* bondwire Instance I2 = hspiceS device XI2
* Instance of Lib: package, Cell: bondwire, View: schematic
XI2 NET105 NET92 BONDWIRE_1
* fullanalog Instance I1 = hspiceS device XI1
* Instance of Lib: packagesim35, Cell: fullanalog, View: extracted
XI1 NET86 80 92 NET84 NET90 NET88 NET82 FULLANALOG_G1
* bnr28_44_300_quad Instance I0 = hspiceS device XI0
* Instance of Lib: package, Cell: bnr28_44_300_quad, View: schematic
XI0 NET105 NET107 NET106 NET112 NET110 NET109 NET108 OUP VDD! 0 NPUT
R L OUN
+0 SUB1
XI9 80 NET80 VDD! 0 buffer
XI10 92 NET92 VDD! 0 buffer

* File name: package_bondwire_schematic.s.
* Subcircuit for cell: bondwire.
* Generated for: hspiceS.
* Generated on Jun 14 10:55:21 1999.
* terminal mapping: MINUS = MINUS
*                   PLUS = PLUS
* inductor Instance L0 = hspiceS device L0
* resistor Instance R0 = hspiceS device R0
* capacitor Instance C3 = hspiceS device C3
* capacitor Instance C0 = hspiceS device C0
* End of subcircuit definition.
*Model definitions
* File name: packagesim35_fullanalog_extracted.s.
* Subcircuit for cell: fullanalog.
```

```
* Generated for: hspiceS.
* Generated on Jun 14 10:55:22 1999.
* terminal mapping: IN = IN
*                   OUTN = OUTN
*                   OUTP = OUTP
*                   REF = REF
*                   VDD = VDD
*                   VSS = VSS
*                   latch = latch
* End of subcircuit definition.
* File name: package_bnr28_44_300_quad_schematic.s.
* Subcircuit for cell: bnr28_44_300_quad.
* Generated for: hspiceS.
* Generated on Jun 14 10:55:24 1999.
* terminal mapping: B1 = B1
*                   B3 = B3
*                   B4 = B4
*                   B6 = B6
*                   B8 = B8
*                   B9 = B9
*                   B11 = B11
*                   L1 = L1
*                   L3 = L3
*                   L4 = L4
*                   L6 = L6
*                   L8 = L8
*                   L9 = L9
*                   L11 = L11
*                   gnd! = 0
* End of subcircuit definition.
* Include files
* End of Netlist
.SUBCKT BONDWIRE_1 MINUS PLUS
L0 NET12 MINUS  +1.51751463E-09 M=1.0
R0 PLUS NET12  (50E-3) M=1.0 L=25.5E-6 W=4E-6
C3 MINUS 0  +1.12250898E-14 M=1.0 W=5.5E-6 L=5.5E-6
C0 PLUS 0  +1.12250898E-14 M=1.0 W=5.5E-6 L=5.5E-6
.ENDS BONDWIRE_1
.SUBCKT FULLANALOG_G1 IN OUTN OUTP REF VDD VSS LATCH
C18 VDD LATCH  100.598000329555E-18 M=1.0
C20 LATCH VSS  193.358762140191E-18 M=1.0
C22 LATCH 4  373.661993706114E-18 M=1.0
C24 LATCH 6  181.200001229049E-18 M=1.0
C26 VSS 6  709.539965217581E-18 M=1.0
C28 VSS 5  1.4564629884084E-15 M=1.0
C30 VSS OUTN  626.228504443168E-18 M=1.0
```

C32 IN VSS 432.719989524881E-18 M=1.0
C34 REF VSS 478.560009731964E-18 M=1.0
C36 OUTP VSS 581.696964851135E-18 M=1.0
C38 REF 5 301.928229241025E-18 M=1.0
C40 6 7 100.975690997247E-18 M=1.0
C42 5 6 111.85739753917E-18 M=1.0
C44 4 6 368.03668908472E-18 M=1.0
C46 4 5 409.452947375871E-18 M=1.0
C48 3 5 357.622551347127E-18 M=1.0
C50 3 4 113.702936747449E-18 M=1.0
C52 VSS OUTN 223.775013826933E-18 M=1.0
C54 VDD 6 654.700775811292E-18 M=1.0
C56 VDD 5 907.040890523413E-18 M=1.0
C58 OUTP VSS 217.049995742208E-18 M=1.0
C60 VDD 15 117.583115269482E-18 M=1.0
C62 VDD 7 106.761964965843E-18 M=1.0
C64 VDD 6 274.921166052973E-18 M=1.0
C66 VDD 5 313.281144181973E-18 M=1.0
C68 VDD 4 418.572077616231E-18 M=1.0
C70 VDD 3 446.526441276668E-18 M=1.0
C72 VDD 1 114.522388184358E-18 M=1.0
C74 OUTP VDD 108.038284798678E-18 M=1.0
C76 VSS 16 916.750005681315E-18 M=1.0
C78 VSS 15 916.750005681315E-18 M=1.0
C80 VSS 7 1.03313000329345E-15 M=1.0
C82 VSS 6 953.819979101426E-18 M=1.0
C84 VSS 5 588.212501100092E-18 M=1.0
C86 VSS 4 1.90129504615321E-15 M=1.0
C88 VSS 3 1.53218498103586E-15 M=1.0
C90 VSS 2 1.06785496599909E-15 M=1.0
C92 VSS 1 605.829992309594E-18 M=1.0
C94 VSS OUTN 438.125012640429E-18 M=1.0
C96 LATCH VSS 147.707497931446E-18 M=1.0
C98 VDD VSS 4.94786757545369E-15 M=1.0
C100 IN VSS 147.707497931446E-18 M=1.0
C102 REF VSS 147.707497931446E-18 M=1.0
C104 OUTP VSS 438.125012640429E-18 M=1.0
C106 4 7 787.235279914344E-18 M=1.0
C108 3 7 792.801027531633E-18 M=1.0
C110 LATCH 6 113.696160483871E-18 M=1.0
C112 VDD 7 214.645891244773E-18 M=1.0
C114 IN 3 115.234637013881E-18 M=1.0
C116 IN 2 829.991332569813E-18 M=1.0
C118 IN 1 111.380173882731E-18 M=1.0
C120 IN VSS 196.246006289805E-18 M=1.0
C122 REF 4 344.117352156986E-18 M=1.0

C124 REF 3 345.373184380409E-18 M=1.0
C126 REF 1 117.295004953407E-18 M=1.0
C128 REF VSS 198.791035893839E-18 M=1.0
C130 VDD 16 580.25250897827E-18 M=1.0
C132 VDD 15 580.25250897827E-18 M=1.0
C134 VDD 7 6.28950762456525E-15 M=1.0
C136 VDD 6 397.290004239552E-18 M=1.0
C138 VDD 5 397.290004239552E-18 M=1.0
C140 VDD 1 452.699987973172E-18 M=1.0
C142 VSS 16 902.632507549428E-18 M=1.0
C144 VSS 15 902.632507549428E-18 M=1.0
C146 VSS 7 693.629986550626E-18 M=1.0
C148 VSS 6 2.52532497070266E-15 M=1.0
C150 VSS 5 2.33207990950075E-15 M=1.0
C152 VSS 1 5.73286510020051E-15 M=1.0
C154 LATCH VSS 1.50377253136963E-15 M=1.0
C156 IN VSS 7.4126097851534E-15 M=1.0
C158 REF VSS 8.75046020885895E-15 M=1.0
C160 5 6 256.581049860345E-18 M=1.0
C162 REF IN 382.374998118045E-18 M=1.0
C164 6 7 160.009420645564E-18 M=1.0
C166 5 6 311.668314041062E-18 M=1.0
C168 4 7 111.528960513872E-18 M=1.0
C170 4 6 1.28237971829751E-15 M=1.0
C172 3 5 1.13809242029307E-15 M=1.0
C174 3 4 723.351896213747E-18 M=1.0
C176 2 4 1.61134296281385E-15 M=1.0
C178 2 3 1.56362790282912E-15 M=1.0
C180 1 3 136.969475970646E-18 M=1.0
C182 1 2 148.556410233052E-18 M=1.0
C184 OUTN 16 205.2019768087E-18 M=1.0
C186 VSS 16 242.131514813134E-18 M=1.0
C188 VSS 15 236.393025414164E-18 M=1.0
C190 VSS 7 320.843613153737E-18 M=1.0
C192 VSS 6 223.214833881222E-18 M=1.0
C194 VSS 5 521.800882870619E-18 M=1.0
C196 VSS 4 277.161859366036E-18 M=1.0
C198 VSS 3 207.183478039904E-18 M=1.0
C200 VSS 2 1.50138305142543E-15 M=1.0
C202 VSS 1 805.157014770587E-18 M=1.0
C204 VSS OUTN 567.836805916535E-18 M=1.0
C206 VDD 16 579.538513143294E-18 M=1.0
C208 VDD 15 579.538513143294E-18 M=1.0
C210 VDD 7 443.997862640657E-18 M=1.0
C212 VDD 6 198.785728703028E-18 M=1.0
C214 VDD 5 220.152849481567E-18 M=1.0

C216 VDD 4 751.883830465093E-18 M=1.0
C218 VDD 3 848.665603260133E-18 M=1.0
C220 VDD 1 287.517154783575E-18 M=1.0
C222 VDD OUTN 829.583221507914E-18 M=1.0
C224 VDD VSS 2.22980745738337E-15 M=1.0
C226 OUTP 15 205.2019768087E-18 M=1.0
C228 OUTP VSS 562.279581568277E-18 M=1.0
C230 OUTP VDD 829.583221507914E-18 M=1.0
M232 VDD VDD VDD VDD PCH L=349.999993431993E-9 W=1.9999999949509E-6
+AD=999.999996004197E-15 AS=2.49999999001049E-12 PD=999.999997475243E-9
+PS=4.50000015916885E-6 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M234 VDD VDD 1 VDD PCH L=349.999993431993E-9 W=1.99999999495049E-6
+AD=2.57499989213261E-12 AS=999.999996004197E-15 PD=2.64999994215032E-6
+PS=999.999997475243E-9 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M236 1 1 VDD VDD PCH L=349.999993431993E-9 W=1.99999999495049E-6
+AD=999.999996004197E-15 AS=999.999996004197E-15 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M238 VDD VDD 7 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=2.54999992475857E-12 AS=1.4999999940063E-12 PD=4.69999986307812E-6
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M240 7 7 VDD VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M242 VDD 7 4 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M244 4 7 6 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M246 6 7 4 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M248 4 7 6 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M250 6 7 4 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M252 4 7 VDD VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M254 VDD 7 3 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M256 3 7 5 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9

+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M258 5 7 3 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M260 3 7 5 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M262 3 7 VDD VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M264 VDD VDD VDD VDD PCH L=349.999993431993E-9 W=3.0000001061257E-6
+AD=1.4999999940063E-12 AS=2.5749998921326E-12 PD=999.999997475243E-9
+PS=2.64999994215032E-6 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M266 5 7 3 VDD PCH L=349.999993431993E-9 W=3.00000010611257E-6
+AD=1.4999999940063E-12 AS=1.4999999940063E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+3.33333322E-01 NRS=+3.33333322E-01 M=1.0
M268 15 6 VDD VDD PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=2.12500004571903E-12 AS=2.12500004571903E-12 PD=4.20000014855759E-6
+PS=4.20000014855759E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M270 16 5 VDD VDD PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=2.12500004571903E-12 AS=2.12500004571903E-12 PD=4.20000014855759E-6
+PS=4.20000014855759E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M272 OUTP 15 VDD VDD PCH L=349.999993431993E-9 W=6.7500000113796E-6
+AD=5.7374998849169E-12 AS=5.7374998849169E-12 PD=8.44999976834515E-6
+PS=8.44999976834515E-6 NRD=+1.48148148E-01 NRS=+1.48148148E-01 M=1.0
M274 OUTN 16 VDD VDD PCH L=349.999993431993E-9 W=6.7500000113796E-6
+AD=5.7374998849169E-12 AS=5.7374998849169E-12 PD=8.44999976834515E-6
+PS=8.44999976834515E-6 NRD=+1.48148148E-01 NRS=+1.48148148E-01 M=1.0
M276 6 LATCH 5 VSS NCH L=349.999993431993E-9 W=3.99999998990097E-6
+AD=1.99999999200839E-12 AS=1.99999999200839E-12 PD=2.15000000025611E-6
+PS=2.15000000025611E-6 NRD=+2.50000001E-01 NRS=+2.50000001E-01 M=1.0
M278 VSS VSS VSS VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=3.85000017977255E-12 AS=2.99999998801259E-12 PD=4.15000022258027E-6
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M280 VSS 1 2 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M282 2 REF 4 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M284 4 REF 2 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M286 2 IN 3 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0

M288 3 IN 2 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M290 2 REF 4 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M292 4 REF 2 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M294 2 IN 3 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M296 3 IN 2 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M298 2 1 VSS VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M300 VSS 1 1 VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=2.99999998801259E-12 PD=999.999997475243E-9
+PS=999.999997475243E-9 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M302 1 VSS VSS VSS NCH L=349.999993431993E-9 W=6.00000021222513E-6
+AD=2.99999998801259E-12 AS=5.09999849517 15E-12 PD=999.999997475243E-9
+PS=7.70000042393804E-6 NRD=+1.66666661E-01 NRS=+1.66666661E-01 M=1.0
M304 VSS 5 6 VSS NCH L=349.999993431993E-9 W=1.99999999495049E-6
+AD=1.16250000077589E-12 AS=1.99999999200839E-12 PD=1.50000005305628E-6
+PS=2.15000000025611E-6 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M306 5 6 VSS VSS NCH L=349.999993431993E-9 W=1.99999999495049E-6
+AD=1.99999999200839E-12 AS=999.999996004197E-15 PD=2.15000000025611E-6
+PS=999.999997475243E-9 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M308 VSS VSS VSS VSS NCH L=349.999993431993E-9 W=1.99999999495049E-6
+AD=999.999996004197E-15 AS=3.85000017977255E-12 PD=999.999997475243E-9
+PS=4.15000022258027E-6 NRD=+5.00000001E-01 NRS=+5.00000001E-01 M=1.0
M310 VSS VSS 7 VSS NCH L=349.999993431993E-9 W=1.50000005305628E-6
+AD=1.27499996237929E-12 AS=749.999997003148E-15 PD=3.20000003739551E-6
+PS=999.999997475243E-9 NRD=+6.66666643E-01 NRS=+6.66666643E-01 M=1.0
M312 7 7 VSS VSS NCH L=349.999993431993E-9 W=1.50000005305628E-6
+AD=749.999997003148E-15 AS=1.16250000077589E-12 PD=999.999997475243E-9
+PS=1.50000005305628E-6 NRD=+6.66666643E-01 NRS=+6.66666643E-01 M=1.0
M314 15 6 VSS VSS NCH L=349.999993431993E-9 W=999.999997475243E-9
+AD=849.999974919524E-15 AS=849.999974919524E-15 PD=2.70000009550131E-6
+PS=2.70000009550131E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M316 16 5 VSS VSS NCH L=349.999993431993E-9 W=999.999997475243E-9
+AD=849.999974919524E-15 AS=849.999974919524E-15 PD=2.70000009550131E-6
+PS=2.70000009550131E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M318 OUTP 15 VSS VSS NCH L=349.999993431993E-9 W=2.49999993684469E-6

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+AD=2.12500004571903E-12 AS=2.12500004571903E-12 PD=4.20000014855759E-6
+PS=4.20000014855759E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M320 OUTN 16 VSS VSS  NCH  L=349.999993431993E-9 W=2.49999993684469E-6
+AD=2.12500004571903E-12 AS=2.12500004571903E-12 PD=4.20000014855759E-6
+PS=4.20000014855759E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
.ENDS FULLANALOG_G1
.SUBCKT SUB1 B1 B3 B4 B6 B8 B9 B11 L1 L3 L4 L6 L8 L9 L11 0
R6 NET37 L11  2.0 M=1.0 L=25.5E-6 W=4E-6
R5 NET132 L9  2.0 M=1.0 L=25.5E-6 W=4E-6
R0 NET83 L1  1.5 M=1.0 L=25.5E-6 W=4E-6
R2 NET124 L4  3.5 M=1.0 L=25.5E-6 W=4E-6
R1 NET130 L3  2.7 M=1.0 L=25.5E-6 W=4E-6
R3 NET122 L8  3.4 M=1.0 L=25.5E-6 W=4E-6
R4 NET128 L6  2.47 M=1.0 L=25.5E-6 W=4E-6
L13 B8 NET122  5E-9 M=1.0 R=0.0
L12 B3 NET130  5E-9 M=1.0 R=0.0
L0 B1 NET83  5.5E-9 M=1.0 R=0.0
L14 B11 NET37  5.5E-9 M=1.0 R=0.0
L15 B6 NET128  4.65E-9 M=1.0 R=0.0
L2 B4 NET124  5.4E-9 M=1.0 R=0.0
L5 B9 NET132  5.2E-9 M=1.0 R=0.0
C2 B1 B3  70E-15 M=1.0 W=500E-9 L=500E-9
C25 L9 0  350E-15 M=1.0 W=500E-9 L=500E-9
C26 L9 L11  60E-15 M=1.0 W=500E-9 L=500E-9
C27 B11 0  620E-15 M=1.0 W=500E-9 L=500E-9
C28 L11 0  620E-15 M=1.0 W=500E-9 L=500E-9
C17 B6 0  630E-15 M=1.0 W=500E-9 L=500E-9
C23 B9 B11  60E-15 M=1.0 W=500E-9 L=500E-9
C21 B8 B9  160E-15 M=1.0 W=500E-9 L=500E-9
C8 L3 0  300E-15 M=1.0 W=500E-9 L=500E-9
C15 L6 L8  65E-15 M=1.0 W=500E-9 L=500E-9
C0 B1 0  775E-15 M=1.0 W=500E-9 L=500E-9
C7 L3 L4  160E-15 M=1.0 W=500E-9 L=500E-9
C20 L8 0  310E-15 M=1.0 W=500E-9 L=500E-9
C9 B3 B4  160E-15 M=1.0 W=500E-9 L=500E-9
C11 L4 L6  65E-15 M=1.0 W=500E-9 L=500E-9
C12 B4 B6  65E-15 M=1.0 W=500E-9 L=500E-9
C13 L4 0  400E-15 M=1.0 W=500E-9 L=500E-9
C14 B4 0  400E-15 M=1.0 W=500E-9 L=500E-9
C10 B3 0  300E-15 M=1.0 W=500E-9 L=500E-9
C16 B6 B8  65E-15 M=1.0 W=500E-9 L=500E-9
C18 L6 0  630E-15 M=1.0 W=500E-9 L=500E-9
C22 L8 L9  160E-15 M=1.0 W=500E-9 L=500E-9
C24 B9 0  350E-15 M=1.0 W=500E-9 L=500E-9
C19 B8 0  310E-15 M=1.0 W=500E-9 L=500E-9
C6 L1 0  775E-15 M=1.0 W=500E-9 L=500E-9
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C5 L1 L3  70E-15 M=1.0 W=500E-9 L=500E-9
.ENDS SUB1

.SUBCKT BUFFER 4 7 2 3
* # FILE NAME: /ENSC/CMC9/ROCKEY/CADENCE/SIMULATION/BUFFERX4/
HSPICES/
* extracted/netlist/bufferx4.c.raw
* Netlist output for hspiceS.
* Generated on Jun 29 18:53:02 1999
* File name: SFMR4_bufferx4_extracted.S.
* Subcircuit for cell: bufferx4.
* Generated for: hspiceS.
* Generated on Jun 29 18:53:03 1999.
* pcapacitor Instance +30 = hspiceS device C9
C9 1 2  211.622407139549E-18 M=1.0
* pcapacitor Instance +31 = hspiceS device C11
C11 1 3  179.599850112567E-18 M=1.0
* pcapacitor Instance +32 = hspiceS device C13
C13 1 4  299.682665488515E-18 M=1.0
* pcapacitor Instance +33 = hspiceS device C15
C15 1 5  464.262411219667E-18 M=1.0
* pcapacitor Instance +34 = hspiceS device C17
C17 2 5  340.71317968153E-18 M=1.0
* pcapacitor Instance +35 = hspiceS device C19
C19 2 6  781.117055057208E-18 M=1.0
* pcapacitor Instance +36 = hspiceS device C21
C21 2 7  1.22614265983046E-15 M=1.0
* pcapacitor Instance +37 = hspiceS device C23
C23 3 5  285.339671304201E-18 M=1.0
* pcapacitor Instance +38 = hspiceS device C25
C25 3 6  648.404462276996E-18 M=1.0
* pcapacitor Instance +39 = hspiceS device C27
C27 3 7  802.150418384749E-18 M=1.0
* pcapacitor Instance +40 = hspiceS device C29
C29 5 6  982.768388865026E-18 M=1.0
* pcapacitor Instance +41 = hspiceS device C31
C31 6 7  1.99466878188497E-15 M=1.0
* pcapacitor Instance +42 = hspiceS device C33
C33 1 3  1.50689998876913E-15 M=1.0
* pcapacitor Instance +43 = hspiceS device C35
C35 3 4  753.449994384567E-18 M=1.0
* pcapacitor Instance +44 = hspiceS device C37
C37 3 5  3.01379997753827E-15 M=1.0
* pcapacitor Instance +45 = hspiceS device C39
C39 3 6  6.02759995507653E-15 M=1.0
* pcapacitor Instance +46 = hspiceS device C41
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C41 1 2  1.00545002536836E-15 M=1.0
* pcapacitor Instance +47 = hspiceS device C43
C43 2 4  502.725012684182E-18 M=1.0
* pcapacitor Instance +48 = hspiceS device C45
C45 2 5  2.01090005073673E-15 M=1.0
* pcapacitor Instance +49 = hspiceS device C47
C47 2 6  4.02180010147346E-15 M=1.0
* pcapacitor Instance +50 = hspiceS device C49
C49 1 4  208.532894169108E-18 M=1.0
* pcapacitor Instance +51 = hspiceS device C51
C51 1 5  200.533581189688E-18 M=1.0
* pcapacitor Instance +52 = hspiceS device C53
C53 5 6  607.814114048978E-18 M=1.0
* pcapacitor Instance +53 = hspiceS device C55
C55 6 7  1.4251699914468E-15 M=1.0
* pcapacitor Instance +54 = hspiceS device C57
C57 2 6  178.526990240641E-18 M=1.0
* pcapacitor Instance +55 = hspiceS device C59
C59 2 7  390.256480873569E-18 M=1.0
* pcapacitor Instance +56 = hspiceS device C61
C61 1 3  389.639999706645E-18 M=1.0
* pcapacitor Instance +57 = hspiceS device C63
C63 2 3  1.16958997571143E-15 M=1.0
* pcapacitor Instance +58 = hspiceS device C65
C65 3 5  487.239979858953E-18 M=1.0
* pcapacitor Instance +59 = hspiceS device C67
C67 3 6  913.779990530886E-18 M=1.0
* pcapacitor Instance +60 = hspiceS device C69
C69 3 7  1.09847997160266E-15 M=1.0
* pcapacitor Instance +61 = hspiceS device C71
C71 1 2  132.78645670019E-18 M=1.0
* pcapacitor Instance +62 = hspiceS device C73
C73 2 5  207.872777570511E-18 M=1.0
* pcapacitor Instance +63 = hspiceS device C75
C75 2 6  398.067448136234E-18 M=1.0
* pcapacitor Instance +64 = hspiceS device C77
C77 2 7  313.340304139382E-18 M=1.0
*Model definitions
* Include files
* End of Netlist
M79 2 4 1 2  PCH  L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=2.12500004571903E-12 PD=1.0500000371394E-6
+PS=4.20000014855759E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M81 5 1 2 2  PCH  L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.31250002186056E-12 PD=1.0500000371394E-6
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
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M83 2 1 5 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M85 6 5 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M87 2 5 6 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M89 6 5 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M91 2 5 6 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M93 7 6 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M95 2 6 7 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M97 7 6 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M99 2 6 7 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M101 7 6 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M103 2 6 7 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.24999999500525E-12 AS=1.31250002186056E-12 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M105 7 6 2 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=1.31250002186056E-12 AS=1.24999999500525E-12 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M107 2 6 7 2 PCH L=349.999993431993E-9 W=2.49999993684469E-6
+AD=2.12500004571903E-12 AS=1.31250002186056E-12 PD=4.20000014855759E-6
+PS=1.0500000371394E-6 NRD=+4.00000010E-01 NRS=+4.00000010E-01 M=1.0
M109 3 4 1 3 NCH L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=849.999974919524E-15 PD=1.0500000371394E-6
+PS=2.70000009550131E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M111 5 1 3 3 NCH L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=525.000019586247E-15 PD=1.0500000371394E-6
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M113 3 1 5 3 NCH L=349.999993431993E-9 W=999.999997475243E-9

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+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M115 6 5 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M117 3 5 6 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M119 6 5 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M121 3 5 6 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M123 7 6 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M125 3 6 7 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M127 7 6 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M129 3 6 7 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M131 7 6 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M133 3 6 7 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=499.999998002099E-15 AS=525.000019586247E-15 PD=999.999997475243E-9
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M135 7 6 3 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=525.000019586247E-15 AS=499.999998002099E-15 PD=1.0500000371394E-6
+PS=999.999997475243E-9 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
M137 3 6 7 3  NCH  L=349.999993431993E-9 W=999.999997475243E-9
+AD=900.000018087821E-15 AS=525.000019586247E-15 PD=2.79999994745594E-6
+PS=1.0500000371394E-6 NRD=+1.00000000E+00 NRS=+1.00000000E+00 M=1.0
.ENDS $ BUFFER$

.TEMP   27.0000

****Load Capacitors****
Cl1 OUP 0 1p
Cl2 OUN 0 1p
```

```
****Power Supplies*****
VD VDD! 0 DC 3.3

****Inputs****
Vl L 0 pulse (3.3 0 0.0n 3n 3n 7n 20n)

Vref R 0 pwl 2n 1.0, 15n 1.0, 20n 1.0
Vin NPUT 0 pwl 2n 1.2, 20n 1.2

****Trans Analysis****
.TRAN 0.05n 20n
.PRINT V(L) V(OUP) V(OUN)
.options post nomod nopage brief nowarn ingold=1
.op

*.LIB '/amd/cygnus/ensc/cmc9/rockey/hspice/models/CMOSP35/logp3v5v.l' TT
*.lib '/net/cmc9/rockey/hspice/models/CMOSP35/logp3v5v.l' FF
*.lib '/net/cmc9/rockey/hspice/models/CMOSP35/logp3v5v.l' FS
*.lib '/net/cmc9/rockey/hspice/models/CMOSP35/logp3v5v.l' SF
.lib '/net/cmc9/rockey/hspice/models/CMOSP35/logp3v5v.l' SS
.END
```

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