MONOLITHIC INDUCTORS

FOR SILICON RADIO FREQUENCY INTEGRATED CIRCUITS

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

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Monolithic Inductors
for Silicon Radio Frequency Integrated Circuits

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Master of Applied Science
Department of Electrical and Computer Engineering
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1999

ABSTRACT

A novel parameter extraction technique is applied to the modeling of rectangular spiral inductors and validated with measurements and simulations. To enhance the inductor quality (Q) factor, a differentially excited symmetric inductor is used. Compared with a single-ended configuration, the differential structure offers a higher Q-factor over a wider range of frequencies. Application of the symmetric inductor model is demonstrated using two oscillator designs in which a differentially excited symmetric inductor is compared with conventional spiral inductors. The symmetric inductor improves the overall circuit performance and saves chip area.

ACKNOWLEDGMENTS

I wish to thank Professor John R. Long for introducing me to the world of RF electronics, and in particular, to microstrip structures on semiconductors, where electromagnetics is coupled to electronics. He helped me in many ways throughout the course of my studies. I appreciate his patience and his sympathy.

I am also grateful to my fellow graduate students and friends: Ramesh Abhari (Yes, you will be a professor!), Xidong Wu (for his Eastern philosophy and insightful comments), Leesa and Karam Noujeim, Micah Stickel, Sebastian Magierowski, Dickson Cheung, Ali Sheikholeslami, Vincent Gaudet, and Mr. Gerald Dubois who plays a special role in the group. I also appreciate having met many interesting people, as well as the Massey College community, who made my stay in Toronto much more enjoyable. I shall not forget Behzad, a soulful musician.

Je tiens à remercier mes parents et toute ma famille pour leur appui au cours de ces deux dernières années. Karima a aussi tenu une place que je ne saurai décrire. Nilda et Alexandra demeureront mes amies pour toujours.

I am thankful for the NSERC Graduate Scholarship which gave me the opportunity to come to the University of Toronto.

Finally, I wish to thank Prof. Christopher W. Trueman who knows how to guide his students in their research.

"One is capable, if one is knowledgeable Knowledge *(danesh)* rejuvenates the soul"

Ferdowsi (940 - 1020 A.D.)

FOREWORD

This thesis is mainly aimed at RF circuit engineers. For those who do not have any previous knowledge of how a spiral inductor works, the mechanisms behind microstrip structures on a silicon substrate are presented. Chapter 2 explains the fundamentals of a single microstrip line. Even though the world of electromagnetics may seem to exist in a realm other than microelectronics, this is in fact not the case. One must realize that electromagnetics (EM) is the basis of everything electrical. I have tried to explain the interactions of the EM fields in semiconductors as simply as possible. I deliberately did not give any formulations regarding EM fields for they might confuse the reader. Since circuit engineers love circuits, equivalent circuit models for monolthic inductors are given, which should simplify their application in a circuit simulator.

For those who already have some experience with spiral inductors, Chapters 3 and 4 present new approaches to the modeling and optimization techniques for inductors. Differential circuits may seem very familiar, but the designer rarely considers the EM mechanism behind a differentially excited microstrip line or a different inductor configuration. Chapter 4 gives an example of a cross-coupled oscillator where two inductor configurations are compared.

A bibliography is given for those interested in further investigation. It is not an extensive list, but it covers the major references.

Mina Danesh
September 1998

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LIST OF SYMBOLS

C_o	overall capacitance due to the overlap and interwinding capacitances
C_{ox}	oxide capacitance from the strip line to the SiO_2/Si interface
C_{si}	silicon capacitance from the strip line to the ground plane without the oxide layer
δ	skin depth
ε_r	relative permittivity
ε_{reff}	effective relative permittivity/dielectric constant
f	frequency of operation
f_{peak}	frequency at which the Q peaks
f_{sr}	self-resonant frequency
G	inner gap between opposing groups of coupled strips of a spiral inductor
l	total length of a microstrip line structure
λ_g	guided wavelength
L	transmission line inductance
N	number of turns of a spiral inductor
OD	outer turn dimension of a rectangular spiral inductor
Q	inductor quality factor
Q_{peak}	maximum inductor quality inductor value
r	resistance due to a strip conductor
R_{si}	dissipation due to the conductive silicon
ρ_S	metal sheet resistivity
ρ_{si}	silicon resistivity
s	spacing between two microstrip lines
t_M	upper metal thickness
t_{Mox}	oxide thickness between upper and lower metals used for an underpass
t_{ox}	oxide layer thickness
t_{si}	silicon layer thickness
w	microstrip line width
w_u	microstrip line width for an underpass

Chapter 1

INTRODUCTION

1.1 Silicon Radio Frequency Integrated Circuits

With the emergence of wireless communications systems such as personal communication services (PCS), wireless local area networks (WLANs), satellite communications, and the global positioning system (GPS), interest has focussed on radio frequency integrated circuits (RF ICs). In the 1980s, military applications drove the development of monolithic microwave integrated circuits (MMICs) forward by fabricating passive and active circuit elements on the same semi-insulating gallium arsenide (GaAs) substrate [1]. Compared with discrete and hybrid designs [2], the monolithic approach offers low cost, improved reliability and reproducibility, small size and weight, broadband performance, and circuit design flexibility. Disadvantages of the monolithic approach, such as process difficulties, low yields and poor performance, have largely been overcome [3]. The consumer electronics market favours silicon (Si) technology for its lower cost, higher yield, and the potential for mixing analog and digital circuits. Silicon bipolar and BiCMOS technologies now offer performance comparable with GaAs in the low GHz frequency range [1].

Figure 1 shows the RF front-end architecture for a heterodyne transceiver, where filters, amplifiers, mixers, and oscillators are needed for implementation. Inductors can be used in all stages of an RF IC for the input/output matching circuitry and passive filters. They are also convenient loads for active circuits, such as amplifiers and mixers, where lower noise performance and 1-3 V supply voltages may be realized. However, implementing the inductor on-chip has been regarded as an impractical task because of excessive substrate capacitance and substantial resistive losses due to metallization and the conductive silicon substrate, which degrade the overall performance of the circuit. Hence, all inductive components were integrated off-chip until, in 1990, planar inductors were demonstrated to be feasible in modern silicon technologies [4].

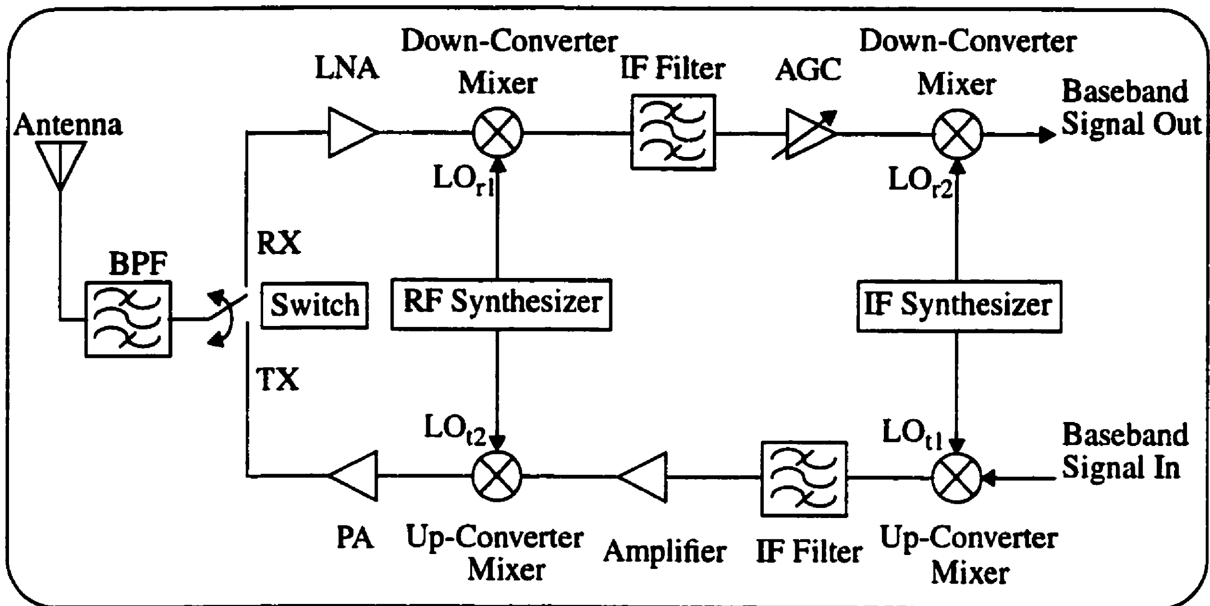


Fig. 1. RF front-end: heterodyne transceiver architecture.

Compared with GaAs, on-chip inductors on silicon substrates have poorer performance simply because of the low substrate resistivity. Depending on the dopant concentration of the silicon wafer, the silicon resistivity can be as low as 0.01 Ω-cm for CMOS and 1 Ω-cm for bipolar, as illustrated in Fig. 2. For current bipolar and BiCMOS technologies, the typical silicon resistivity ranges from 1 to 10 Ω-cm, and for CMOS, from 0.01 to 1 Ω-cm.

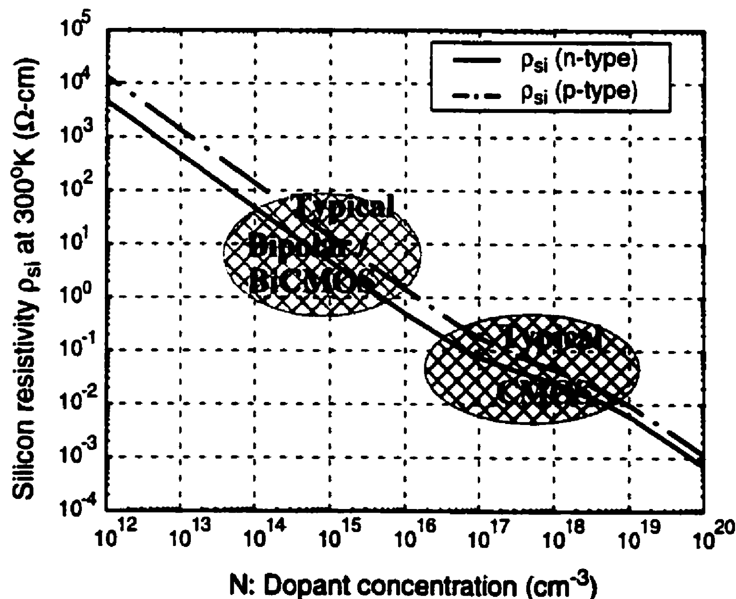


Fig. 2. Silicon resistivity as a function of doping concentrations of n-type (phosphorus) and p-type (boron) [5].

1.2 Microwave Monolithic Inductors

Passive inductors are implemented with high characteristic impedance microstrip lines fabricated on an insulating (SiO_2) layer that lies on top of a silicon substrate and lower ground plane, as shown in Fig. 3. The typical range of values for each parameter is indicated. The silicon resistivity ρ_{si} must be accounted for in transmission line losses, whereas the oxide conductivity is on the order of 10^{-13} S/m, and hence is considered negligible. Because of finite ρ_{si} and narrow strip width, design guidelines for MMIC structures are not found in the literature, contrary to established design guidelines for MICs [6, 7, 8, 9] for which the fields are in the quasi-TEM (transverse electromagnetic) mode [10]. This will be considered in Chapter 2.

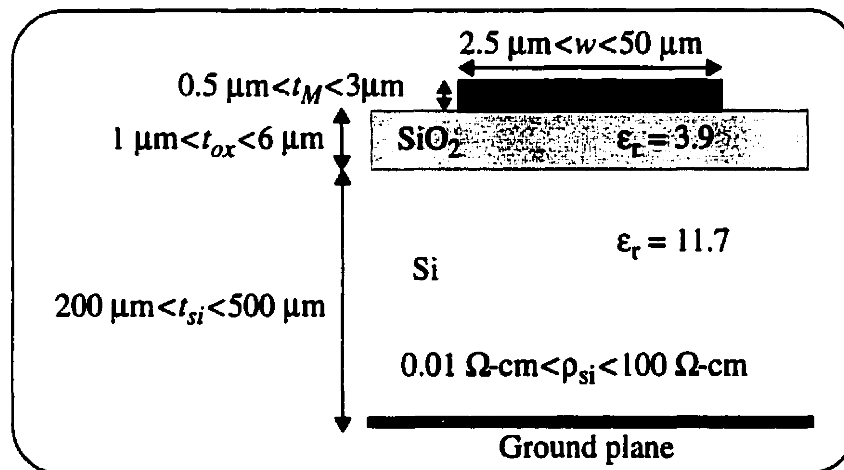


Fig. 3. Microstrip line on silicon with a typical range of parameter values.

Figure 4 shows some planar inductor designs. The single microstrip line, meander, and single loop inductors provide inductances up to 0.5 nH and are seldom used. The meander inductor is designed to conserve chip area, but a better approach is to wind the microstrip line in a spiral, as shown in Fig. 4 (d), (e), and (f). Mutual coupling resulting from the closely spaced lines adds to the self-inductance of the transmission line, increasing the overall inductance. However, because of practical restrictions in the mask making process, the circular shape is implemented as an octogonal or a hexagonal spiral. Typically, inductances up to 20 nH are realized on-chip with spiral configurations. The rectangular spiral is the most

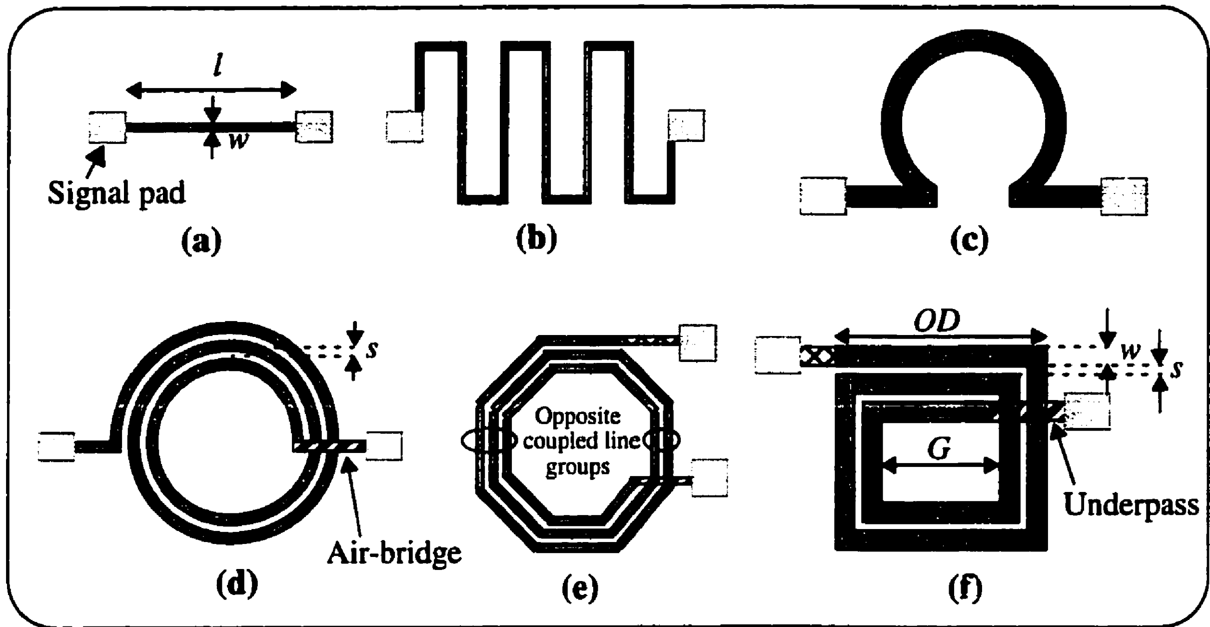


Fig. 4. Monolithic inductor configurations: **(a)** Microstrip line, **(b)** Meander line, **(c)** Single loop, **(d)** Circular spiral, **(e)** Octogonal spiral, **(f)** Rectangular spiral.

commonly used design due to its layout simplicity, however, higher losses are obtained compared with a circular layout, i.e., for equal inductances, as high as a 10% increase in the metallization loss results [11]. Its parameters include the outer dimension *OD*, the strip width *w*, the spacing between lines *s*, the number of turns N, and the gap between opposing groups of coupled lines *G*. The inner turn is connected to the outer circuitry by an underpass, routed via a lower level metal, or an air-bridge.

A coil or solenoid is the most familiar inductive component; thus the design of a planar spiral inductor may seem odd at first. Figure 5 illustrates the magnetic field lines for a coil, a planar solenoid, and the rectangular spiral. Closely spaced windings of the coil provide flux linkages on the top and bottom windings, and the flux lines pass through the middle of the coil. The same idea applies to the planar solenoid, but this design is not suitable for monolithic integration [12]. For the rectangular spiral, groups of coupled lines are located on the same plane, and the flux lines pass through the substrate layers, which results in greater inductance values compared with the planar solenoid.

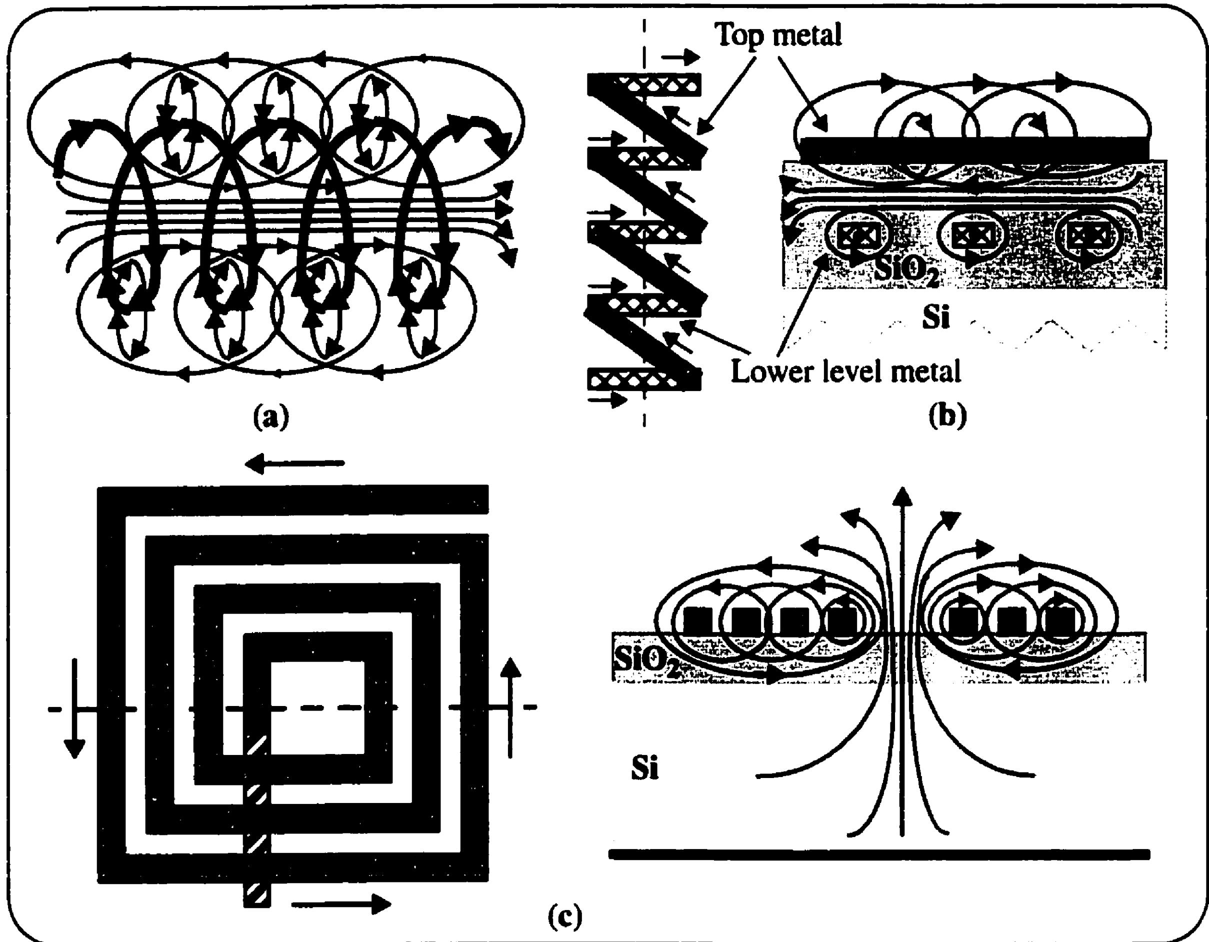


Fig. 5. Magnetic field lines for (a) an air coil, (b) a planar solenoid, and (c) a planar rectangular spiral inductor.

1.3 Purpose and Organization of this Thesis

The purpose of this thesis is to study the behavior of microstrip line structures on silicon in order to model monolithic inductors as equivalent electrical circtuits and to design higher quality inductors for enhancing the performance of RF circuits. Chapter 2 provides an in-depth analysis of propagation issues for Si MMIC technology. This introduces the RF engineer to the design considerations for microstrip elements on a silicon substrate. Illustrations of various line parameters as a function of silicon resistivity and frequency will be presented to support theoretical predictions. A lumped element model is proposed for the single microstrip line, which is compared with numerical simulation results from commercial electromagnetic simulators.

Chapter 3 focusses on the modeling of spiral inductors in silicon technologies. A new inductor model and lumped element parameter extraction technique, based on the single microstrip line case, is compared with experimental and simulated results.

Present monolithic inductors can achieve a maximum Q-factor of 10, posing a limitation for narrowband circuits. Various Q enhancement and chip area reduction techniques have been proposed in the literature, as described in Chapter 4. A closer look at differential symmetric circuits that integrate spiral inductors leads to a differentially excited inductor instead of a single-ended layout where one end of the port is grounded. The differential configuration provides a higher Q (up to a 50% increase in the peak Q) by lowering the substrate parasitics which degrade the inductor performance without altering the fabrication process. A symmetric inductor structure is proposed that is suitable for differential circuits. A model for the symmetric inductor is also presented. Measured and simulated inductor Q-factors agree to within 10%. To demonstrate the advantages and improvement in performance associated with a differential excitation of a symmetric inductor versus single-ended conventional asymmetric spiral inductors, the performance of single-ended and differential Colpitts oscillators at 2 GHz are compared.

Chapter 2

SILICON MICROSTRIP STRUCTURE CHARACTERISTICS

The first section of this chapter introduces the electromagnetic theory behind a microstrip line on a silicon substrate for which different propagation modes are defined. Lumped pi-type equivalent circuits for single and coupled microstrip lines are reviewed. The last section of this chapter will show how the propagation modes can be related to a lumped element equivalent circuit.

2.1 Wave Propagation Modes

Studies of propagation on a microstrip line on a SiO_2/Si substrate were first analyzed using a parallel-plate waveguide model [10, 13]. By observing the associated loss for various values of silicon resistivities and frequency ranges, three specific regimes were identified, each associated with a different propagation mode, as illustrated in Fig. 6 for the electric field distribution.

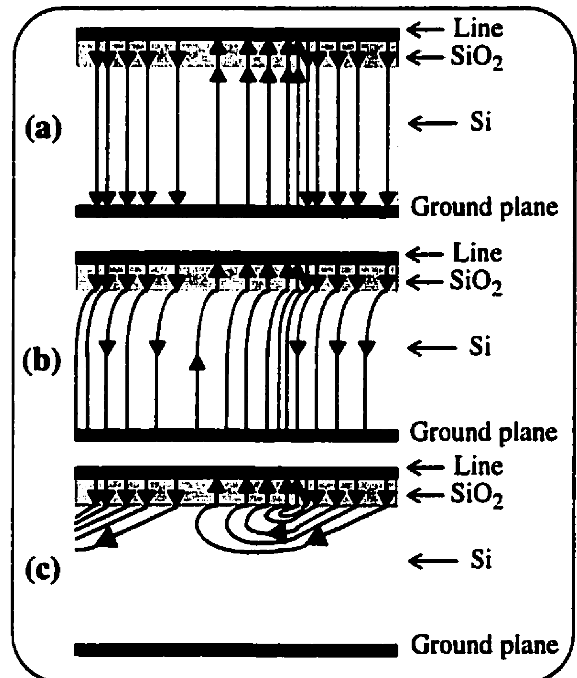


Fig. 6. Electrtic field distribution of **(a)** quasi-TEM, **(b)** slow-wave, and **(c)** skin-effect modes [10].

In Fig. 7, these three regimes are shown in a resistivity-frequency mode chart for typical oxide and silicon thicknesses. The regimes are defined as follows:

1) When the product of frequency and silicon resistivity is high, the silicon substrate acts as a dielectric with a small dielectric loss tangent; the fundamental mode is close to the TEM mode and is therefore called a quasi-TEM mode. Its frequency range is defined for

$$f \geq \frac{1.5}{2\pi\rho_{si}\varepsilon_{si}} \text{ (Hz)} \tag{1}$$

2) When the product of frequency and silicon resistivity is moderate, a surface wave propagates along the transmission line at the SiO_2/Si interface with a propagation velocity smaller than in the previous case. This is the slow-wave mode for which

$$f \le \frac{0.3}{\left(\frac{1}{f_s} + \frac{2}{3f_\delta}\right)} \text{ (Hz)} \tag{2}$$

where $f_s = \frac{t_{ox}}{2\pi t_{si}\varepsilon_{si}\rho_{si}}$ (Hz) and $f_\delta = \frac{\rho_{si}}{\pi\mu_o(t_{si})^2}$ (Hz);

3) When the product of frequency and silicon conductivity is large enough so that the silicon substrate acts as a lossy conductor or an imperfect ground plane, the fundamental mode is called the skin-effect mode (where the skin depth $\delta = \sqrt{\rho_{si}/(\pi\mu_o f)}$ (m) is on the order of the silicon thickness, i. e., δ = 160 μm at 1 GHz for ρ_{si} = 0.01 Ω-cm). This mode appears for

$$f \ge 0.4 f_\delta \text{ (Hz).} \tag{3}$$

Standard Si bipolar processes range in the slow-wave, transition region of the slow-wave to quasi-TEM, and quasi-TEM modes in the 1 to 10 GHz frequency range. CMOS RF applications are well within the slow-wave and even in the skin-effect regimes.

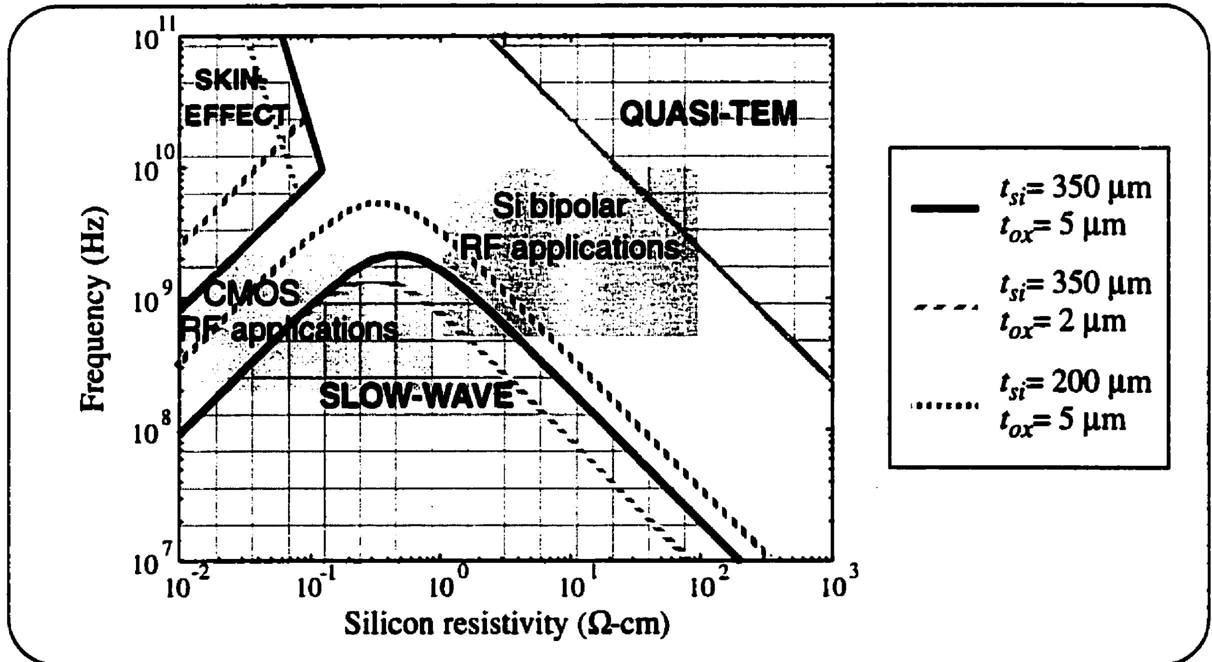


Fig. 7. Resistivity-frequency mode chart for various oxide/silicon thicknesses.

To show how the silicon substrate behaves with respect to its resistivity, vertical electric field maps for different ρ_{si} are given at 1 GHz. These field maps were extracted by a 3D finite-difference time-domain (FDTD) method [14]. The structure consists of a perfect electric conductor (PEC) sheet of 100 μm width, oxide and silicon thicknesses of 5 μm and 200 μm, respectively, and a 195 μm height of free space, as shown in Fig. 8. For a 0.1 Ω-cm resistivity (Fig. 9), the silicon substrate is a lossy conductor, and most of the fields are in the oxide and air. A slow surface wave propagates along the line. The fields penetrate into the silicon as its resistivity increases, as shown in Fig. 10, where the propagation mode lies in the transition region between the slow-wave to quasi-TEM modes and in Fig. 11, where it is in the quasi-TEM mode. Fringing fields are also present at the edges of the strip.

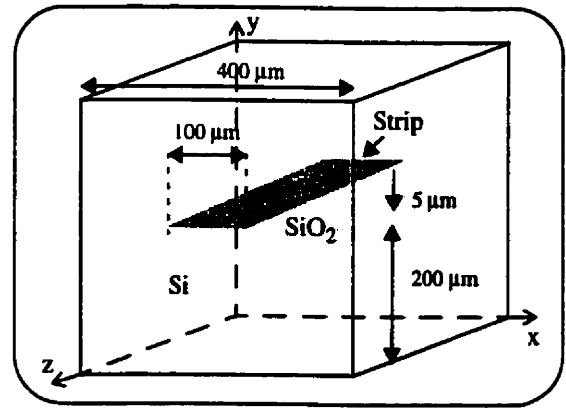


Fig. 8. FDTD space for a 100 μm strip line.

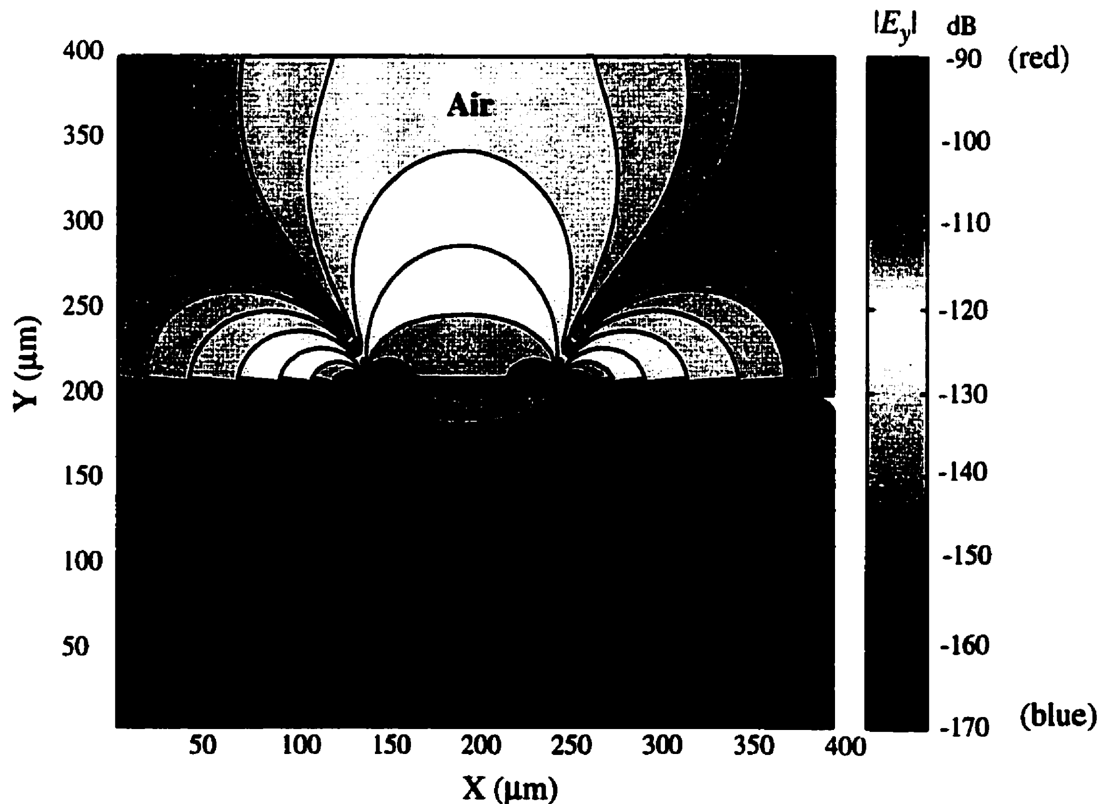


Fig. 9. Unnormalized vertical electric field for $\rho_{si} = 0.1$ Ω-cm.

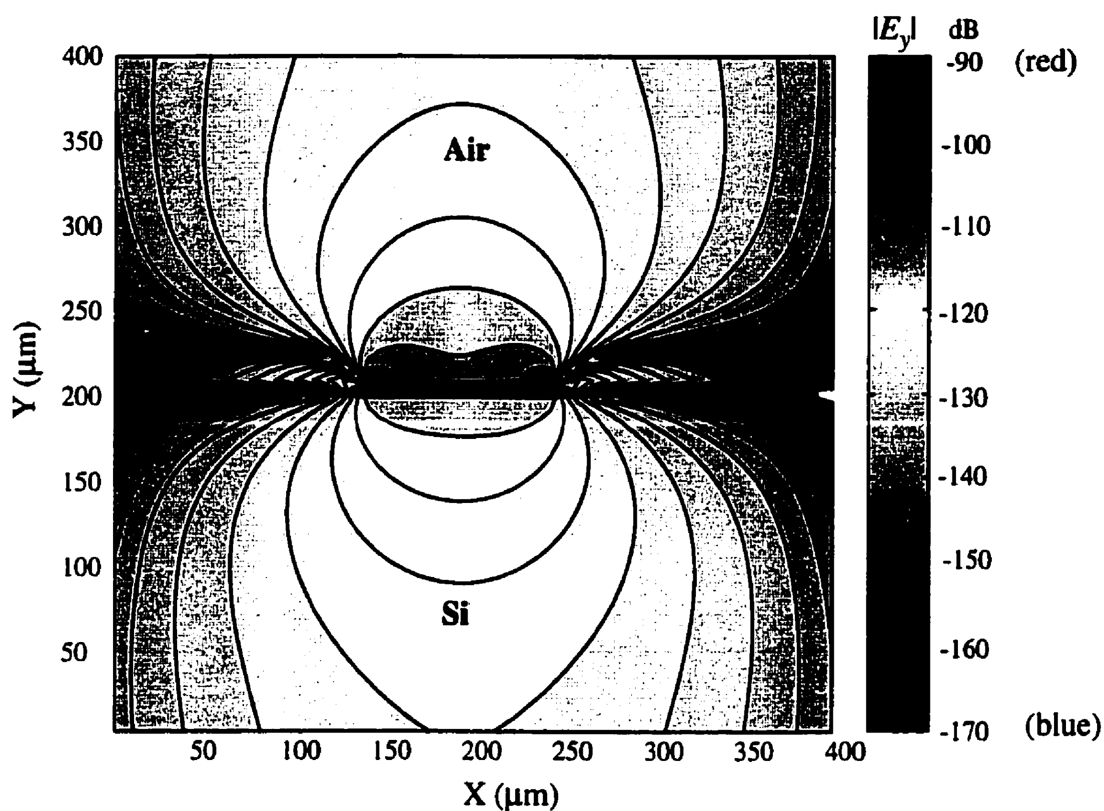


Fig. 10. Unnormalized vertical electric field for ρ_{si} = 10 Ω-cm.

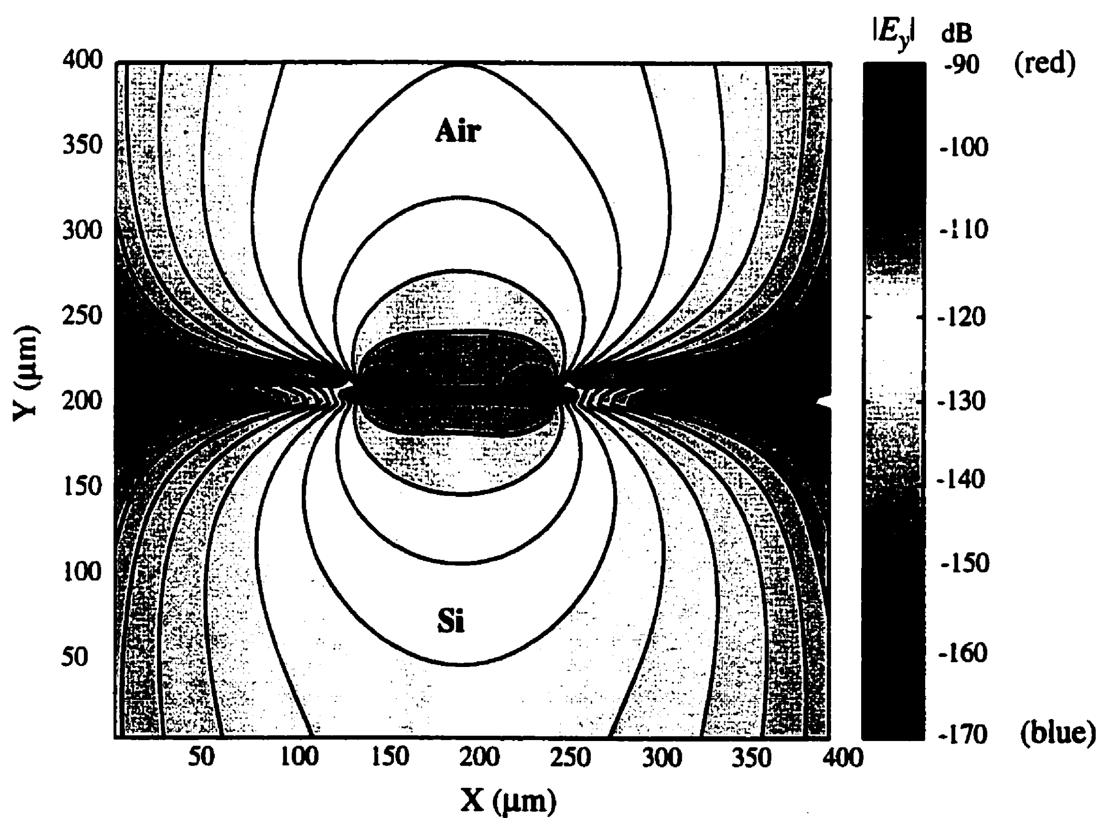


Fig. 11. Unnormalized vertical electric field for ρ_{si} = 10 kΩ-cm.

A two-dimensional numerical simulation using the spectral domain approach (SDA) [15, 16, 17] was used to extract the power in different layers, as shown in Fig. 12, for a single line and two coupled microstrip lines of 10 μm width and 5 μm spacing. (The SDA is a less computer intensive numerical method appropriate for 2D planar strip lines in a shielded box. Convergence was achieved with a box length of 10 mm with 4000 points and an air height greater than 1 mm.) All subsequent figures will show results for a 5 μm thick oxide and a 350 μm silicon layer. In the skin-effect mode, most of the fields penetrate the oxide layer and only slightly penetrate the silicon because of its high loss tangent (> 100 at 1 GHz). For the slow-wave regime, most of the active power is still in the oxide, but the rest is dissipated in the silicon by a conduction current. A large amount of reactive power is exchanged between substrate layers because of the movement of charges at the SiO_2/Si interface [10]. Due to this energy transfer, a slower propagation velocity results. In the quasi-TEM regime, for a single microstrip line and evenly excited coupled lines, most of the energy is transmitted in the silicon substrate (as compared with the oxide) [10]. More electric field lines pass through the

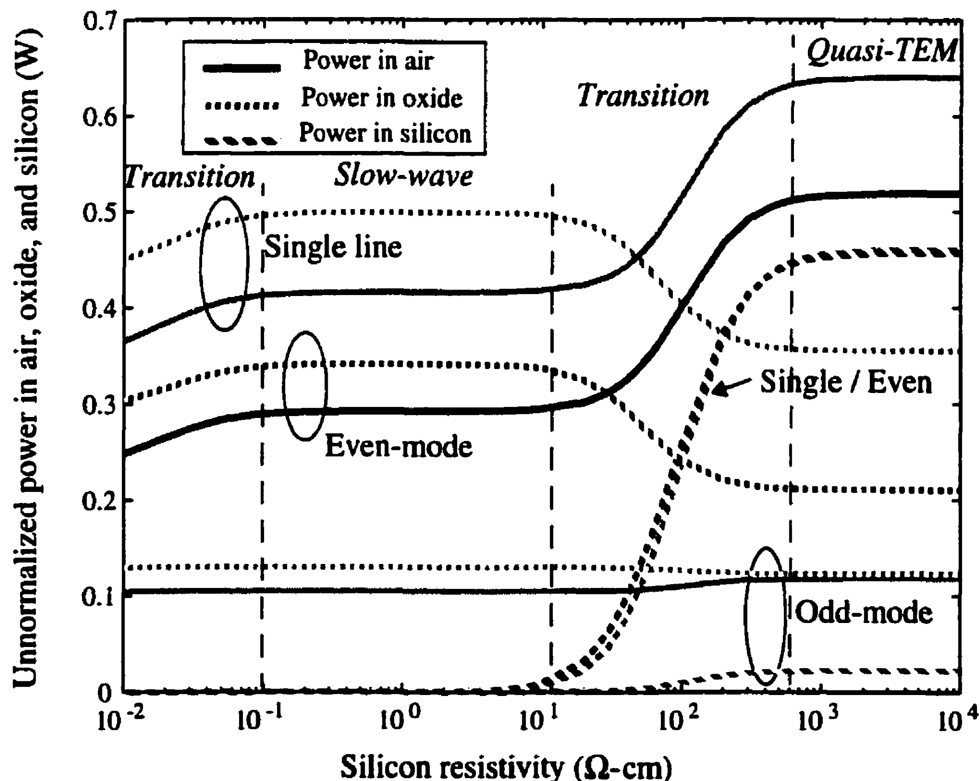


Fig. 12. Unnormalized power in air, oxide and silicon for a single line, and even-mode and odd-mode excitations of two coupled microstrip lines (w = 10 μm, s = 5 μm) at 1 GHz.

conductive layer in the even-mode than in the single line case, whereas in the odd-mode, a substantial portion of the electric field is concentrated between the two strips [18, 19].

Figure 13 illustrates the slow-wave and quasi-TEM regimes for the range of silicon resistivities and frequencies of interest for RF ICs, given the effective dielectric constant ε_{reff} value of a 10 μm wide single microstrip line. As previously defined, a slow-wave propagates for certain silicon resistivity and frequency ranges, which results in higher effective dielectric constants. The quasi-TEM effective dielectric constant is around 5 (region shown in blue), while its value increases to reach a constant (11.6) in the slow-wave regime.

Figure 14 shows the transmission line parameters for single and coupled microstrip lines at a frequency of 1 GHz using the SDA method. Decreasing the line width causes less of the field to be contained in the lossy silicon substrate than in the oxide and the air, which reduces the value of the effective dielectric constant in the slow-wave region. This is also observed for an odd-mode excitation. Hence, as the width increases, the skin-effect is more

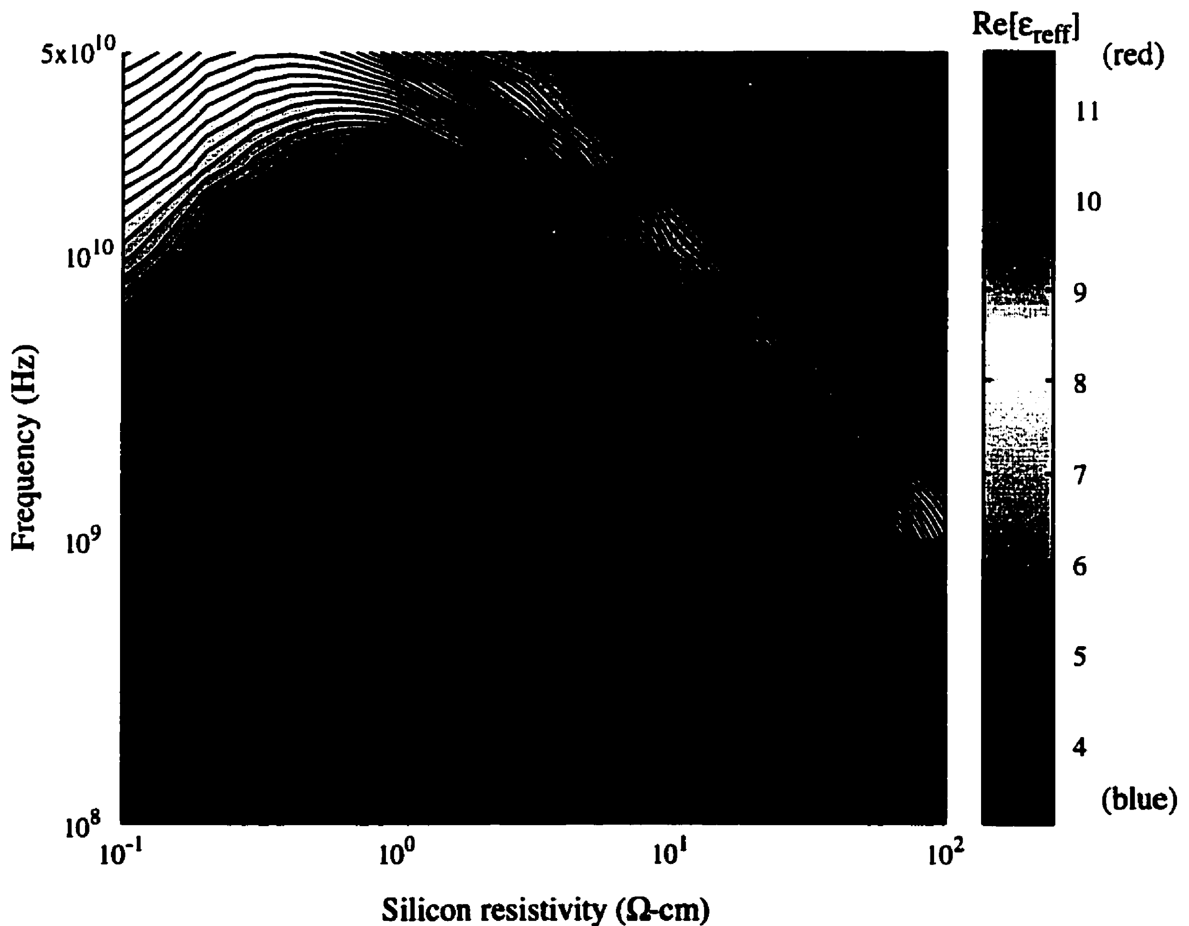


Fig. 13. Resistivity-frequency mode chart for Re[ε_{reff}] for a 10 μm wide microstrip line.

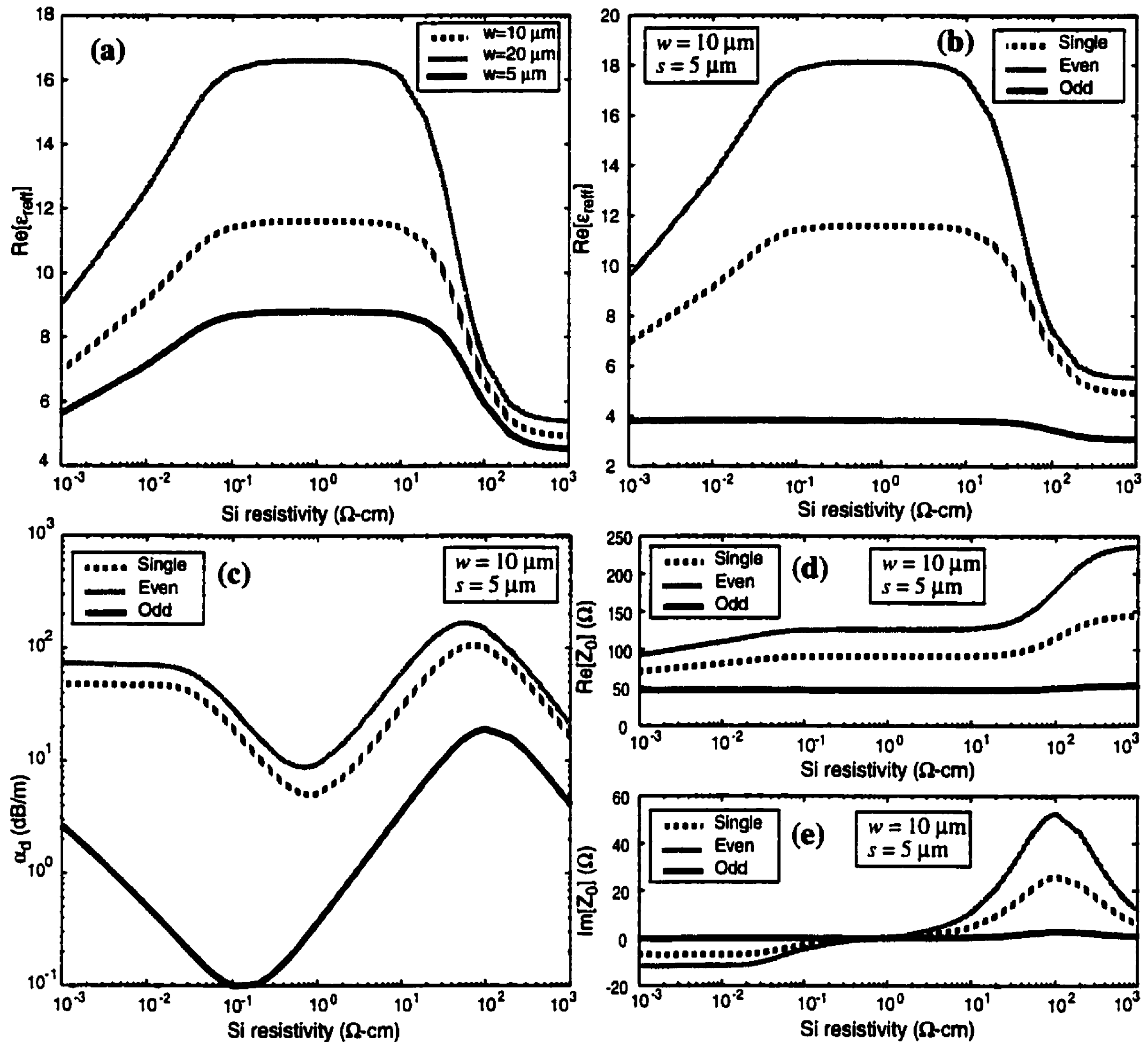


Fig. 14. **(a)** Re[ε_{reff}] for three different line widths. **(b)** Re[ε_{reff}] for a 10 μm single line and coupled lines with 5 μm spacing. **(c)** Attenuation constant for single and coupled lines. **(d)** Real part and **(e)** imaginary part of the characteristic impedance for single and coupled lines.

pronounced and its region comes into effect earlier in terms of ρ_{Si}. In the skin-effect regime, the silicon substrate acts as a lossy conductor, therefore reducing the effective height of the microstrip line from the actual ground plane. These arguments are further strengthened by the attenuation constant graph (Fig. 14 (c)). Attenuation is minimum in the slow-wave regime, and maxima occur for transitions from quasi-TEM to slow-wave and from slow-wave to the skin-effect regime. The highest attenuation is obtained at the transition to the quasi-TEM mode because of the dominant displacement current in silicon [10], and in the skin-effect region where the attenuation is constant. Both effective dielectric constant and characteristic

impedance are constant in the slow-wave regime. The real part of the characteristic impedance follows the curves of the power flow in air, as shown in Fig. 12, whereas the reactive component is similar to the reactive power in the silicon layer.

For typical RF applications, it has been shown that due to the silicon resistivity value and frequency of operation, the slow-wave propagation mode and transitions between quasi-TEM and skin-effect modes are excited. This demonstrates the importance of the process chosen for the design of monolithic inductors. The influences of these propagation modes will be described throughout this chapter.

2.2 Lumped Circuit Modeling

For RF design, representation of microstrip lines by an equivalent circuit is needed in circuit simulators. Physical/electrical behaviours of monolithic inductors are translated into lumped element equivalent circuit models. The microstrip line is the simplest physical layout for a planar inductor for which an equivalent circuit is determined. This single microstrip line circuit model can also be applied to spiral inductors which consist of groups of coupled strips.

2.2.1 Single Microstrip Line Modeling

The electrical behaviour of a transmission line can be approximated over a range of frequencies by a lumped element equivalent circuit model. For a microstrip transmission line fabricated in silicon technology, an appropriate equivalent circuit is shown in Fig. 15, where L is the inductance of the line, and r is the series resistance mainly due to conductor losses. It is a frequency dependent element which accounts for the edge, proximity, and skin effects [20] on the current flow, and for the conductive silicon substrate [10], due to the current flow parallel to the strip current that is induced in the substrate. Induced eddy currents are attributed to the proximity effect [21]. The shunt parasitics result from a combination of capacitances, involving the insulating layer of silicon dioxide (C_{ox}), the underlying substrate (C_{si}) and its dissipation (R_{si}) [10]. For an electrically short microstrip line where $l < \lambda_g/10$, a single π-section equivalent circuit (Fig. 15) is sufficient, whereas for a longer line, a distributed model should be used.

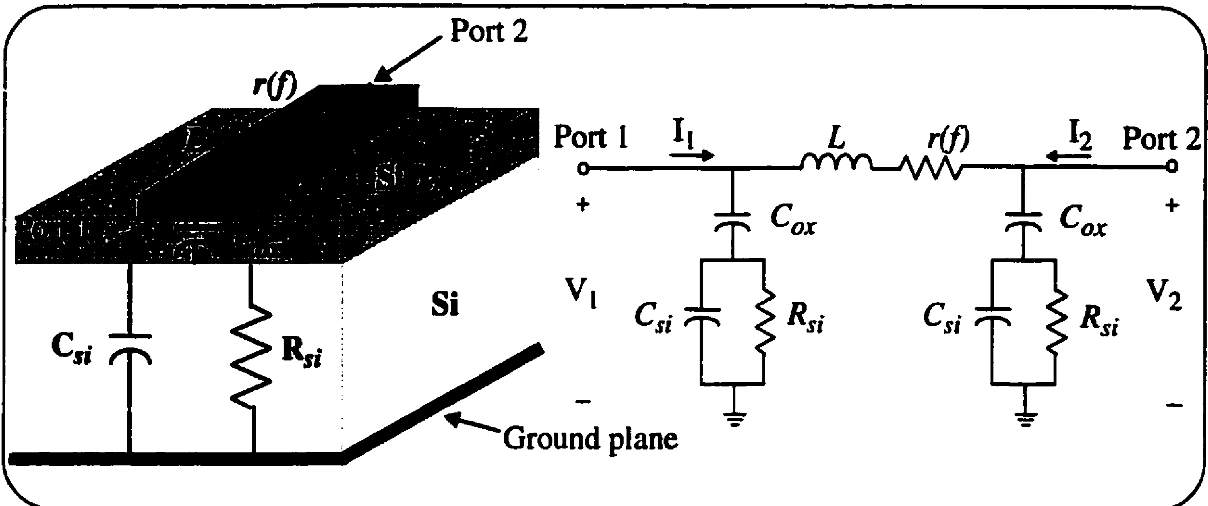


Fig. 15. Microstrip line equivalent circuit.

2.2.2 Spiral Inductor Modeling

A spiral inductor consists of groups of coupled microstrip lines. Modeling the spiral requires knowledge of the currents flowing on the conductor. The current is a time varying component and flows continuously along the spiral. Currents on the same group of coupled strips flow in the same direction, which results in an even-mode excitation for the adjacent strips, as shown in Fig. 16 (a). This holds when the total length of the spiral is less than a quarter of the guided wavelength (where the inductor is self-resonant) and there is a negligible phase shift in the signal voltage or current. Currents on opposing groups of coupled strips flow

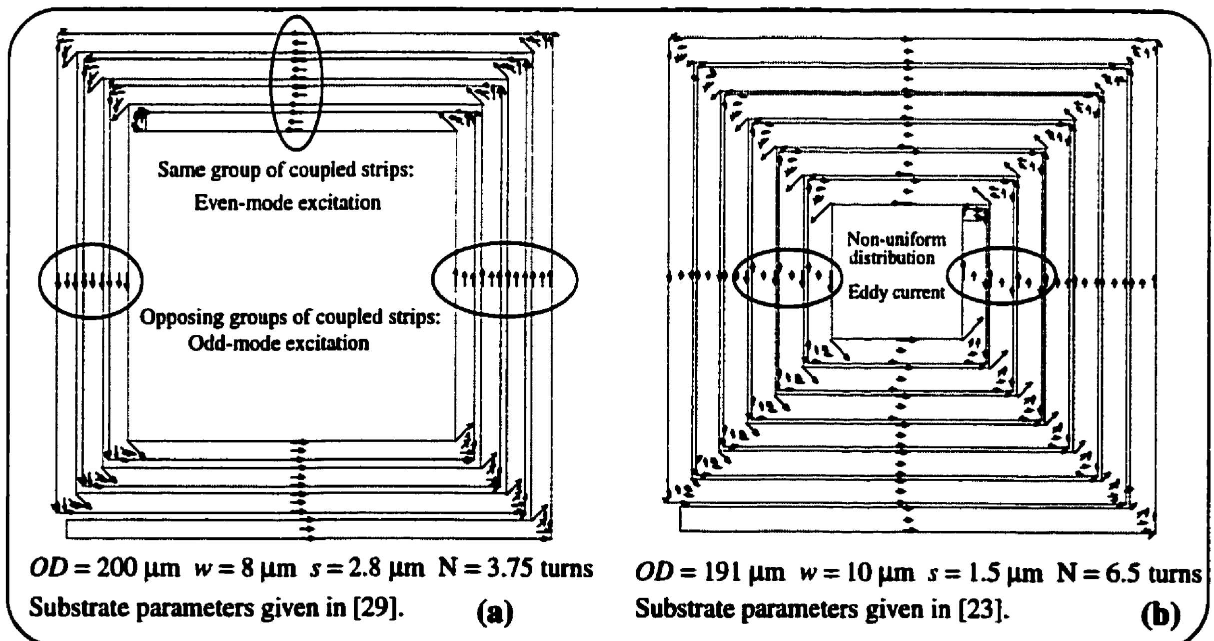


Fig. 16. Surface current flow for spiral inductors of **(a)** 3.75 turns and **(b)** 6.5 turns at 1 GHz.

in different directions, as in Fig. 16 (a), and hence, the odd-mode is excited. Also, the effect of the air-bridge or underpass can disturb the current distribution on the upper metal layer of the spiral, depending on the separation between the two metal layers [22]. As shown in Fig. 16 (b), decreasing the inner gap of the spiral causes a non-uniform current distribution. This current crowding effect is due to induced eddy currents on adjacent strips in the same group and in inner turns, which degrades the total inductance and increases the series resistance [23, 24].

Figure 17 illustrates the electromagnetic field lines and how they influence the transmission line parameters for both odd and even-modes. In the latter case, both currents on adjacent strips flow in the same direction, which results in a positive mutual inductive coupling K_e, thereby increasing the total inductance. For silicon MMICs, K_e typically ranges from 0.5 to 0.8 [21]. Only the electric fields from the strips to the ground plane are present. Therefore, tighter spacing increases the inductance and decreases the substrate capacitance because of reduced electric fringing field lines. For an odd-mode excitation, currents flow in the opposite direction, which results in electric field lines between the strips through the air, oxide and silicon layers. Moreover, negative mutual inductive coupling K_0 degrades the total inductance. Hence, for a spiral inductor, a substantial gap ($G > 5w$) must separate opposing groups of coupled strips [24, 25]. In conclusion, a spiral inductor can have excitations of

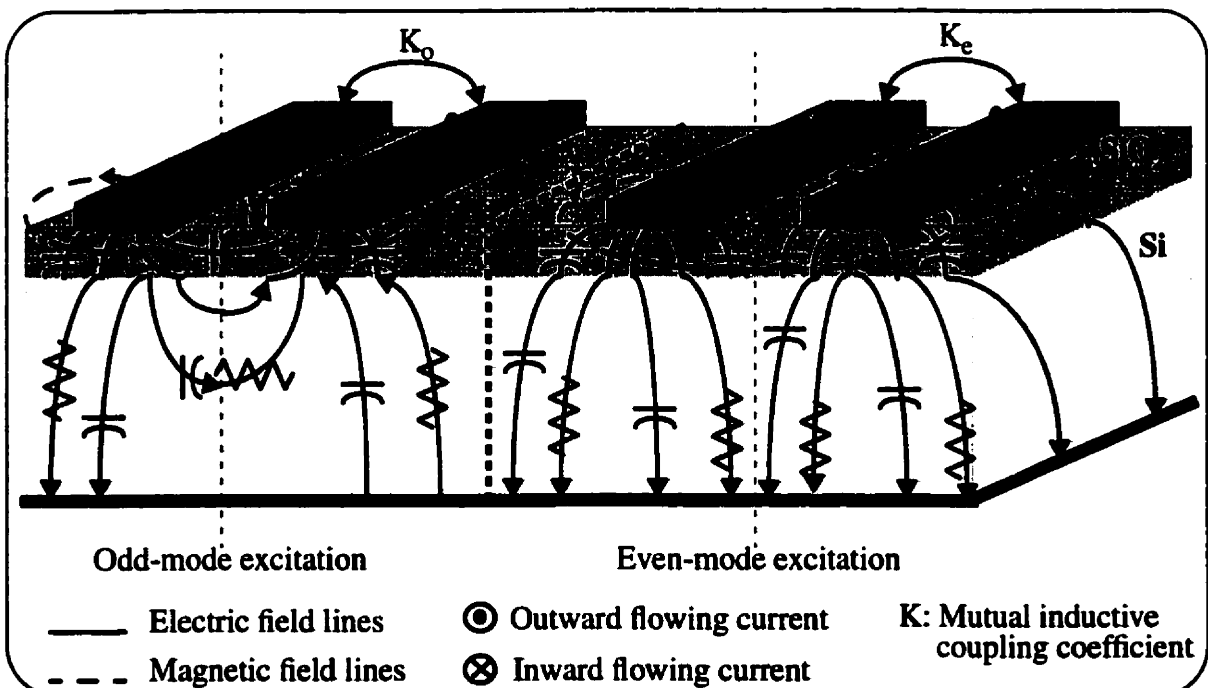


Fig. 17. Electromagnetic field lines and line parameters for two coupled lines for odd- and even-mode excitations.

mixed modes, making it difficult to understand and model.

The spiral inductor can be considered to be a series of electrically short microstrip lines (Fig. 18) connected by mutual inductive coupling coefficients, interwinding (line-to-line) capacitances, and added parasitics due to the bends (considered negligible: C_{bend} < 1 fF and L_{bend} < ~ 0.05 nH [26]) [25, 27]. Added capacitance due to the overlap between the turns of the spiral and the center-tap underpass or cross-over should also be taken into account. A more common representation of a spiral inductor is a compact model, shown in Fig. 19, which is derived from a single microstrip line equivalent circuit. Here, L and r represent the total inductance and resistance of the inductor, respectively. Shunt parasitics model the outer winding at Port 1, and the inner winding at Port 2. Using a conventional spiral inductor results in an asymmetry in the layout, which is represented by two sets of substrate parasitic values [25]. C_o represents the overall line-to-line capacitance resulting from the combination of interwinding and overlap capacitances.

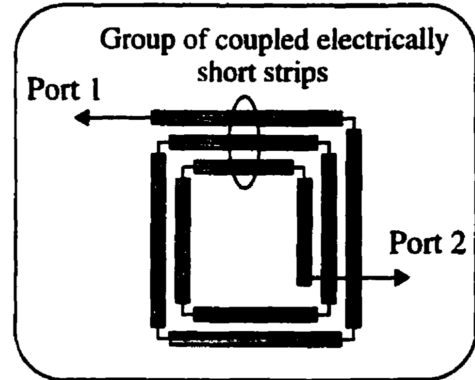


Fig. 18. Simplified spiral inductor layout.

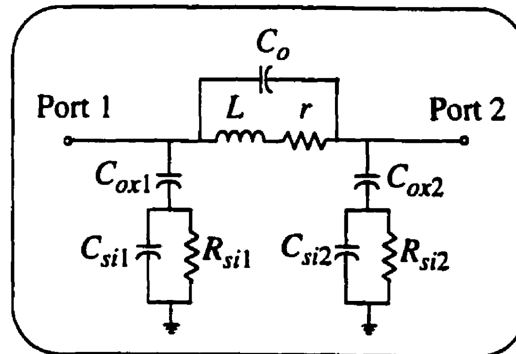


Fig. 19. Compact lumped element inductor model.

2.3 Inductor Quality-Factor

The performance of an inductor is measured by its quality-factor (Q). It is defined as the ratio of the energy stored to the total dissipation per cycle for a sinusoidal excitation [28]:

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy lost per cycle}} = \omega \cdot \frac{\text{energy stored}}{\text{average power loss}}. \quad (4)$$

From a circuit point of view, other interpretations of Q can be used, such as those from the -3 dB bandwidth at the angular resonant frequency (ω_o) or the rate of change of the phase shift at resonance, defined as follows:

$$Q = \frac{\omega_o}{\Delta\omega_{3dB}} \quad (5)$$

$$Q = \frac{\omega_o}{2} \cdot \left.\frac{d\phi}{d\omega}\right|_{\omega_o} . \quad (6)$$

For the case of an inductor, only the energy stored in the magnetic field is considered, whereas energy stored in the electric field, due to parasitic capacitances, counteracts the inductive energy.

For a series L-r circuit connected as a one-port, the Q-factor is defined as

$$Q = \frac{\omega L}{\mathrm{Re}[Z_{in}]} = \frac{\omega L}{r} \quad (7)$$

and for a parallel L_p-r_p circuit,

$$Q = \frac{1}{\mathrm{Re}[Y_{in}] \cdot \omega L_p} = \frac{r_p}{\omega L_p} \quad (8)$$

valid until the inductor's first self-resonance, where Z_{in} is the input impedance and Y_{in} is the input admittance of the one-port structure. A resonance occurs when the peak magnetic energy equals the peak electric energy or $X_L = -X_C$, where C is the total circuit capacitance, and the resonant frequency is

$$f_{sr} = 1/(2\pi\sqrt{L \cdot C}) \text{ (Hz)}. \quad (9)$$

In this case and beyond the self-resonant frequency, no net magnetic energy is available.

Closed-form expressions approximating the monolithic inductor Q-factor are given by Yue and Wong [29] by considering the circuit in Fig. 20, where C_p and R_p replace the substrate shunt parasitics C_{ox1}, C_{si1} and R_{si1} in Fig. 19, and are thus frequency dependent, and by Long and Copeland [25]. Different estimations of Q-factor expression are presented in [30] and [31] and their range of validity is discussed. For this thesis, Eq. (8) is mainly used.

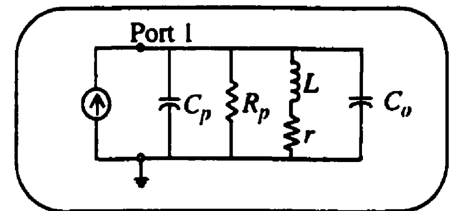


Fig. 20. Equivalent 1-port model.

2.4 Parameter Extraction Methods

This section describes how inductor parameter values for the lumped elements are obtained. The first method does not require knowledge of the physical layout of the structure. From the two-port S-parameters, given either by measurement or simulation, series and shunt impedances for the compact model of Fig. 19 are derived. The second method consists of determining analytically the *L*, *R*, and *C* component values from the physical layout and fabrication process specifications.

2.4.1 Parameter Extraction from Two-Port Results

A microstrip inductor is a two-port element. The S-parameters are determined from simulation or measurement. Series inductance *L* and resistance *r* in the compact model (see Fig. 19), are first derived at low frequencies from the one-port input impedance of the two-port network, as

$$Z_{in} = Z_{11} - \frac{Z_{12} \cdot Z_{21}}{Z_{22}} (\Omega). \tag{10}$$

Figure 21 gives an example of the real and imaginary parts of the input impedance for a spiral inductor derived from measured two-port S-parameters [32]. At low frequencies ($|X_C| >> |X_L|$), *r* is given by $\mathrm{Re}[Z_{in}]$, and *L* as $\mathrm{Im}[Z_{in}]/2\pi f$; they are 7.7 Ω and 7.5 nH, respectively. As the frequency increases, inductive reactance increases and capacitive and resistive parasitics come into play, causing a resonance near 6.3 GHz, when the resistive part of the input impedance is maximum and the reactance is zero. Beyond resonance, the

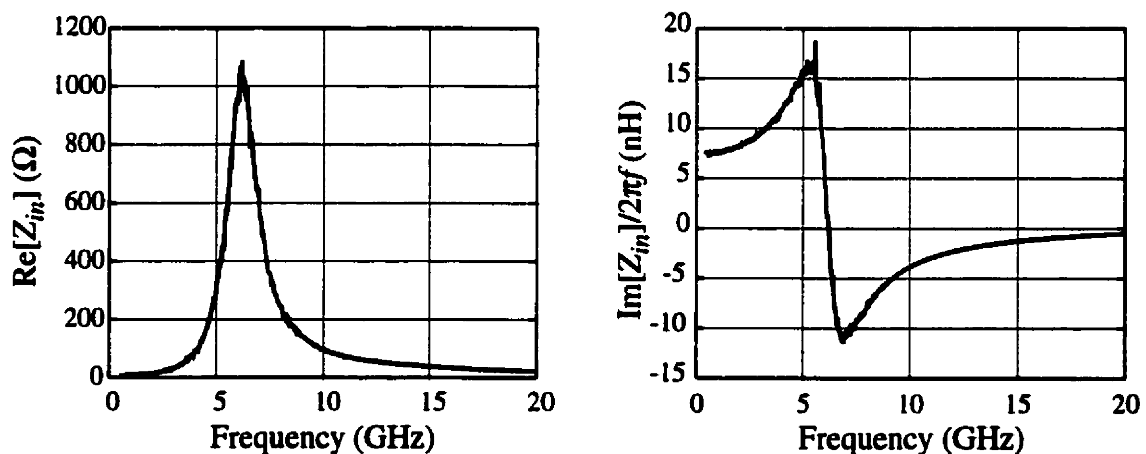


Fig. 21. Measured real and imaginary parts of the input impedance of a spiral indutor (N=5, *w*=8 μm, *s*=2.8 μm).

reactance is negative, and hence the inductor behaves as a capacitor.

Using an optimizer to fit the measured and simulated S-parameters, approximate values for shunt parasitics and overall capacitance C_o are obtained, as shown in Fig. 22. Data for a CMOS 4.25 turn spiral inductor are fit to a frequency range of 0.5 to 6 GHz (below the self-resonance). The shunt parasitic capacitances are lower at the output port (Port 2) because the inner turn of the spiral is shorter in length than the input port (Port 1) outer turn. This results in an asymmetry in the parameter values for C_{ox}, C_{si}, and R_{si} in the model.

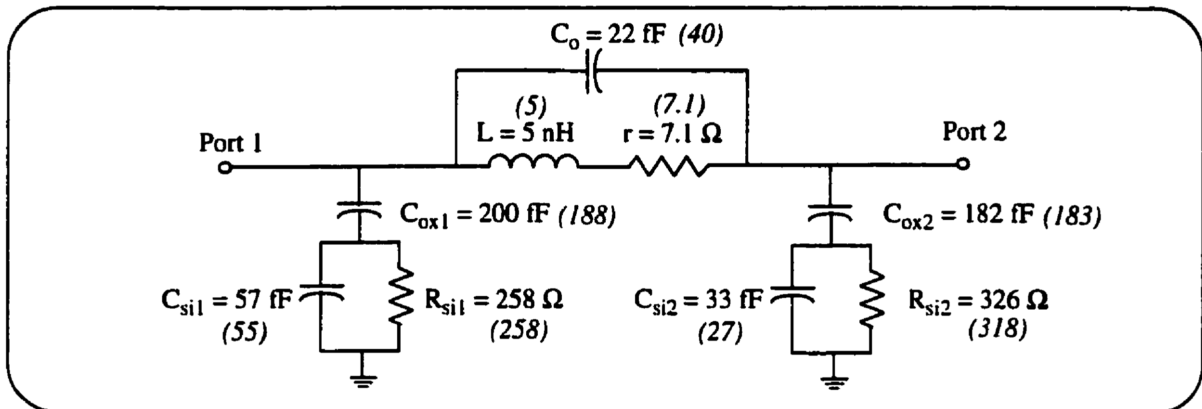


Fig. 22. Parameter fit circuit model for measured and *(simulated)* CMOS spiral inductor.

The previous method involved fitting the parameter values to a set of two-port results over a range of frequencies, using a computer. Another way is to translate the two-port S-parameters to a set of lumped element values at each frequency point. The S-parameters are converted into the propagation constant γ and the characteristic impedance Z_o of a transmission line, from which the lumped elements (L, r, C_p, R_p and C_o) are derived [33]. Figure 23 summarizes the procedure in a flowchart. Simulators such as Sonnet-em provide ε_{reff} and Z_o values for both ports which can be applied to the method of Fig. 23 by directly extracting the component values per unit length.

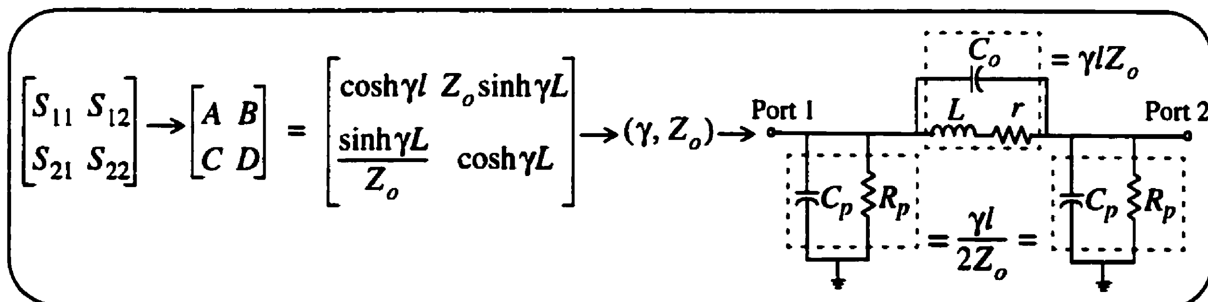


Fig. 23. Parameter extraction by the transmission matrix .

2.4.2 Analytical Parameter Extraction

This section provides a review and a discussion of the extraction methods used for each lumped element parameter, as well as new concepts.

a) Inductance

Inductance is defined as the ratio of the total flux linkages to the current to which they link [34]. Mutual inductance caused by the magnetic interaction between two currents adds to the self-inductance. Depending on the configuration of the conductors, the inductance may be expressed as a function of the physical dimensions, as for an N-turn coil or solenoid [35]. Greenhouse derived the total inductance of a planar rectangular spiral inductor [36], based on the closed-form inductance formulas for the self and mutual inductances of rectangular conductors published by Grover [37], resulting in an inaccuracy of less than 5% compared with measurements. However, these inductances were derived assuming a thick substrate ($w <<$ substrate height) and a static value which does not take into account the electrical length of the spiral inductor at high frequencies where the inductor resonates. Krafesik and Dawson [38] approached these effects by including a negative mutual inductance when the spiral outer diameter is comparable to the ground plane distance, and taking into account propagation delay around the spiral. The experimental results agreed to within 5%.

Other authors have provided crude estimates of the total spiral inductance with closed-form expressions [39, 40]. Mohan *et al.* [41] obtained an inductance expression for square spirals with tight line spacings ($s < w/2$), which does not take into account the metal thickness. It has been shown that the inductance matrix can be obtained from the free space capacitance matrix $[C_{air}]$ with respect to the ground plane, defined as $[L] = \varepsilon_o \mu_o / [C_{air}]$ [42]. This definition can be useful if a full-wave or 2D method gives the capacitive parameter values in matrix form. Full-wave methods can also be applied to obtain more accurate results [31].

However, Greenhouse's method can be easily implemented in a computer program and can be modified for any rectangular layout geometry. Therefore, this method will be used throughout this thesis.

b) Capacitance

The capacitance C relates the ratio of the total charge to the potential difference between two conductors. For two parallel conducting plates, C is expressed as a function of the physical dimensions and substrate layer permittivity as

$$C = \frac{\varepsilon_o \varepsilon_r \cdot w \cdot l}{d} \text{ (F)} \quad (11)$$

where d is the separation between the two plates, assuming a uniform current distribution on the plates and $d << w$ and l [43]. For an MMIC microstrip line where w is on the order of 2 to 50 µm, which is comparable to the oxide thickness, and is much smaller than the silicon thickness (200 - 500 µm), these assumptions are no longer valid.

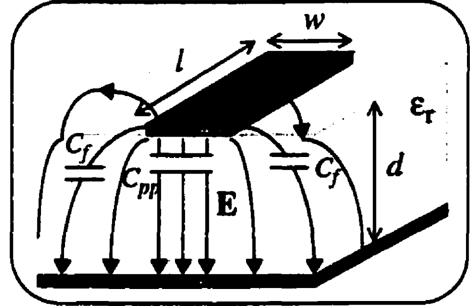


Fig. 24. MMIC microstrip line with electric fields shown.

As illustrated in Fig. 24, electric field lines are non-uniform; hence, fringing fields must be taken into account. The total capacitance consists of C_{pp}, the parallel plate capacitance, and of C_f for the fringing capacitance. To provide accurate capacitance values, several approaches have been used. For computational efficiency, a two-dimensional numerical analysis technique is often used under static assumptions. For coupled strips, odd and even-mode capacitances have been calculated [44, 45], and for multiconductor strips, capacitance matrices are obtained [46, 47, 48, 49, 42]. Basis functions for the non-uniform current, which model the surface edge effect on the charge density for a microstrip line, are used to enhance the accuracy of solutions [50]. Other methods, such as the boundary element method (BEM) [51], the finite-difference (FD) [52], or the measured equation of invariance (MEI) [53], have been used. (The references do not provide an exhaustive list of publications.)

The overlap capacitance for the underpass C_u may be approximated using (11)

$$C_u = \frac{\varepsilon_{ox} w w_u}{t_{Mox}} \text{ (F)} \quad (12)$$

where t_{Mox} is the separating distance between the upper and lower metals used for the underpass in the oxide layer, and w_u is the line width of the underpass. Because of additional

stray fields surrounding the overlap, it has been shown that C_u is increased by a factor of 1.5 to 1.7 relative to (12) [54].

The interwinding capacitance is the line-to-line coupling capacitance between adjacent conducting strips. Due to differences in phase between the voltage on each strip, the interwinding capacitance is the odd-mode coupling capacitance in the substrate and air. Figure 25 illustrates the electric field lines and associated odd-mode capacitances for two coupled microstrip lines. The coupling capacitances, C_{gd} and C_{ga}, can be calculated from the corresponding coupled stripline geometry filled with substrate dielectric and air, respectively [55]. This method is efficient for two coupled microstrip lines only. Mutual coupling capacitances can be also obtained using a full-wave analysis technique for any arbitrary number of conductors [31, 46].

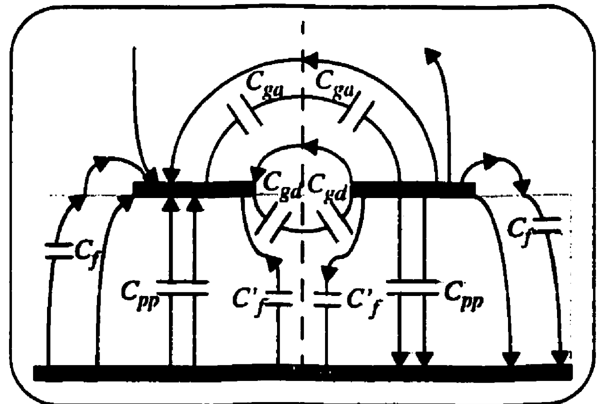


Fig. 25. Odd-mode capacitances for two coupled microstrip lines.

The overall capacitance C_o in shunt with the series inductance and resistance is a combination of interwinding and the underpass or bridge capacitances. This will be discussed in Chapter 3.

c) Resistance

From Ohm's law, the resistance of a conductor is defined to be the ratio of the electromotive force to the strength of the current that it produces. The DC resistance depends on the nature of the conductive material and the temperature [56].

Series Resistance due to Metallization

Resistance is defined by the current distribution on the mictrostrip line, and in the case of silicon, also by the conduction current inside the silicon substrate. Resistance due to the strip line varies with frequency in a complicated manner. They are four factors to take into account: 1) DC, 2) Edge effect, 3) Proximity effect, and 4) Skin-effect [20].

At low frequencies, approaching DC, the current is uniformly distributed over the conductor. The DC resistance R_{dc} of a microstrip line is determined from the sheet resistivity

ρ_s of the metal. Typical values for aluminum and aluminum alloys are on the order of 30 mΩ-μm.

As the frequency increases (low MHz range), the current distribution changes due to the induced electric field in the conductor (produced by excess charges). The current concentrates at the sharp edges of the conductor. A reduction of the effective conductor cross-section increases the resistance [20]. Proximity effect also takes place when a nearby conductor carrying a time-varying current induces a magnetic field on the conductor which causes a current to flow in the opposite direction [21, 57].

At higher frequencies (in the range of MHz or GHz, depending on the strip line geometry), for MMIC lines, where $w/h < 0.1$ (h is the total substrate thickness, i.e., $t_{ox}+t_{si}$), the microstrip line is far enough from the ground plane such that the current is concentrated on the surface of the conductor as in the case of an isolated conductor, as illustrated in Fig. 26 (a). Hence, the ground plane resistance can be considered negligible [58].

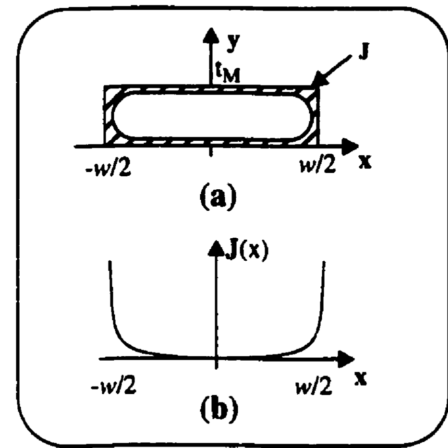


Fig. 26. Current distribution for an MMIC microstrip line.

At these higher frequencies, skin-effect takes place because for MMIC strip lines, the width is comparable to the metallization thickness (0.5 to 3 μm typical), and the skin depth value ($\delta = \sqrt{\rho_S/(\pi\mu_o f)}$ (m)) approaches that of the metal thickness: for ρ_{sAl} given above, $\delta = 2.578/(\sqrt{f})$ (μm), where f is in GHz. Also, due to skin-effect, the current crowds at the edges of the strip. However, all three effects (edge, proximity, and skin-effect) are present and it is difficult to identify the contribution of each one on the total current distribution [20]. Figure 26 (b) shows the current distribution on a microstrip line at high frequencies. Exact calculation of the frequency dependent resistance requires the need of a full-wave method. For example, Waldow and Wolff investigated the skin-effect on rectangular conductors at higher frequencies using a variational approach [59, 60].

To quantify the total resistance at high frequencies without the use of a full-wave method, the resistance can be defined as having a DC and an AC component R_{ac} as

$$R = R_{dc} + R_{ac} = \frac{\rho_s \cdot l}{t_M \cdot w} + R_{ac} \ (\Omega). \tag{13}$$

Several closed-form resistance approximations are found in the literature. Pettenpaul *et al.* [39] give an expression based on measured data for wide strips ($w > 50$ μm), Eo and Eisenstadt [61] derive an expression assuming an exponentially decaying current function, and Sonnet-em uses a square root frequency dependence to account for the skin-effect [62].

For this thesis, the series resistance expression chosen for the strip line r_{sl} is based on [61], given as

$$r_{sl} = \frac{\rho_{sAl} \cdot l}{w \cdot \delta \cdot (1 - e^{-t_M/\delta})} \ (\Omega) \tag{14}$$

which accounts for the metallization skin depth δ. The $\delta \cdot (1 - e^{-t_M/\delta})$ term is equivalent to an effective metal thickness t_{eff} [63]. However, Eq. (14) assumes that the skin-effect occurs from frequencies just above DC, which is not the case for narrow strip widths. To account for the skin-effect influence at a higher frequency, a transition frequency f_{se} is defined when $\delta = t_M$, which is also dependent on the t_M / w ratio. Hence, the resistance is normalized at a frequency f_{se} and the values below this frequency threshold is approximated by the DC resistance, as the following:

$$r_{sl} = \begin{cases} R_{dc} & f \le f_{se} \\ \dfrac{R_{dc}}{r_{se}} \cdot \dfrac{t_M}{\delta \cdot (1 - e^{-t_M/\delta})} & f > f_{se} \end{cases} \tag{15}$$

where r_{se} is the resistance at f_{se} defined by (14). Another approximation is also proposed by Eo and Eisenstadt [61], for modeling the side wall current of microstrip lines.

The resistance r_δ accounts for losses due to the longitudinal component of the conduction current in silicon. It is a function of the square of frequency [10] and dominates the inductor loss mainly as a function of ρ_{si} and f. It is approximated as

$$r_\delta \approx 3.5 \times 10^6 \cdot \frac{f^2 \cdot t_{si}^2}{\rho_{si}} \cdot l \ (\Omega) \tag{16}$$

where f is in GHz. r_δ was obtained by fitting Eq. (16) to the series resistance curves given by simulators. Hence, the total resistance becomes

$$r = r_{sl} + r_\delta \ (\Omega). \tag{17}$$

The accuracy of Eq. (17) will be illustrated through examples.

As the silicon resistivity decreases (ρ_{si} << 0.1 Ω-cm), the silicon acts as a lossy ground plane and its effect becomes dominant. For very low resistivities (< 0.1 mΩ-cm), the silicon can be considered as a lossy metal. Hence, the total resistance must take into account the resistance due to the silicon 'ground plane' because the strip is only on top of the oxide layer, such that the current distribution on the strip is mainly concentrated on the lower side close to the silicon 'ground plane'. The surface current on the ground plane is also concentrated under the strip so that the resistance of the ground place converges to r_{sl} at high frequencies and for $w/t_{ox} \rightarrow \infty$ [58].

Substrate Resistance due to Conductive Silicon

Similarly, computing the substrate resistance R_{si} is not an easy task. Full-wave methods that account for substrate resistivity are required. However, if the silicon capacitance is known, the following result is obtained from the resistance and capacitance definitions [64, 65]:

$$R_{si} = \frac{\varepsilon_{si} \cdot \rho_{si}}{C_{si}} \ (\Omega). \tag{18}$$

d) Temperature Dependence

An important aspect in designing RF circuits is the ability of the circuit to function within a broad temperature range (typically, -50 to 85°C). Metallization and substrate resistivities depend on temperature according to the following linear approximation:

$$\rho - \rho_o = \rho_o \alpha (T - T_o) \tag{19}$$

where T_o is a selected temperature, ρ_o is the resistivity at that temperature, and α is the temperature coefficient [66]. From experimental results, it has been shown that for Al/Cu (98% Al), α is around 0.34%/°C, whereas for a 15 Ω-cm silicon resistivity, it is 0.35%/°C [67]. As the substrate doping decreases, and hence a higher resistivity ρ_o ensues, a higher

temperature dependence is obtained, as seen from Eq. (19) [5]. An increase in the temperature results in an increase in the metal series resistance causing Q to decrease. The substrate resistance would, on the contrary, dominate the determination of Q at frequencies beyond the Q peak, and cause an increase in the Q. Nevertheless, for applications of inductors in silicon, the metallization resistance has the dominant effect on Q [67]. The inductance is not affected by temperature variation, and the substrate capacitance has a temperature coefficient of -0.18%/°C [67], which can be considered negligible for MMIC microstrip structures because a 10% change in the substrate capacitance would cause less than a 5% decrease in the overall performance such as Q. Hence, for MMIC spiral inductors on a SiO_2/Si substrate, it is the effect of temperature on the series resistance which should be considered.

2.5 Microstrip Line Simulation and Modeling

To verify what has been described throughout this chapter, various 1 mm long microstrip lines were simulated by two full-wave commercial electromagnetic simulators, Sonnet Software em and HP-EESof Series IV Momentum, referred to as the MoM (method of moment) simulator in this thesis, and an approximate model was also developed. Each simulator uses the method of moments in the spatial domain. Momentum uses a mixed potential integral equation [68], whereas Sonnet is based on an FFT [69]. Both use a rooftop expansion or basis functions for the current distribution. Results for line widths of 5, 10, and 20 μm and for silicon resistivities of 1, 10, and 100 Ω-cm will be presented and discussed. The oxide and silicon thicknesses are 5 μm and 350 μm, respectively. The aluminum metal thickness is 2 μm with a 30 mΩ-μm resistivity.

2.5.1 Approximation Model

The spectral domain technique was used to derive the substrate capacitances. For each substrate layer, the program was run for the particular substrate thicknesses: first, for that of the oxide from which C_{ox} was determined; and second, for that of the lossless silicon layer, where C_{si} and L were obtained. For ratios of $t_{si}/t_{ox} > 50$, the electric field distribution in the silicon layer does not change significantly whether a thin layer of oxide is present or not. For typical thicknesses (i.e., $t_{ox} = 5$ μm and $t_{si} = 300$ μm), this assumption holds. For this model, the line inductance value was approximated to be the same as the value for the silicon layer

alone because L depends on physical dimensions, and the difference is negligible (<1%) when compared with the structure's exact simulation. The program does not account for metal thickness. Other closed-form expressions could also be used, such as that of Greenhouse. The total series resistance r accounts for the skin-effect and the conductive silicon, defined in Eq. (17). Here, R_{si} was determined from C_{si} as in (18).

In the worst case, where w = 20 μm at 20 GHz, an effective relative permittivity of 13.6 was obtained. Hence the guided wavelength is 4.06 mm. For a lumped element equivalent circuit to hold for the microstrip line of 1 mm, a distributed model with at least three sections must be used, assuming that each section is smaller than one-tenth of the guided wavelength. For clarity, Fig. 27 shows a two-section distributed model. The series impedance and the shunt admittance are divided by the number of sections. To obtain the resulting Q, Port 2 is shorted, and the input impedance is determined as a function of Z_A and Z_B.

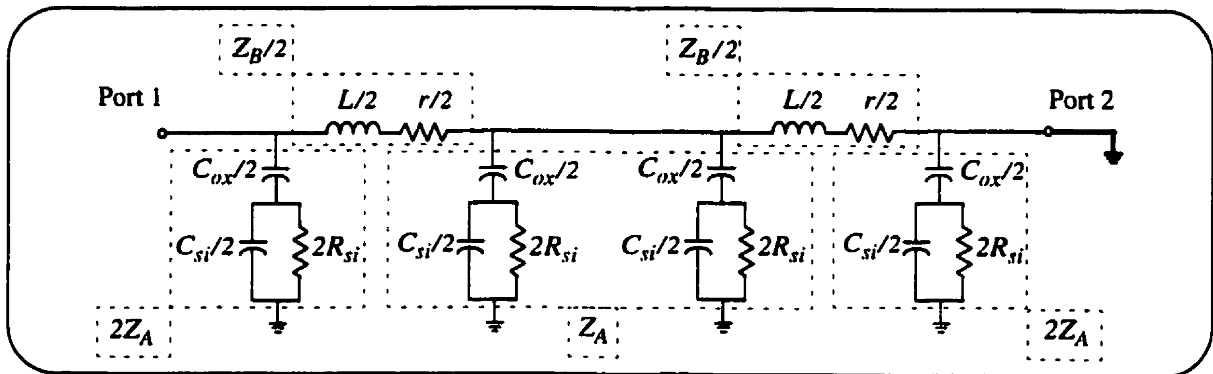


Fig. 27. Distributed model of a microstrip line with two sections.

2.5.2 Results

Table 1 compares the line inductance values obtained from the electromagnetic simulators and approximate expressions for ρ_{si} = 10 Ω-cm. Only Greenhouse [36] and Pettenpaul [39] account for the metal thickness. Sonnet-em and Momentum give the highest values, differing by as much as 10% from the other methods.

Table 1. Microstrip line inductance comparison for ρ_{si} = 10 Ω-cm.

Methods	*L* (nH) (*w*=5 μm)	*L* (nH) (*w*=10 μm)	*L* (nH) (*w*=20 μm)
Sonnet-em	1.357	1.176	1.009
Momentum	1.39	1.203	1.035
Model: SDA	1.26	1.12	0.988
Greenhouse [36]	1.231	1.124	1.003
Pettenpaul [39]	1.231	1.123	1.003
Lawton [70]	1.268	1.13	0.991

The inductance and series resistance (Fig. 28) are extracted from the simulated S-parameters using the method illustrated in Fig. 23. Simulated inductance curves show higher inductance values at low frequencies, an effect that is more pronounced using Sonnet-em (f < 4 GHz), which illustrate the limitations of the simulators. Moreover, the two simulators define the AC resistance differently, which results in different series resistance curves. Depending on the silicon resistivity and the frequency of operation, series impedances are different, mainly due to the conduction current in the silicon: r increases drastically as the frequency increases, and the line inductance decreases approximately linearly (< 1%/GHz at 1 Ω-cm). Therefore, a reasonable assumption for the inductance value as a consant is verified. Taking into account the metal thickness for the inductance causes a slight error (a 5% difference for a 5 μm width, computed by the Greenhouse and Pettenpaul expressions). The low frequency series resistances are equivalent to the DC resistance. The model used for the resistance approximates the curve of Sonnet-em because the resistance expressions both depend on the square root of the frequency. For ρ_{si} equal to 100 Ω-cm, the conduction current in the silicon is considered negligible and does not affect the total resistance. At 10 Ω-cm, the conductive silicon effect is more pronounced at higher frequencies (> 10 GHz). In the slow-wave mode (ρ_{si} = 1 Ω-cm), the conduction current in the silicon is dominant, so that the total resistance depends mainly on r_δ. Therefore, the resistance expression for the model, Eq. (17), is validated.

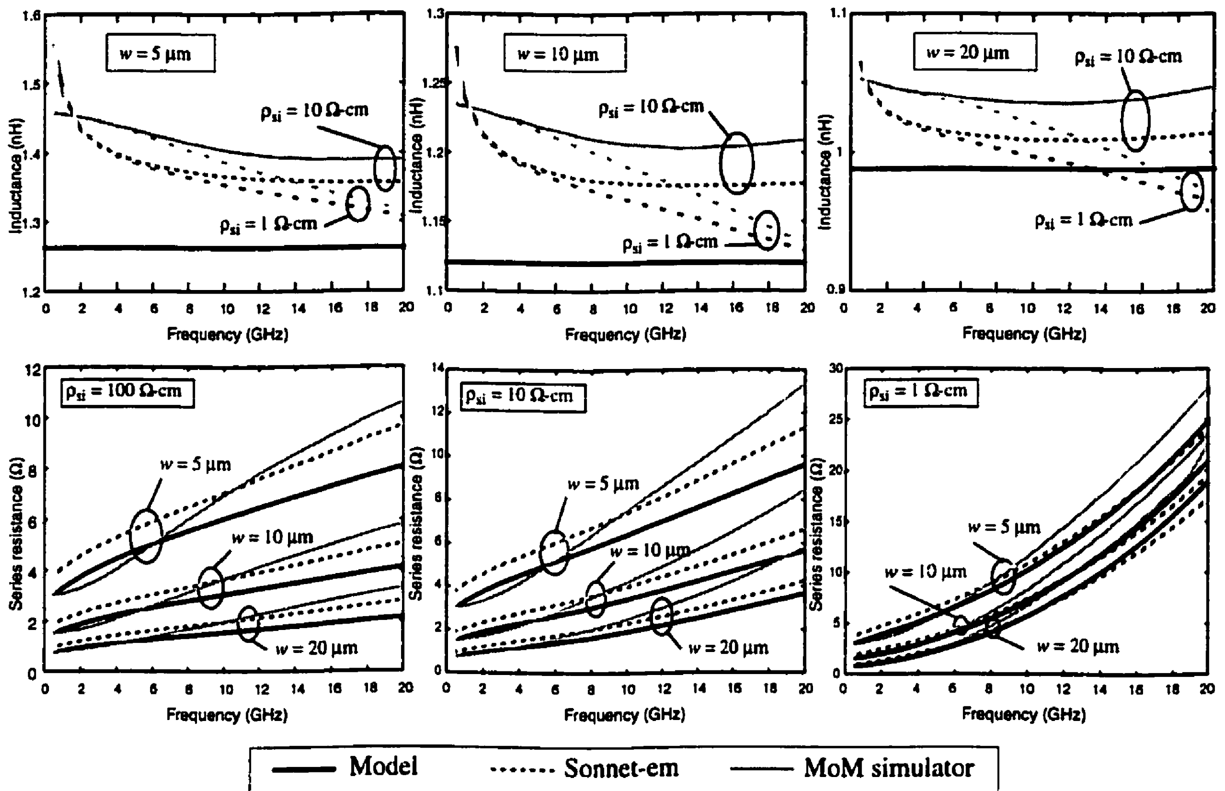


Fig. 28. Inductance L and series resistance r for 1 mm long microstrip lines.

As shown in Fig. 29, for substrate parasitics, two models were used, where C_p and R_p are the parallel equivalent, and C_s and R_s are the series equivalent frequency dependent lumped elements corresponding to the actual shunt impedance.

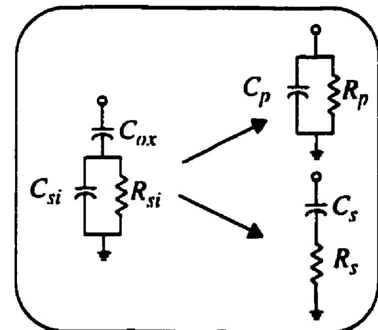


Fig. 29. Equivalent shunt substrate parasitics.

In Fig. 30, substrate parasitic plots are shown for each of the three silicon resistivity values. The approximate model provides reasonable values, within 5% of the simulated results. Therefore, representing the substrate parasitics as a series connection of the oxide and silicon parasitics seperately as assumed, is verified. The frequency behaviour of the equivalent total substrate capacitance depends on the distribution of electric fields in the oxide and the silicon layers. For ρ_{si} equal to 100 Ω-cm, substrate parasitics are constant beyond 3 GHz, proving that the quasi-TEM mode is excited (see Fig. 13). Since R_p is in the kΩ range (> 5 kΩ), C_p is equivalent to the series combination of C_{ox} and C_{si}, for frequencies beyond 3 GHz where the electric field is distributed in the oxide

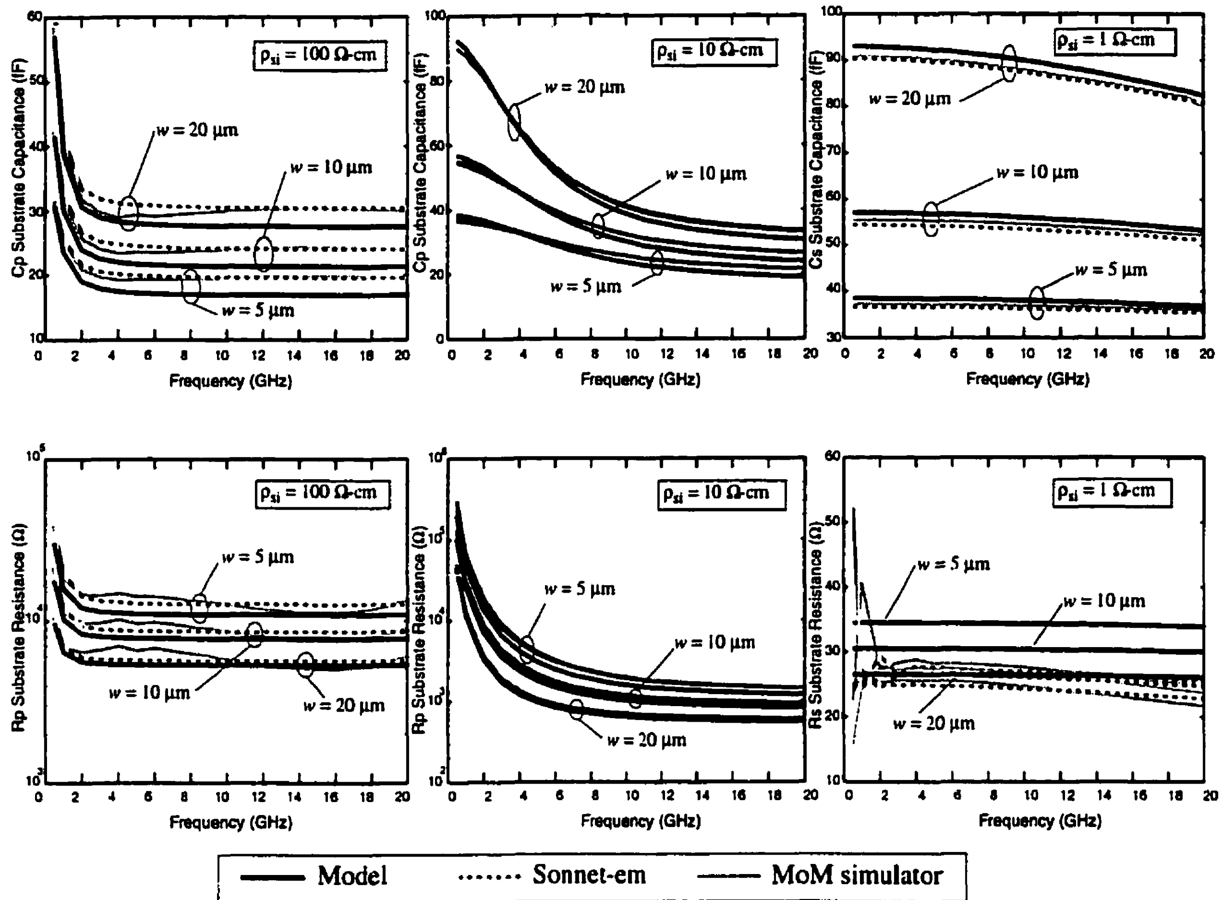


Fig. 30. Substrate capacitance and resistance for 1 mm long microstrip lines.

and silicon substrates with a higher domination in the silicon. In the transition region from the quasi-TEM to the slow-wave modes, low frequency substrate capacitance corresponds to the oxide value C_{ox}, whereas when the frequency increases, the value converges to approximately 10% higher of the value of C_{ox} and C_{si} in series because of the presence of the substrate resistance. As shown in Fig.12, in the slow-wave regime, most of the energy is in the oxide. Penetration of electric field in the silicon appears gradually from 2 GHz where it dominates beyond 20 GHz. For a resistivity of 1 Ω-cm, where the microstrip structure is well within the slow-wave mode (see Fig. 13), most of the electric field is present in the oxide compared with in the silicon (as in Fig. 9). Hence, the parasitics correspond to C_{ox} and R_{si} in series, and C_{si} can be considered negligible. At low frequencies, for the R_s plot, both simulators exhibit numerical instabilities.

For overall performance visualization of the microstrip line, Q-factor plots are shown in Fig. 31. The microstrip line model presented compares well with the full-wave simulated data. Agreement within 10% is achieved. Curves obtained from the MoM simulator have a higher peak Q at a lower frequency than those from Sonnet-em and the model, mainly because of the difference in the series resistance. For a ρ_{si} of 100 Ω-cm, the MoM simulator Q curves do not follow the curve obtained from the model because of numerical instabilities of the simulator for the substrate parasitics (see Fig. 30). The Q of the model is higher than the simulators', since the Q follows $\omega L/r$ until 8 GHz, thus the influence of the series resistance r is more pronounced on the overall Q. As shown in Fig. 28, r of the model is smaller than that of the simulators' for frequencies beyond 7 GHz.

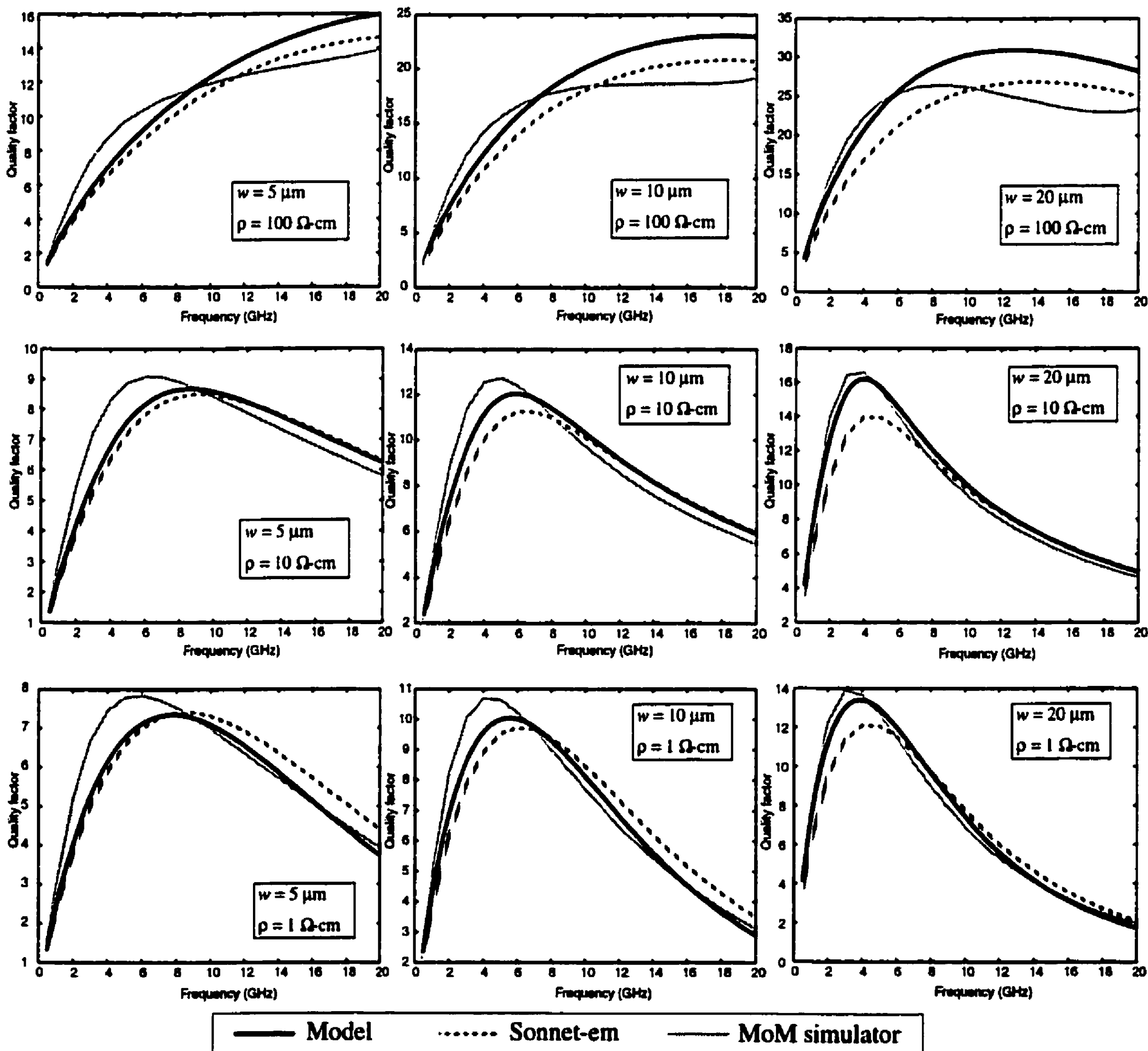


Fig. 31. Quality factor for 1 mm long microstrip lines.

As the silicon resistivity decreases, so does the Q and the self-resonant frequency due to higher substrate capacitance ($C_{ox} > C_{si}$) and lower substrate resistance (R_{si}). With an increase in the linewidth, higher Q and lower self-resonance are obtained because of lower series resistance and higher substrate parasitics, even though the line inductance decreases, although not as significantly.

The model proposed for a microstrip line can be applied to coupled lines or a spiral inductor by including the negative and positive mutual inductances and capacitances, as will be shown in the following chapter.

Chapter 3

SPIRAL INDUCTOR MODELING

This chapter describes a simplified model and parameter extraction technique for spiral inductors in silicon technology. The model is validated using experimental measurements and full-wave electromagnetic simulations.

3.1 Motivation

Spiral inductors are utilized in many RF/MMIC applications. For computer-aided design (CAD) purposes, a lumped element equivalent circuit, or electrical model, is required. An accurate CAD model is needed to predict correctly the overall performance of an RF circuit. Full-wave commercial electromagnetic simulators are computationally intensive, i. e., they require a great deal of CPU time and memory. Therefore, microstrip inductor models, derived from layout and process fabrication parameters, are needed. Several modeling techniques are reviewed in the following paragraphs.

As shown in Fig. 22, the parameters of a single π-type equivalent circuit can be found by computer optimization so that the measured S-parameters for a spiral inductor and the S-parameters of the equivalent circuit model agree to within a specified tolerance. The compact model is the simplest representation of the spiral; it was used by Ashby *et al.* [71] and Yue *et al.* [63]. The total inductance and series resistance are computed from closed-form expressions, as given in Sections 2.4.2 a) and c). However, the total capacitive and resistive substrate parasitics are fit to the measurements using an optimizer [71] or to the measured properties of the silicon substrate [63].

A more accurate equivalent circuit for the entire rectangular spiral inductor is obtained by dividing the spiral into groups of multiple coupled lines. Some approaches derive the inductance and resistances of each line segment in a group in closed-form, whereas the parasitic capacitances are obtained from two-dimensional static numerical computations, as described in Section 2.4.2 b) [38, 72, 25]. Figure 32 gives such a lumped element equivalent circuit model for a one-and-a-half turn rectangular spiral inductor. The model consits of a

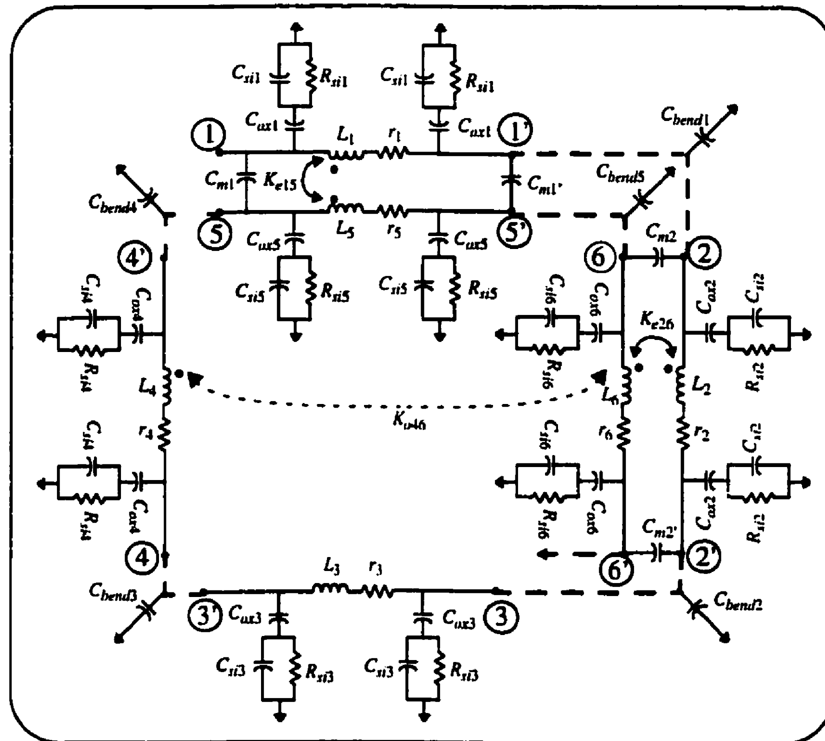


Fig. 32. Lumped element circuit model for one and a half turns of a spiral inductor.

series connection of electrically short microstrip line segments joined by inductive coupling coefficients (K_e for the same group of coupled strips, and K_o for opposite groups) and mutual line-to-line capacitive components C_m. Each segment is represented by its equivalent circuit model (Fig. 15). Capacitances C_{bend} due to the microstrip bends can also be taken into account [25]. Full-wave methods have also been used for extracting the individual lumped elements of each line segment [27] or sets of coupled lines [31, 73], which are then connected together to form the entire spiral. The lumped equivalent circuit can become highly complex; however, it can still be easily handled by a circuit simulator tool, such as SPICE. This equivalent circuit can also be reduced to a compact model [25].

Building upon the simplicity of the compact model, a circuit with only the minimum number of lumped elements, a novel extraction method is proposed for the parasitics and the series resistance of the entire spiral structure; it does not require computer optimization. This technique simplifies the representation of the spiral inductor, and it can be easily integrated into a circuit simulator. It uses closed-form expressions for the total inductance, resistance, and underpass capacitance. A 2D static numerical method extracts the line capacitances, reducing computation time with minimal loss of accuracy. The interwinding capacitances are

obtained from the odd-mode mutual coupling of two coupled lines. The longitudinal component of the conduction current in a semiconducting substrate is included in the resistance model to account for all significant sources of loss. This method is numerically more efficient than full-wave modeling techniques and is sufficiently accurate for design purposes. Measured and simulated results are compared with the proposed model to establish its range of validity.

3.2 Modeling Procedure

A model was developed in Chapter 2 for a single microstrip line. A new approach is presented, based on the parameter extraction procedure for a single microstrip line. Instead of regarding the spiral inductor as a succession of microstrip lines coupled together by groups, as shown in Fig. 32, this approach is derived from looking at the entire structure. The new procedure is outlined below for each extracted parameter.

3.2.1 Inductance

The total static inductance of a spiral inductor is calculated using Greenhouse's method, where the self, mutual positive and negative inductances are computed and summed to obtain the total inductance of the spiral structure [36]. The width and spacing of the lines, the number of turns, the thickness of the metal, and the outer dimensions of the spiral must be specified. For the range of silicon resistivities of interest ($\rho_{si} \geq 1$ Ω-cm), the inductance can be regarded as a constant, as shown in Fig. 28 for a single microstrip line.

3.2.2 Series Resistance

The ohmic loss represented by the series resistance of the inductor is a frequency dependent parameter. The expression given by Eq. (17) is used for the model, which takes the skin-effect and the effect of the conductive silicon into account. An in-depth discussion is given in Section 2.4.2 c).

3.2.3 Substrate Parasitics

a) Substrate Capacitance

The substrate capacitances have series components due to the oxide and silicon layers. In the case of a single microstrip line, these capacitances were calculated by extracting the values for the oxide layer only, i.e., the ground plane at the SiO_2/Si interface, and then repeating this calculation for the silicon layer (oxide removed and $\sigma_{si} \rightarrow 0$). Hence, two line capacitances were obtained separately. This method is also applied to the spiral inductor model.

The line-to-ground capacitance is obtained from the even-mode capacitance of adjacent coupled strips. The capacitance extraction method is explained more clearly by giving an example for a 4.25 turn square spiral inductor, as shown in Fig. 33. The spiral is divided into sections of one, two, three, four, and five coupled strips. The total capacitance is a summation of group capacitances times the lengths of the groups. For a 4.25 turn spiral, the capacitance is approximated as

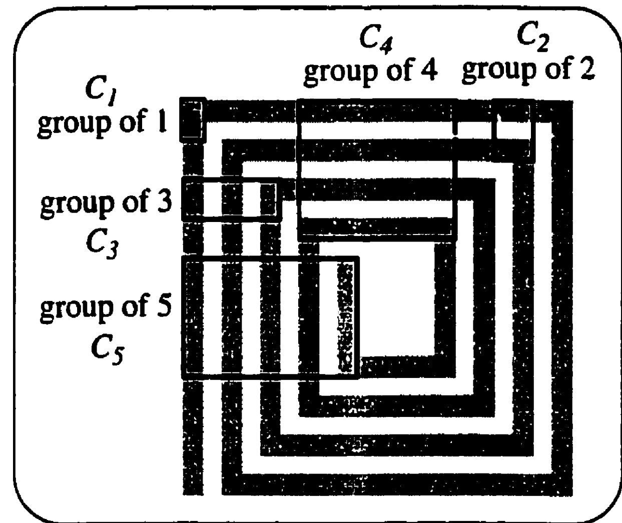


Fig. 33. A 4.25 turn spiral inductor with different groups of coupled lines for line capacitances.

$$C_{total} = C_5 \cdot [OD - 7(w+s)] + C_4 \cdot [3OD - 17(w+s)] + (C_3 + C_2 + C_1) \cdot 8(w+s) \qquad (20)$$

where $C_{i=1..5}$ are the line capacitances for the different groups of coupled strips, computed from a two-dimensional numerical method. For each layer of substrate (SiO_2 and Si), the capacitances per unit length are given for each group of coupled strips, and the total capacitances obtained from (20).

The parameter extraction method for the total substrate capacitances gives the average overall capacitance of the spiral inductor. To approximate for the asymmetry in the spiral inductor distributed by the two ports, the N turn spiral is divided in two at N/2 turns. As shown in Fig. 34, the length corresponding to the first half of the spiral lg_1 is higher than that for the length of the second half lg_2. The fractions lg_1/l and lg_2/l give the ratio for the substrate capacitances. Hence, $C_k = 2C_{total} \cdot lg_k/l$, where k=1, 2.

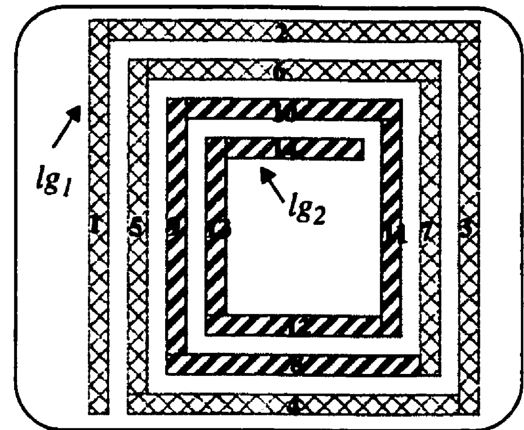


Fig. 34. A 3.5 turn spiral inductor divided into two lengths.

Representation of the compact model using two different sets of substrate parasitics at each port does not significantly improve the overall accuracy when compared with the total average values, using (20) only. Therefore, in this thesis, the same set of parasitic values are used in the compact model, reducing the total computational time.

b) Substrate Resistance

The silicon resistance is obtained using Eq. (18) from the total silicon capacitance. Contrary to the model used for a single microstrip line, where R_{si} is derived from C_{si} (the total silicon capacitance of the line), a factor of 2 in Eq. (21) is a fitting parameter that adjusts the substrate parasitics to correspond to the measurements and full-wave simulations. Therefore, the resulting silicon resistance becomes

$$R_{si} = \frac{2 \cdot \varepsilon_{si} \cdot \rho_{si}}{C_{si}} \ (\Omega). \tag{21}$$

3.2.4 Line-to-line Capacitance

The line-to-line capacitance C_o is a combination of the interwinding and underpass capacitances. The underpass connects the inside of the spiral to the external circuitry; its capacitance is approximated by the parallel-plate capacitance between the top metal and the lower metal used for the underpass, as given by Eq. (12). Due to stray fields, additional capacitance results. It has been shown that the total underpass capacitance is 1.55 to 1.7 times

higher than that of the parallel-plate model [54]. The interwinding capacitance between adjacent strips has to be taken into account in the model due to phase shift along the spiral, resulting in a potential difference between each turn. This was not considered by other authors [31, 74] who approximate the overall line-to-line capacitance as a summation of underpass capacitances only.

The interwinding capacitance is the odd-mode coupling capacitance in the substrate and air between two coupled strips [55], as described in Section 2.4.2. b). The thickness of the metal conductors must also be taken into account in the 2D numerical method. The coupling capacitance C_c is a summation of C_{gd} and C_{ga}, the gap capacitances in the dielectric and the air, respectively. C_{gd} is defined as the average difference of the odd-mode and even-mode stripline-to-ground capacitances with the dielectric filled with oxide. The gap capacitance in the silicon is considered negligible. Similarly, C_{ga} is obtained with air as dielectric, and it should not take the fringing capacitances into account since these were included in the calculation of C_{gd}. Hence, C_c is the average sum of C_{gd} and C_{ga}.

As shown in Fig. 35, the different mutual coupling capacitances C_m are distributed along the spiral. Each C_m is obtained from the coupling capacitance C_c times the length of each set of two coupled strips and is represented by two components at each end of the coupled strips. The coupling between non-adjacent strips of the same group has been considered negligible. Underpass capacitances C_u are also distributed along the segments where the underpass crosses the spiral. These are connected to Port 2.

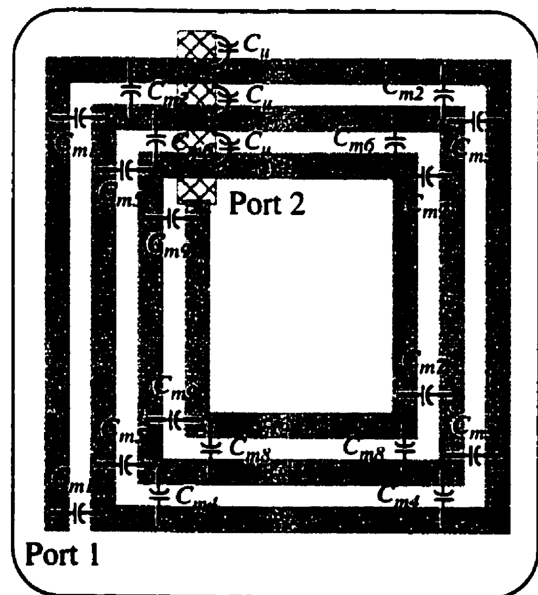


Fig. 35. Representation of the interwinding and underpass capacitances.

The total line-to-line capacitance C_o is obtained from optimization. Each line segment is approximated as an inductance to represent the series impedance of the microstrip line. The two-port network consisting of interwinding capacitances bridged between line segments is translated to a capacitance in shunt with an

inductance. The optimization is performed by fitting the equivalent two-port parameters of the entire structure to a single capacitance, that is, C_o, in shunt with an inductance L_o, at frequencies near the resonance of C_o and L_o.

3.2.5 Final Inductor Model

The inductor equivalent circuit is distributed into $n = 4N$ identical sections, as illustrated in Fig. 36. The maximum *OD* represented as a single lumped element pi-section is assumed to be less than one-tenth of the guided-wavelength, defined as

$$OD_{max} = \frac{\lambda_g}{10} = \frac{c}{2.5 f_{srf} \cdot \sqrt{\varepsilon_{reff}}} \text{ (m)} \tag{22}$$

where c the speed of light and f_{srf} is the self-resonant frequency of the spiral inductor defined for $\lambda_g/4$.

Justification for the number of sections chosen is as follows. Assuming a maximum line width of 50 μm and an effective dielectric constant of 100, Eq. (22) predicts that f_{srf} is 40 GHz for an *OD* of 300 μm. The useful range of frequencies for a spiral inductor with an *OD* of 300 μm is typically below 4 GHz, or one order of magnitude lower in frequency. Therefore, a conservative estimate for the maximum number of sections n required is the total number of segments 4N. The final equivalent circuit model is shown in Fig. 36.

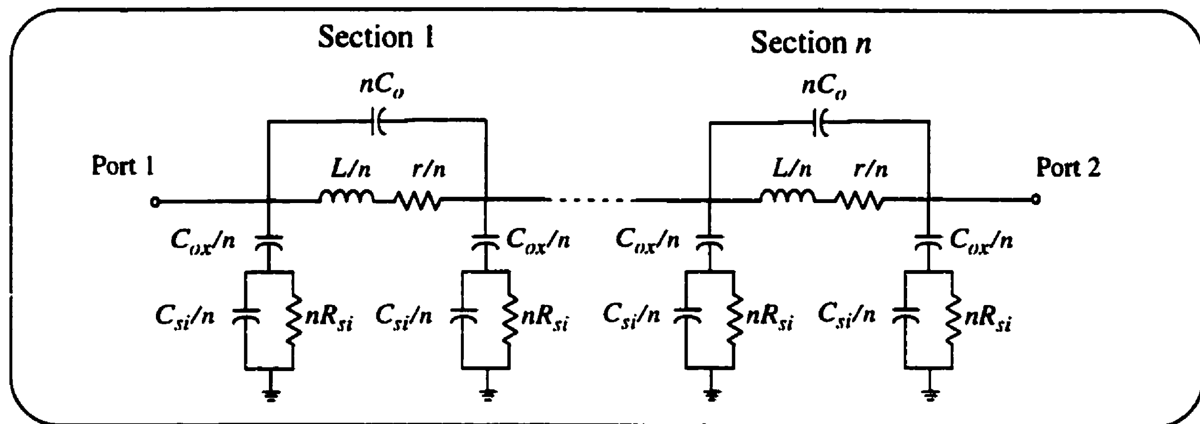


Fig. 36. Distributed model for the spiral inductor equivalent circuit.

Fig. 37. Photomicrograph of a 4.25 turn, 5 nH spiral inductor of 15 μm width and 1 μm spacing.

3.3 Test Structures

Two different spiral inductor structures are used to verify experimentally the model described above. The first inductor consists of a 4.5 turn spiral with $OD = 241$ μm, $w = 10$ μm, and $s = 5$ μm, fabricated in a BiCMOS process, (see [25]). The specified ρ_{si} can range between 5 Ω-cm and 15 Ω-cm due to the uncertainty in the starting wafer. The underpass is 15 μm wide and is 1 μm from the upper metal.

A second 4.25 turn 5 nH square spiral inductor, fabricated in a medium resistivity silicon ($1 < \rho_{si} < 10$ Ω-cm) CMOS process, is also used for validation. Figure 37 shows the top view of a 15 μm width inductor with its signal and ground pads.

3.4 Results and Discussion

Table 2 gives the lumped element values obtained from the model for each inductor. The total length of both inductors is around 3.2 mm. The maximum number of sections required to account for the distributed model of the coil is 18 for the BiCMOS inductor. It has been verified that $n = 8$ is a sufficient value. Parameters for the CMOS inductor confirm the

component values extracted from optimization fit of measured and simulated data (see Fig. 22). In the model, C_{ox} represents C_{oxl} in Fig. 22, and C_{si} and R_{si} are the averaged values of $C_{sil,2}$ and $R_{sil,2}$, respectively. To account for the asymmetry of the spiral, Table 2 also gives the corresponding substrate parasitics at each port. Using the averaged values in the compact model does not alter the overall performance such as Q-factor.

Table 2. Lumped element values for spiral inductor models.

Inductor	L (nH)	R_{dc} (Ω)	C_{ox} (fF)	C_{si} (fF)	R_{si} (Ω)	C_o (fF)
BiCMOS	5.3	8.7	178 (210/146)*	45 (53/37)	229 (196/280)	15
CMOS	5	7.1	204 (238/172)	44(51/37)	282 (243/336)	35

* Values in ( ) are the calculated subtrate parasitics at Port1 and Port2, respectively.

To compare the different results, the equivalent transmission line parameters are extracted using the method shown in Fig. 23. In the case of low silicon resistivities, the representation of the substrate parasitics as a series capacitance and resistance is adequate, as shown for a single microstrip line in Fig. 30.

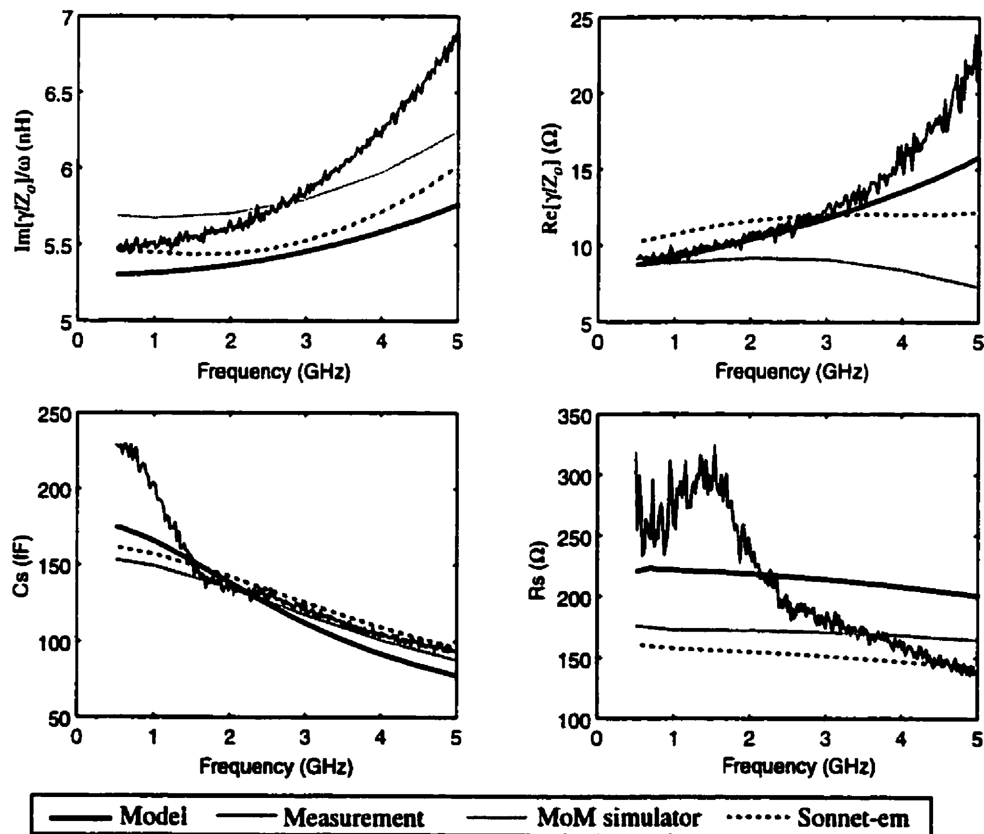


Fig. 38. Transmission line equivalent parameters for the BiCMOS 4.5 turn inductor.

Line parameters as a function of frequency are given in Figs. 38 and 39 for the two different spiral inductors. The low frequency inductance agrees with the total inductance obtained using Greenhouse's method. The MoM simulator predicts an inductance that is higher by 10%. The agreement between simulations for the series resistance is less good: low frequency resistance r_{LF} approximates the DC resistance, but the Sonnet-em resistance model gives a 10% higher r_{LF}. Moreover, neither simulator seems to properly predict the influence of the skin-effect and substrate conductive losses. However, substrate elements extracted from the simulation compare reasonably well with the measurements. In Fig. 38, measurement errors for the substrate parasitics result from inaccuracies due to the network analyzer at low frequencies (f < 1.6 GHz). The model provides a substrate resistance as much as 30% higher than the measurements due to lower C_{si} compared with the input port C_{sil} of a spiral inductor. The difference in substrate resistance does not alter significantly the overall performance of the inductor.

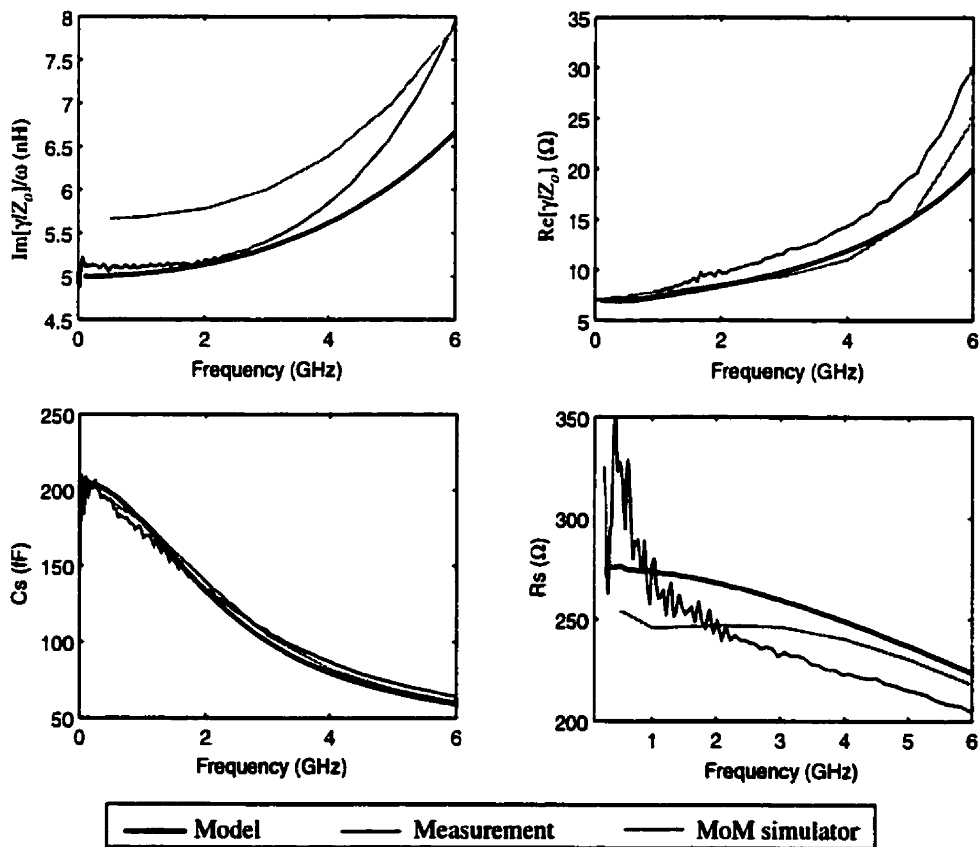
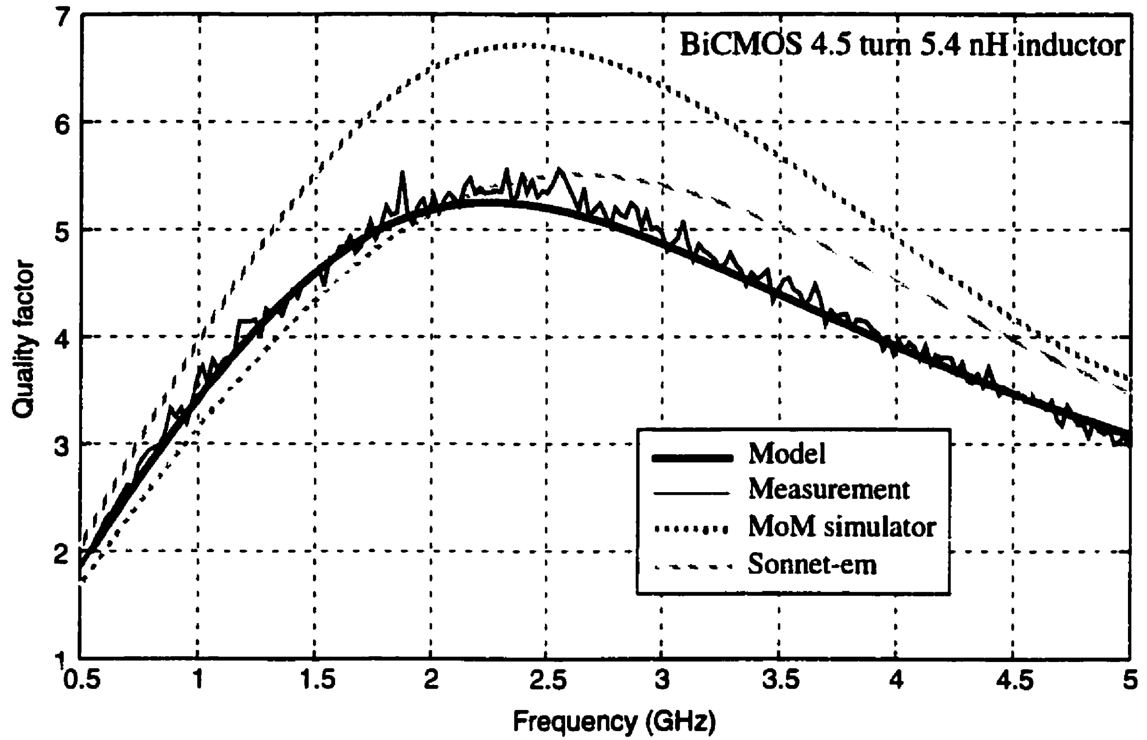


Fig. 39. Transmission line equivalent parameters for the CMOS 4.25 turn inductor.

The Q-factors (Fig. 40) for both inductors show the influence of the line parameters. The model agrees well with the measurement curve. The Q-factors from the MoM and Sonnet-em simulators differ from the model and measurement curves because of the inaccurate series impedance values. The low frequency ($f < 1$ GHz) Q demonstrates the variation in series resistance: Sonnet-em has a higher r_{LF}, and the MoM simulator a lower r_{LF}, which explains the difference in the peak Q and the shift in the frequency at which Q peaks.

The inductor model compares well with the experimental results, so it can be used to predict the actual performance of an inductor before it is fabricated. Moreover, the model can be easily implemented in a circuit simulator, given prior knowledge of process parameters and the physical layout of the inductor. The various lumped element parameter extraction methods can be implemented in a single computer program. The input parameters are OD, w, w_o, s, N, t_{ox}, t_{si}, t_M, t_{Mox}, ρ_{si}, and ρ_S. Since the single element section can be represented as a subcircuit, implementation in the circuit simulator such as SPICE is simplified. The application of the inductor model will be demonstrated for an oscillator circuit, described in Chapter 4. The modeling technique proposed in this thesis can also be used for MMIC spiral transformers. The same extraction procedure for the substrate parasitics would apply.



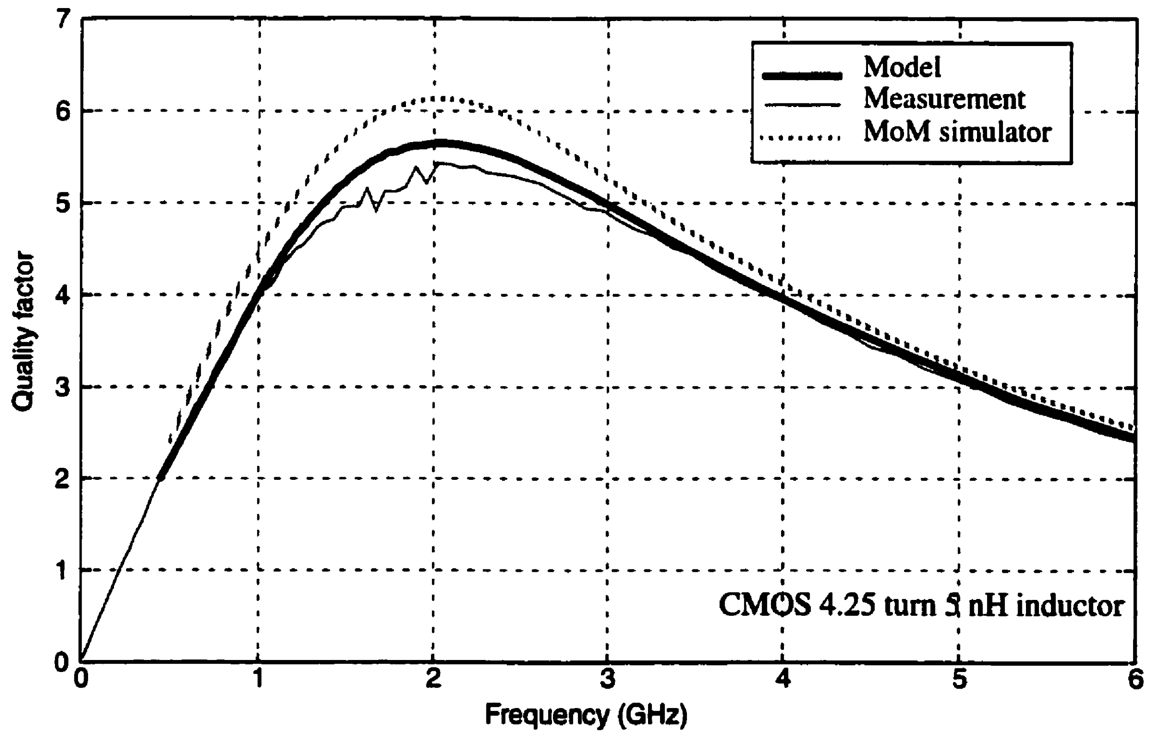


Fig. 40. Quality factor comparisons between models, measurements, and simulations for two spiral inductors.

Chapter 4

SYMMETRIC INDUCTORS FOR DIFFERENTIAL CIRCUITS

This chapter proposes a new inductor design that is suitable for differential circuits, in particular. First, current inductor configurations and their performance are reviewed. The theoretical background for single-ended and differential excitations of a microstrip structure is presented. Measurements, simulations, and an inductor model are then compared. Finally, oscillator circuits are designed to illustrate an application of inductors and their models.

4.1 Motivation

The quality factor of microstrip structures is limited by the series resistance of the metallization and, in the case of silicon technology, losses in the conductive substrate. The *Q*-factor is typically less than 10 for a metal-insulator-semiconductor (MIS) structure fabricated in a production silicon IC technology. Table 3 lists typical *Q*s for different inductor designs and silicon resistivities. For most CMOS technologies, *Q*-factors range from 2 to 4.

Table 3. Typical inductor *Q*-factors for standard Si IC processes.

Technology	Reference	*L* (nH)	ρ_{Si} (Ω-cm)	t_M (μm) / ρ_{SAl} (mΩ-μm)	Dimensions $OD/w/s/t_{ox}$ (μm) / N	Q_{peak} f_{peak} (Ghz)
Bipolar	Nguyen [4]	1.9	14	1.8 / 20	115/6.5/5.5/ 1.7/4	8 4.1
Bipolar	Nguyen [4]	9.7	14	1.8 / 20	230/6.5/5.5/ 1.7/9	3 0.9
BiCMOS	Long [25]	5	10	1 / 30	166/5/1.5/5 /4.5	5.3 3.3
BiCMOS	Long [25]	1.8	10	3 / 3C	-/ 15/ 1.5/5/ 3.5	10 4
BiCMOS	Yue [63]	8	10	2 / 30	300 / 13 / 7 / 4.5 / 7	5.5 1.3
CMOS	Craninckx [24]	3.2	0.01	- / 35	r=85 / 8.5 / 1.5 / 0.7 / 4	5.7 1.8
CMOS	Lutz [27]	10	0.01	0.75 / 34	245, 230 / 10 / 1.8 / 3 / 9.5	2.3 1.5

For narrowband wireless applications, such as *LC* tanks in oscillators, *Q*s of at least 10 are required [1]. Thus, due to the limited *Qs* available on-chip, low noise and very narrowband applications require external high *Q* resonators. Front-end filters are commonly placed off-chip. However, integrated spiral inductors are currently used for on-chip impedance matching and tuned loads [74, 75].

4.2 Review of *Q* Enhancement Techniques

The inductor *Q*-factor is constrained by the metallization resistance, the conductive loss due to the silicon substrate, and the substrate parasitic capacitances (which limit the inductor self-resonant frequency). Several approaches have been applied to enhance the *Q* at its peak and/or the self-resonant frequency. Before applying the enhancement methods, a set of inductor design guidelines must be followed.

4.2.1 Optimization by Inductor Design

A set of design rules for rectangular spiral inductors [25, 76], most of which have already been presented in Chapter 2, are summarized as follows:

1) The space between the outer spiral turn and any other surrounding metal structures must be at least $5w$ to avoid coupling between structures.

2) Tight magnetic coupling, using the minimal allowable spacing s, not only maximizes *Q* but also reduces the total chip area.

3) A 10 to 15 μm strip width w is close to optimum for the *Q*-factor when the frequency of operation is in the 1-3 GHz range. Another consideration is the skin effect at higher operating frequencies for increasing line widths.

4) Opposing sets of coupled lines must be separated by at least $5w$ to allow enough magnetic flux to pass through the hollow part of the spiral, and also to minimize the conductive substrate eddy current effects.

5) The oxide layer should be as thick as possible to reduce the substrate parasitic capacitance, thus increasing the inductor self-resonant frequency.

6) The metal thickness and resistivity are fixed by the fabrication technology; however, multilevel metal processes allow for the parallel connection of metals or metal stacking to reduce the ohmic losses at the expense of decreasing the oxide thickness.

4.2.2 Optimization by Reducing Ohmic Losses

Investigation of varying strip line metal thickness has been conducted by Long and Copeland [25], showing a 67% increase in the peak Q-factor for a 1.8 nH inductance resulting from a 1 μm to 3 μm metal thickness increase, whereas Yue *et al.* [63] show a 37% increase from a 1 μm to 2 μm increase for an 8 nH inductor. Hence, doubling the metal thickness does not result in twice the Q-factor. For a double metal thickness, the DC resistance is halved. However, the total resistance is higher than expected due to the skin-effect. An effective thickness t_{eff} defined using (14) shows that a 1 μm and a 3 μm thick Al metallization have t_{eff} equal to 0.84 μm and 1.83 μm at 1 GHz, respectively [63]. Moreover, an increase in the metal thickness causes the inductance to decrease by a small percentage (<10%). Hence, for twice the metal thickness, a doubling of the Q-factor is impossible.

With the metal layers provided by modern process technologies, metal strips can be stacked by using vias, as shown in Fig. 41. Lower metal layers are used for underpasses. For a 2 nH inductor, a 50% increase in the peak Q-factor was obtained by shunting three metal layers as in Fig. 41. The DC series resistance was nearly halved. The process used had a greater oxide thickness (10 μm instead of 4 μm) to allow a reasonable (> 2.1 μm) separation distance between the lowest metal and the silicon substrate. The Q increased by 30% if a 5-level metal process was used instead of 4 levels because the underlying oxide thickness was doubled, resulting in a lower oxide parasitic capacitance [77].

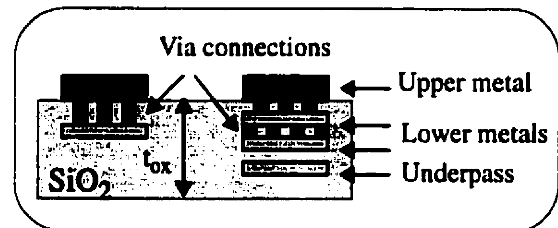


Fig. 41. Metal stacking in the oxide layer.

The use of copper metallization is also being developed to take advantage of its lower resistivity (ρ_{SCu} = 17.5 mΩ-μm). Current Cu VLSI technology allows for 6-level metal layers with a top metal thickness of 4 μm instead of the 2 μm typical for aluminum. For copper conductors fabricated using a damascene process (evaporation of copper followed by chemical/mechanical polishing), the series resistance is 60% lower, and the peak Q increases on the order of 50 to 85%, depending on the inductor layout [78].

4.2.3 Optimization by Reducing Substrate Losses

Conductive losses due to the silicon layer may be reduced by lowering the doping of the wafers themselves. Substrate resistivities in the low kΩ-cm range have been investigated. The results obtained for spiral inductors on a high resistivity silicon (HRS) ($\rho_{Si} > 1$ kΩ-cm) approach those for GaAs ($\rho_{GaAs} \approx 100$ kΩ-cm) [79]. Ashby *et al.* [71] presented a maximum Q of 12 for a 2.5 nH inductor with ρ_{Si} on the order of 150 to 200 Ω-cm and using thick ($t_M = 5$ µm) gold metallization. Park *et al.* [80] investigated the effects of three silicon resistivity values on the inductor line parameters and resulting Qs. For a 13 nH inductor, the Q is 2.7 at 1 GHz for $\rho_{Si} = 4\text{-}6$ Ω-cm, whereas when a 2 kΩ-cm resistivity is used, the Q increases to 6.9 at 3 GHz. The R_{si} was almost twenty times higher for the HRS.

Although increasing the silicon resistivity may seem a perfect way to enhance the Q-factor, restricted wafer size (2" wafer diameter for 10 kΩ-cm silicon instead of 8" for $\rho_{Si} < 20$ Ω-cm) adds to the manufacturing cost of circuits.

A closer look at the behavior of the Q-factor with respect to the ohmic losses in the silicon suggests introducing a ground shield above the silicon layer. The shield creates a "short" instead of an "open" connection, i.e., $R_{si} \rightarrow 0$ vs. $R_{si} \rightarrow \infty$. However, a solid ground shield reduces the inductance because of modified magnetic field distribution and stronger induced currents on the shield, which adds negative magnetic coupling. Figures 42 (a) and (b) illustrate how the electromagnetic field distribution is altered due to the ground shield.

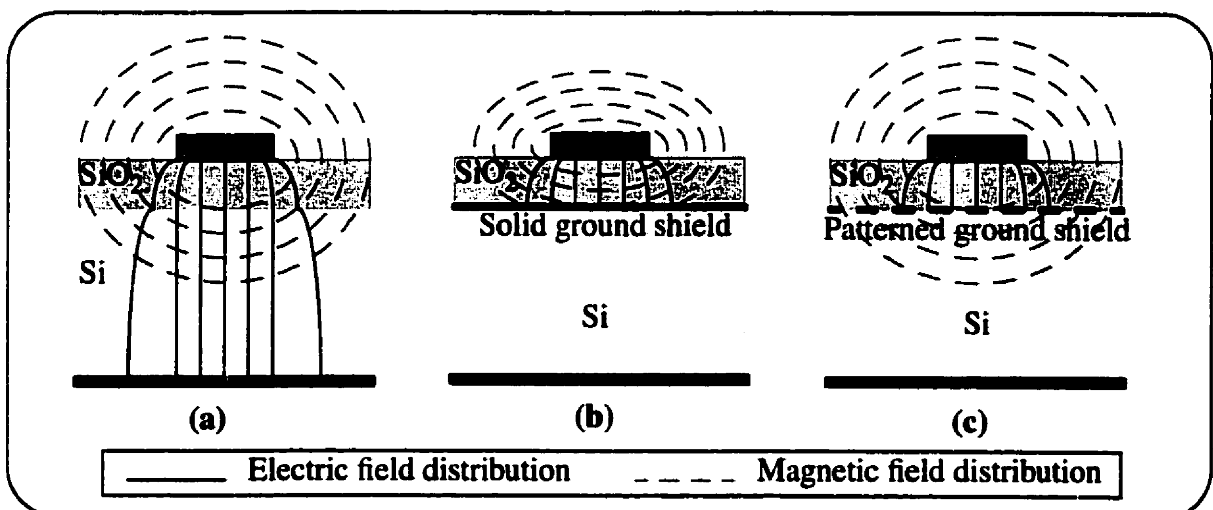


Fig. 42. Electric and magnetic field distributions for microstrip lines (a) without a ground shield, (b) with a ground shield, and (c) with a patterned ground shield.

Designing a patterned ground shield with narrow slots, such as the one shown in Fig. 43, minimizes the electric field penetration into the silicon, but does not significantly alter the magnetic fields (Fig. 42 (c)). Reduction of the line inductance due to the induced currents on the shield is minimized by using a thinner metal layer. The order of the metal thickness must be smaller than the skin depth of the metal at the operating frequency. A comparison between 0.5 µm aluminum (ρ_S = 64 mΩ-µm) and doped polysilicon shields (ρ_S = 12 Ω-µm) for an 8 nH inductor on an 11 Ω-cm substrate showed a greater peak Q for the polysilicon (20% for polySi vs. 13% for Al) than without metal ground shields. The measured substrate loss element R_p of the compact model in Fig. 20 increased more than ten times. However, a higher shunt parasitic capacitance results because the electric field does not penetrate into the silicon, so that only C_{ox} is taken into account in the inductor model. Hence, a faster Q roll-off after the peak ensues, and the inductor self-resonance occurs earlier, at 3.6 GHz instead of at 6.5 GHz [29].

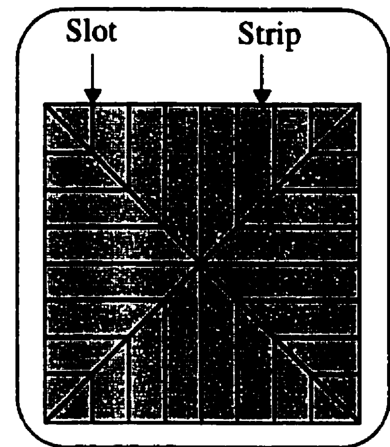


Fig. 43. Patterned ground shield.

Another approach is to selectively remove the underlying silicon substrate using a post-fabrication wet [81] or gaseous etch [82] to reduce the parasitic capacitances of the substrate (Fig. 44 (a)). The "suspended" inductor provides a higher self-resonance: for a 100 nH inductor, the self-resonant frequency increases from 800 MHz to 3 GHz [81]. Other micro-machining techniques consist of etching the silicon substrate underneath the structure, which lies on a 1-2 µm thick dielectric membrane, as shown in Fig. 44 (b). For a 1 nH spiral inductor layout, the self-resonant frequency increases from around 20 GHz to a maximum of

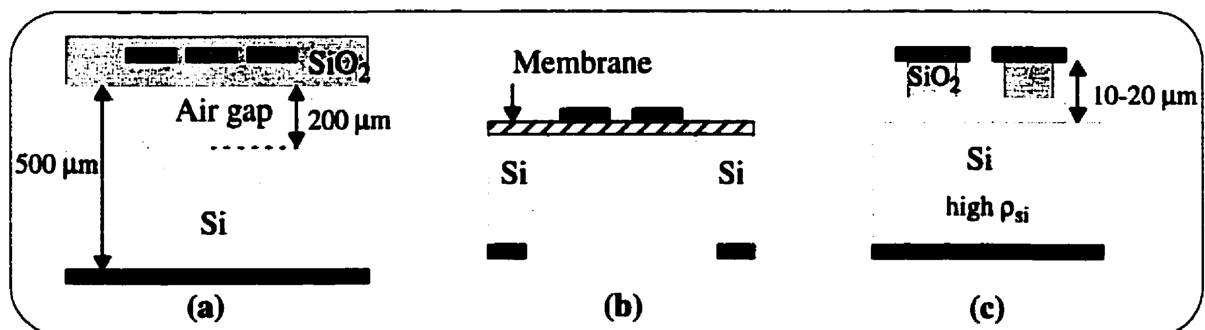


Fig. 44. Removal of substrate parasitics by **(a)** selective etching of the underlying silicon, **(b)** fabrication of a dielectric membrane, or **(c)** etching part of oxide and silicon layers.

70 GHz, after removing the silicon beneath the inductor, thus reducing the substrate capacitance C_p to 2-4 fF. Therefore, the Q for the inductor on a membrane is close to $\omega L/r$. For a 0.9 nH inductor, the Q was 20 at 4.3 GHz [83]. The results given above were obtained with an HRS, whereas the same trend is also obtained with a standard silicon process [84]. Etching the oxide layer and part of the high resistivity (10 kΩ-cm) silicon layer between the strip lines inside and outside the spiral inductor reduced the coupling and substrate parasitic capacitances (see Fig. 44 (c)). For an etch depth of 20 μm, the resonant frequency was nearly doubled, attaining a value of 32 GHz for a 2 nH inductor [85].

The disadvantages of an etched cavity beneath the inductor are the lack of long-term mechanical stability and a requirement for hermetic packages to prevent contamination of the silicon, which increases the overall cost. Moreover, low cost integration with other active devices on the same chip is difficult to achieve with a membrane. However, these techniques are useful for the millimeter-wave frequency range where a high inductor self-resonance is required.

4.3 Review of Inductor Chip Area Reduction

The inductor chip area can be reduced by choosing the optimum physical layout, that is, the strip width, the spacing between adjacent lines, the gap between opposing sets of coupled strips, the outer dimension of the spiral, and the number of turns.

Taking advantage of the additional metal layers provided by modern semiconductor processes, a multilevel spiral inductor can be designed, as shown in Fig. 45. The two spirals are connected with a via from the inner turn. The second spiral is wound beneath the upper spiral, from the center back to the second port. This configuration enhances the total inductance due to additional mutual inductive coupling from the parallel lower metal

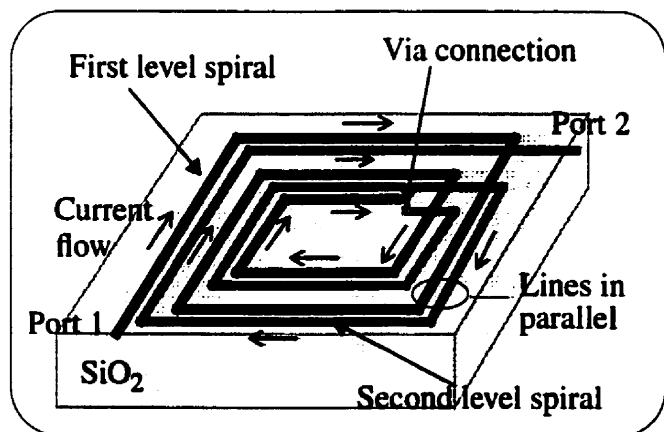


Fig. 45. Multilevel spiral inductor.

strips. To maintain a reasonable series resistance, the lower metals can be stacked. However, separation between the lowest metal layer and the oxide/silicon boundary results in severe degradation of the Q-factor, due to higher oxide and line-to-line coupling capacitances.

Table 4 compares the line parameters and Q-factors for two 4 turn inductors connected in series with a parallel connected spiral as in Fig. 45, for which the overall chip area was reduced by one half. Thus, for the same series resistance, the inductance increased by 70%, whereas the Q decreased by 35%. Resulting from the higher parasitic capacitances, the self-resonant frequency also decreased substantially. For an equal chip area as the parallel connected inductor, an 8 turn 9 nH inductor shows a better performance than the parallel inductor. Although the series resistance is almost double, the influence of the capacitive parasitics is less pronounced [12]. Therefore, this chip area reduction technique is useful for obtaining higher inductances, at the expense of higher parasitic capacitances which degrade the overall performance of the inductor.

Table 4. Comparisons with series and parallel connected inductors [12].

Inductor	N turns	L (nH)	r (Ω)	Q_{peak}	f_{peak} (GHz)	f_{sr} (GHz)
Series	4	5.2	5	10.4	2.4	18.3
Parallel	4	8.8	5	6.8	1	3.3
Single	8	9	9.5	9.5	1.8	9.1

4.4 Proposed Method

Inductive loads are widely used in RF circuits, such as amplifiers, oscillators and mixers. Circuit performance depend on the quality of the components used. These influence the circuit's linearity, total noise level, and power consumption. In the previous section, various Q-factor enhancement techniques were presented. Without altering the fabrication process, a new inductor design is proposed that is suitable for differential circuits (which are one of several existing RF design topologies).

4.4.1 Inductors for Differential Circuits

Differential circuits (e. g., the amplifier shown in Fig. 46) are used in transceiver designs. These circuits add components on the chip, i. e., they require twice the number of active and passive elements, but monolithic components on an integrated circuit can be added at almost no extra cost, compared with discrete components or hybrid MICs [87]. Differential circuits have the ability to reject common-mode disturbances, for which the layout must be exactly symmetrical, and, as shown in Fig. 47 (a), both pairs of inductors, L_d and L_s, must be carefully laid out (i.e., produce a physical layout), such that the currents in opposite groups of strips of the two inductors flow in the same direction. Here, the excitation of each inductor is "single-ended", that is, one terminal of the spiral is grounded by the common node connection of the voltage supply. Figure 47 (b) shows a new inductor design suitable for differential excitation, the symmetric spiral. Here, the voltages and currents at Port 1 and Port 2 are 180° out of phase. For example, the winding corresponding to 'inductor 1' has a positive voltage, whereas the winding of 'inductor 2' has a negative voltage. Therefore, for adjacent coupled strips in the same group, the voltages on

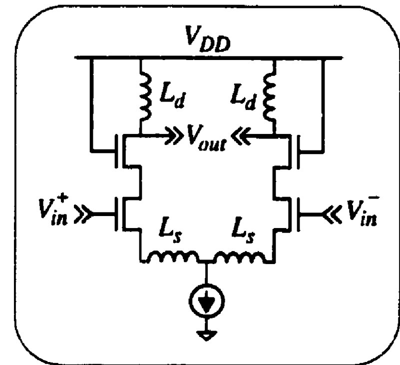


Fig. 46. Differential LNA [86].

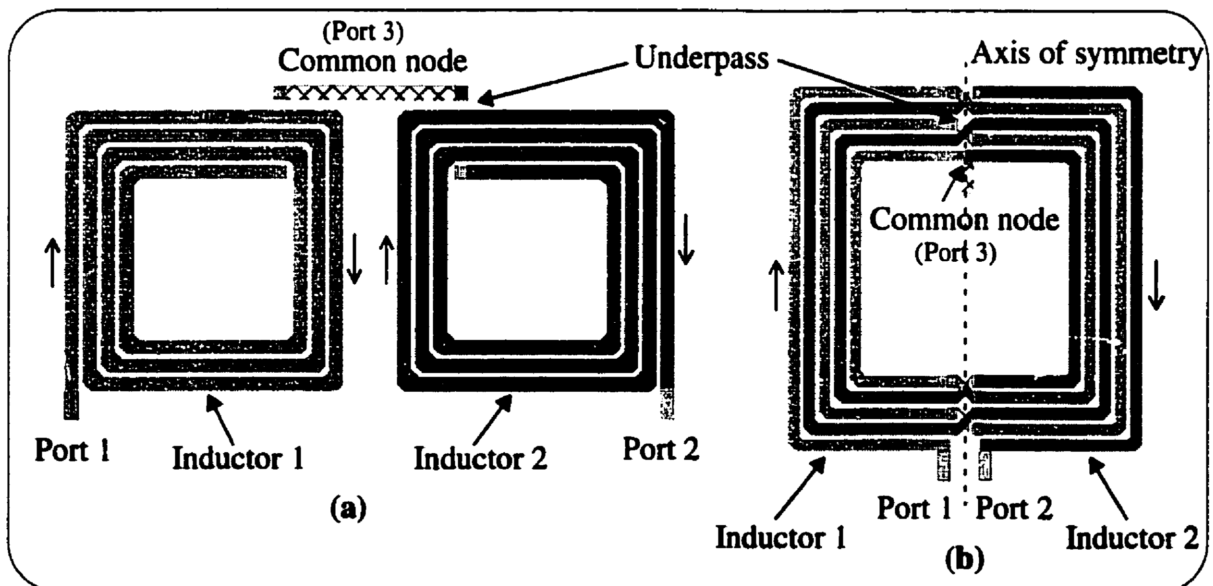


Fig. 47. (a) Two adjacent asymmetrical spiral inductors (b) Single symmetrical inductor for differential excitation.

each strip are out of phase, but the current flow is in the same direction. Whereas for each conventional inductor in Fig. 47 (a), the voltages on adjacent strips of the same group have a small phase lag between each other, and hence, inductors 1 and 2 cannot be differentially excited.

4.4.2. Asymmetrical vs. Symmetrical Inductors

A conventional inductor is wound into a spiral to reduce space and uses an underpass or crossover to the inner node to facilitate connections to other circuitry. The symmetrical inductor is designed by joining groups of coupled strips from one side of the axis of symmetry to the other, using underpasses. This idea was first applied to transformers for coupling both primary and secondary coils [88].

The symmetrical inductor layout has many advantages. Two separate spirals are replaced by a single coil, and the common node separates the spiral to form two equal inductances. Substrate parasitics are the same at either port. For a pair of asymmetric inductors (see Fig. 47 (a)), a finite spacing between both inductors must be maintained to reduce negative coupling; this is not an issue for symmetrical inductors. Moreover, a reduction in chip area results. The example in Fig. 47 shows two 4 nH conventional spiral inductors and an 8 nH symmetric inductor, for which a 35% area reduction results. Since both ports are adjacent, the symmetric inductor is suitable for the connection to active devices, such as transistors.

4.5 One-Port Excitation Theoretical Analysis

As an aid to qualitative understanding of the single-ended and differential one-port excitations, Fig. 48 illustrates the various currents flowing on the conductor and in the substrate of a microstrip line on silicon. Conduction currents are present on the line conductor as I_{cm}, and in the silicon substrate as I_{cs}. The displacement current I_d flows within the substrate layers to reach the ground plane. The difference between single-ended and differential excitations lies in the current return paths. In the differential case, the substrate currents return to the lower potential node. The physical interpretation of this phenomenon will be translated into an equivalent circuit.

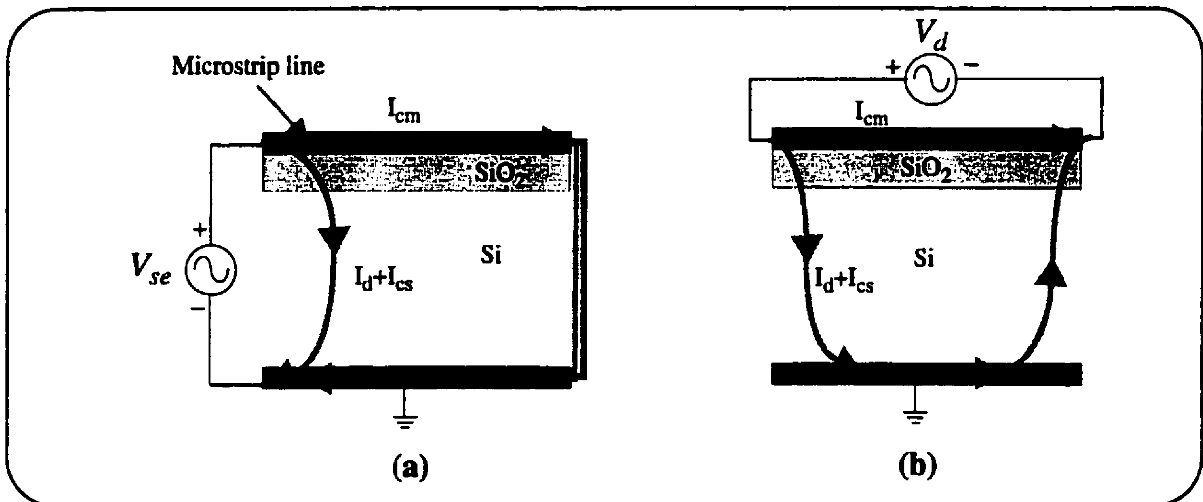


Fig. 48. Current paths for (**a**) single-ended and (**b**) differential connections.

For a simpler illustration of the different excitation models, the equivalent circuit of a single microstrip line, as given in Fig. 15, is analyzed with equivalent C_p and R_p for the substrate shunt parasitics.

For single-ended excitation, Port 2 is grounded and the inductor is connected as a one-port. The input impedance at Port 1, defined as Z_{se}, becomes a parallel combination of two components: Z_B, equivalent to the inductance and series dissipation (L and r), and Z_A equivalent to the shunt R_p-C_p parasitic elements, as illustrated in Fig. 49.

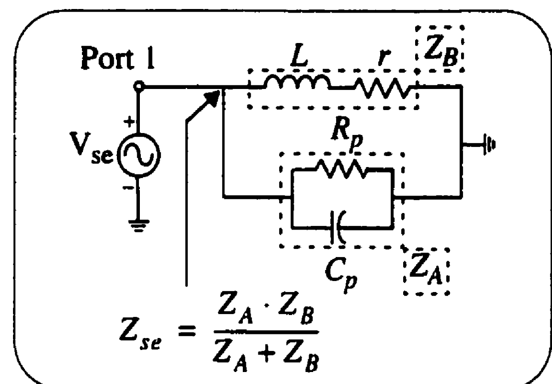


Fig. 49. Single-ended excitation model.

For a differential excitation, where the signal is applied between the two ports (Port 1 and Port 2), the input impedance Z_d is due to the parallel combination of $2Z_A$ and Z_B. Since the substrate parasitics are connected via the ground plane, the two shunt elements are now in series. The equivalent circuit is shown in Fig. 50.

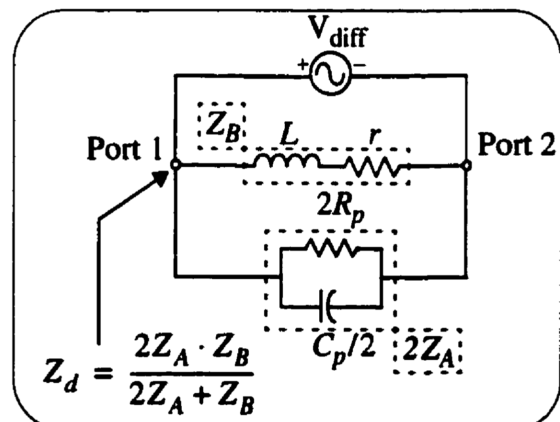


Fig. 50. Differential excitation model.

With a higher substrate shunt impedance for the differential case, Z_d approaches the value of Z_B, over a higher range of frequencies than for Z_{se}. In other words, at lower frequencies, the input impedance in either the shunt or the differential connections is approximately the same, but as the frequency increases, the substrate parasitics, C_p and R_p, come into play. For the differential excitation case, these parasitics have a higher impedance at a given frequency than in the single-ended connection. This reduces the real part and increases the reactive component of the input impedance. Therefore, the inductor Q is improved when driven differentially, and moreover, a wider operating bandwidth can be achieved at no extra processing cost.

4.6 Test Structure

A 5 turn square symmetric spiral inductor was fabricated and tested in order to verify the above predictions. The outer dimension *OD*, as shown in Fig. 51 (a), is 250 μm; the strip line is 8 μm wide, and the spacing *s* between conductors is 2.8 μm. The inner gap between opposite groups of coupled lines is approximately 150 μm, which minimizes negative mutual coupling, whereas the relatively narrow conductor width and spacing results in higher positive

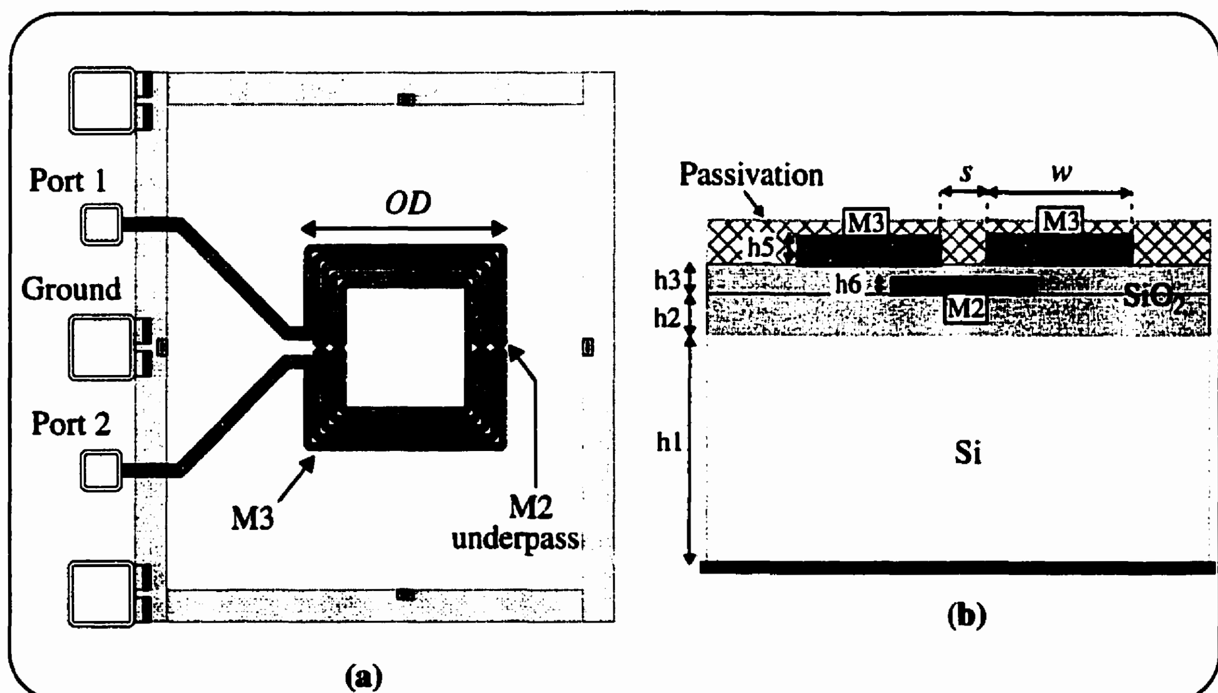


Fig. 51. (a) Inductor test structure layout. (b) Partial cross-sectional view of the inductor.

magnetic coupling and lower substrate capacitive parasitics. The inductor consists mainly of top metal (M3), and the second level metal (M2) is used for the underpasses. Both signal and ground pads are located on the same side; thus a set of probes with two adjacent RF contacts was used. A cross-sectional view of a portion of the structure is illustrated in Fig. 51 (b). (Properties of the substrate and the aluminum alloy metal for the fabrication process [89] are listed in Table 5.) For de-embedding purposes [90], short and open structures or "dummies" were also fabricated, as shown in Fig. 52.

Table 5. Substrate and metal parameters.

Parameter	Value
Oxide thickness over M2	h3 - h6 = 1.3 μm
Oxide thickness below M2	h2 = 3.61 μm
Silicon resistivity	ρ_{si} = 15 Ω-cm
Silicon thickness	h1 = 200 μm
Top metal M3 resistivity	ρ_S = 31 mΩ-μm
M3 thickness	h5 = 2.07 μm
M2 thickness	h6 = 0.84 μm

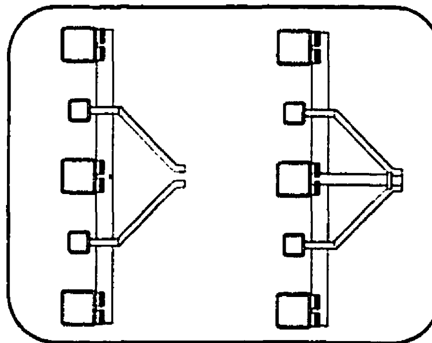


Fig. 52. Open and short dummies for the inductor in Fig. 51 (a).

4.7 Symmetric Inductor Modeling

The modeling procedure for the symmetric inductor follows that of Chapter 3. Figure 53 gives an example for N = 3. For the inductance value, Greenhouse's method is applied, considering six groups of coupled strips instead of four for a conventional spiral. This

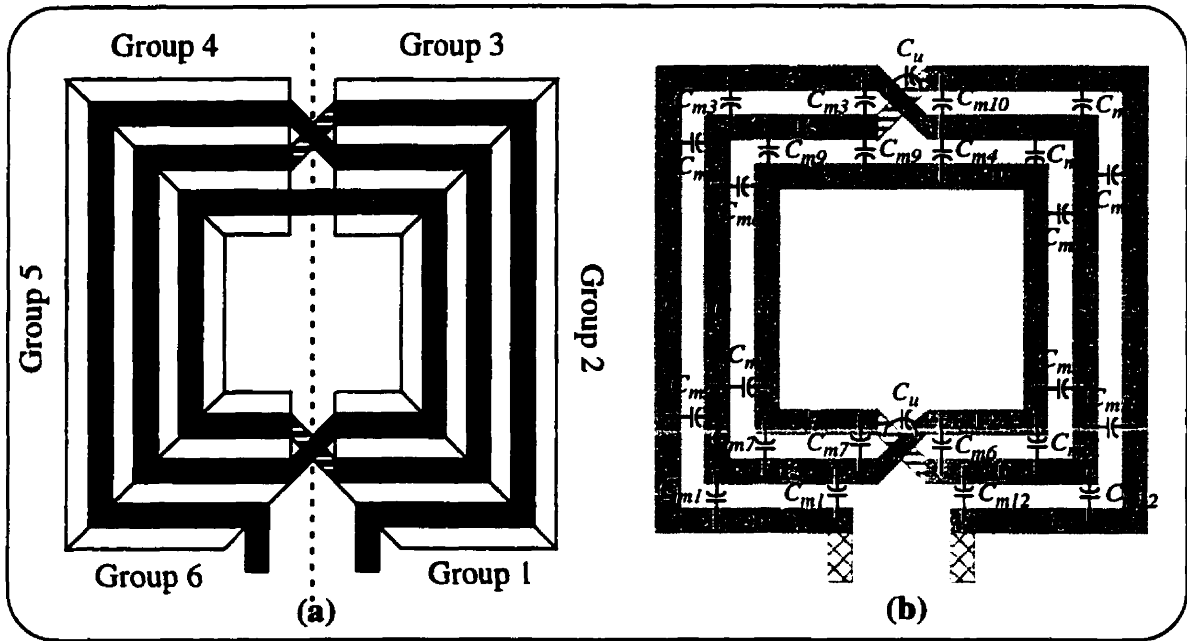


Fig. 53. 3 turn symmetric inductor modeling with (a) group sectioning and (b) line-to-line capacitances.

results in a total of 6N line segments, where N is always an integer. Positive mutual inductances are calculated for each group, whereas negative mutual inductances are obtained with respect to Group 2 and Group 5, Group 3 and Groups 1 and 6, and Group 4 and Groups 6 and 1, as shown in Fig. 53 (a). These mutual inductances are doubled since the inductor geometry is symmetric. Self-inductances for extra connections, i. e., the under and overpasses, which are not included in the groups, are added, but these are negligible (for a typical 20 μm long microstrip line, the inductance is less than 0.05 nH). R_{dc} takes into account the total length of the symmetric structure, including the underpasses, and the different metallization thicknesses and sheet resistivities. The total substrate capacitances C_{ox} and C_{si} are derived in the same manner as described in Section 3.2.3. The overall capacitance C_o is a combination of underpass capacitances C_u and interwinding capacitances. As shown in Fig. 53 (b), the combination differs from the asymmetric inductor, but the optimization method described in Chapter 3 is similarly applied to the symmetric inductor. The final model is also distributed into a maximum of 4N sections, defined in Section 3.2.5.

Table 6 summarizes the element values found for the 4 mm long structure shown in Fig. 51 (a). The optimized model of Fig. 54 compares well with the values obtained by fitting the simulated and measured data over a frequency range of 0.5 to 6 GHz (below self-

resonance). Since the inductor structure is symmetric, substrate parasitics should be the same at both ports.

Table 6. Lumped element values for the 5 turn symmetric inductor.

L (nH)	R_{dc} (Ω)	C_{ox} (fF)	C_{si} (fF)	R_{si} (Ω)	C_o (fF)
8	7.5	146	52.7	590	52

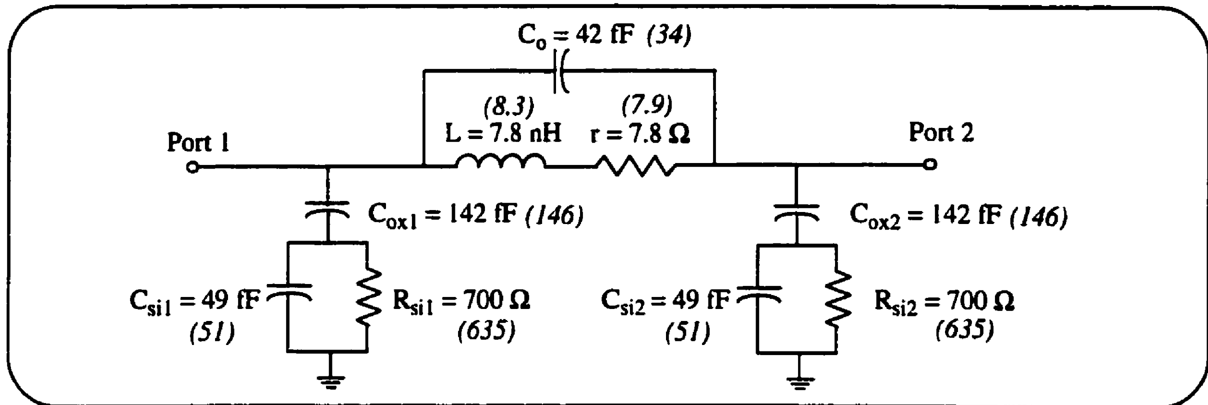


Fig. 54. Parameter fit circuit model for measured and *(simulated)* symmetric inductor.

4.8 Measurement Procedure

The symmetric inductor in Fig. 51 (a) was characterized experimentally from on-wafer measurements using a two-port vector network analyzer and Picoprobe 40A-GS-150-DUAL RF probes. The probes, manufactured by GGB Industries, consists of two signal-ground coaxial probes mounted on a single base, as illustrated in Fig. 55. The spacing between the ground G and signal S fingers is 150 μm [91].

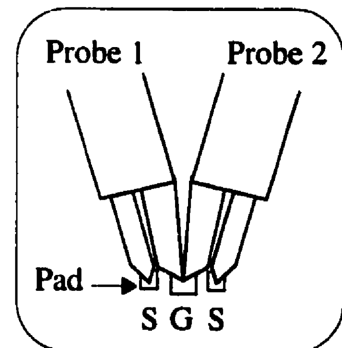


Fig. 55. Dual probes.

4.8.1 Calibration

First, the calibration specifications for the probes provided by the manufacturer are entered into the network analyzer. Second, an impedance standard substrate (ISS) [92] is used for the short, open, load, and thru (SOLT) full 2-port calibration. During calibration, Probe 1 of the set of dual probes is positioned on a holder opposite Probe 2. After calibration, it is moved back to the same probe head, as shown in Fig. 55. This extra step may add some error

to the measurements because the cable and probe are moved between calibration and measurement steps. However, this error can be considered negligible.

4.8.2 De-embedding Procedure

There are three measurement steps required to obtain de-embedded measurements for the DUT (device under test): 1) measure the device with its connections to the pads; 2) measure the open dummy structure; and 3) measure the short dummy structure [90]. The probe resistance is 0.25 Ω for the first use and can increase significantly after long-term use. This value can be determined by DC probing on the short structure whose DC resistance is obtained and is subtracted from the RF measurements at low frequencies.

The open dummy represents the substrate shunt parasitics, while the short dummy characterizes the inductance and resistance of the interconnect lines between the pads and the DUT. Figure 56 represents the DUT with its asscociated equivalent parasitics, which have to be removed from measurement data.

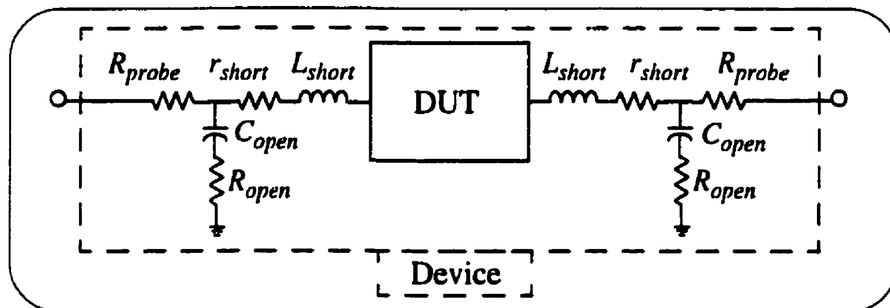


Fig. 56. Device under test with associated parasitics.

As presented in Fig. 57, the de-embedding steps are as follows:

1) Translate the S-parameters of the open and device structures into Y-parameters.

2) Subtract the open Y-parameters from the device and short Y-parameters.

3) Translate the resulting device Y-parameters into Z-parameters.

4) Subtract the short Z-parameters from the device Z-parameters.

5) Translate back the final DUT Z-parameters into S-parameters, if desired.

If a short dummy is not included, steps 3 and 4 can be eliminated [93]. As an alternative to de-embedding with a short dummy, the estimated series impedance of the connections can be removed in circuit simulators such as HP-EEsof Libra.

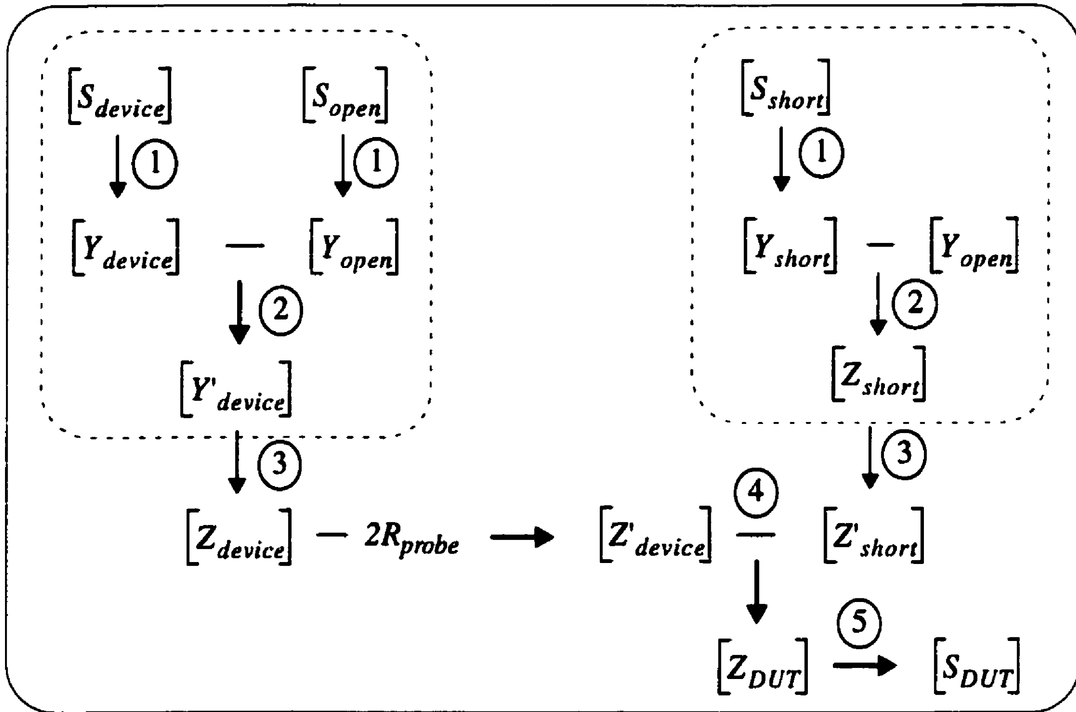


Fig. 57. Flowchart of de-embedding steps.

4.8.3 Single-ended vs. Differential Parameters

Single-ended and differential configurations are derived from the two-port measurements, as shown in Fig. 58. The one-port S-parameters are expressed as the two-port network equivalent incident and reflected signals, as described below:

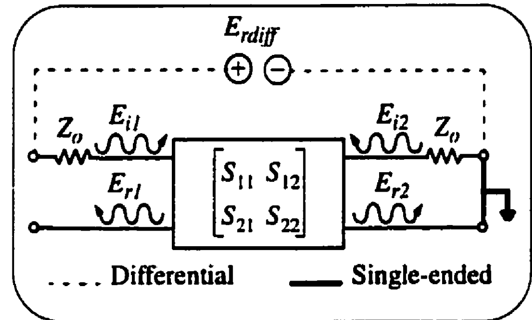


Fig. 58. Two-port S-matrix with both configurations.

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \tag{23}$$

where $a_k = \frac{E_{ik}}{\sqrt{Z_o}}$ and $b_k = \frac{E_{rk}}{\sqrt{Z_o}}$ with $k = 1, 2$; E_i and E_r are the incident and reflected waves, respectively, and Z_o is the system impedance (50 Ω). For the single-ended configuration, $E_{i2} + E_{r2} = 0$ or $a_2 = -b_2$ (with Port 2 grounded), and hence the following equation is obtained from (23) for the one-port S-parameter S_{se}:

$$S_{se} = S_{11} + \frac{S_{12}S_{21}}{1 + S_{22}}. \tag{24}$$

The difference between the first and second equations of (23) gives the differential signal, i.e., $E_{rdiff} = b_1 - b_2$. In this case, $E_{i1} + E_{i2} = 0$ or $a_1 = -a_2$, such that an equivalent incident signal $a = \frac{E_i}{2\sqrt{Z_o}}$ defines the differential one-port S-parameter S_d as

$$S_d = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2}. \tag{25}$$

The second approach consists in deriving the input impedance directly from the transformed 2-port Z-matrix (Fig. 59), which is related to the port voltages and currents by the following expressions:

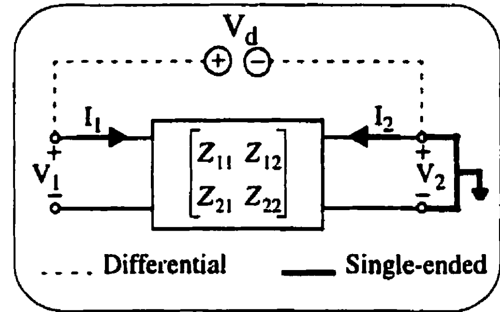


Fig. 59. Two-port Z-matrix with both configurations.

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \end{aligned}. \tag{26}$$

With Port 2 grounded, the single-ended configuration implies that $V_2 = 0$, so that the input impedance becomes

$$Z_{se} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}} = Z_o\left(\frac{1 + S_{se}}{1 - S_{se}}\right)\ (\Omega). \tag{27}$$

For the differential case, $V_d = V_1 - V_2$ is the resulting signal voltage, with $I_2 = -I_1$. Thus the input impedance is

$$Z_d = Z_{11} + Z_{22} - Z_{12} - Z_{21} = 2Z_o\left(\frac{1 + S_d}{1 - S_d}\right)\ (\Omega) \tag{28}$$

where $2Z_o$ is obtained from the differential system impedance.

4.9 Results

The two-port symmetric spiral inductor was simulated using HP-Momentum, for which the spacing between adjacent lines was taken as 3 µm instead of the 2.8 µm specified in the design. The structure was simulated from 500 MHz to 6 GHz in steps of 0.5 GHz.

Measurements performed on the HP 8753D network analyzer ranged from 10 MHz to 6 GHz, and those on the HP 8722C, from 500 MHz to 20 GHz. Measured and simulated structures were properly de-embedded with the open and short dummies. The probe resistance was estimated to be around 0.3 Ω. Three sets of measurements were performed with different calibrations. Calibrations A and B were done with the HP 8753D for which 4 and 11 test samples, respectively, were measured, and calibration C on the HP 8722C used 4 test samples.

4.9.1 Parasitics

With an estimated probe resistance of 0.3 Ω, measured and simulated short interconnections had a 250 pH inductance in series with a 0.1 to 0.4 Ω frequency dependent resistance. Theoretical values for L_{short} were found to be 220 pH and for r_{short}, 0.25 Ω. Shunt parasitic values at 2 GHz for the open structure are shown as histograms in Fig. 60. Depending on the calibration, different values were obtained. Simulated results gave a 51 fF capacitance in series with a 461 Ω resistance.

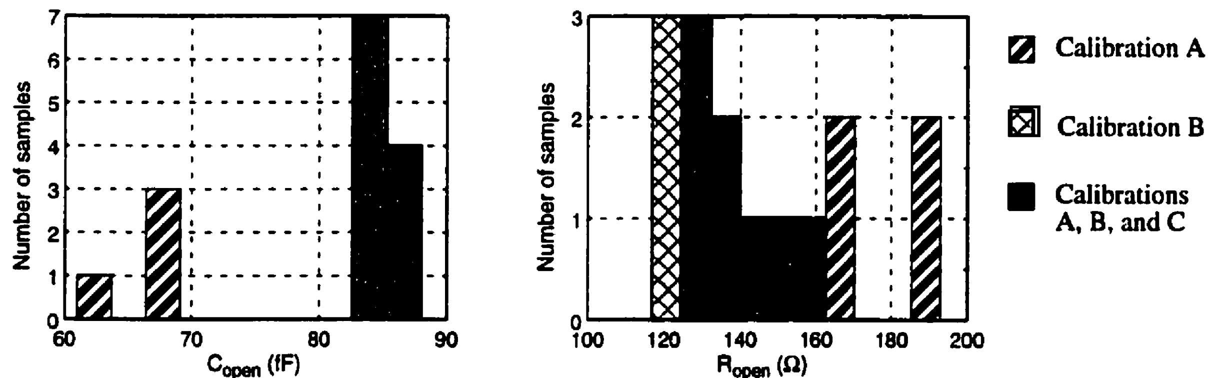


Fig. 60. Open dummy structure parasitic histograms over 15 samples.

4.9.2 Results and Discussion

Figure 61 (a) shows the measured inductance and series resistance of the spiral inductor structure after de-embedding. These values were taken at 500 MHz, for a low frequency parameter extraction from the input impedance. Inductance values are more sensitive to the accuracy of the calibration performed, whereas the resistance fluctuates between 7.3 Ω and 8.8 Ω. For repeatability comparisons, some measurements were done on the same inductor using different calibrations. These results show that the values depended on the calibration and not on the chip itself. Simulated results gave a total inductance of 8.3 nH

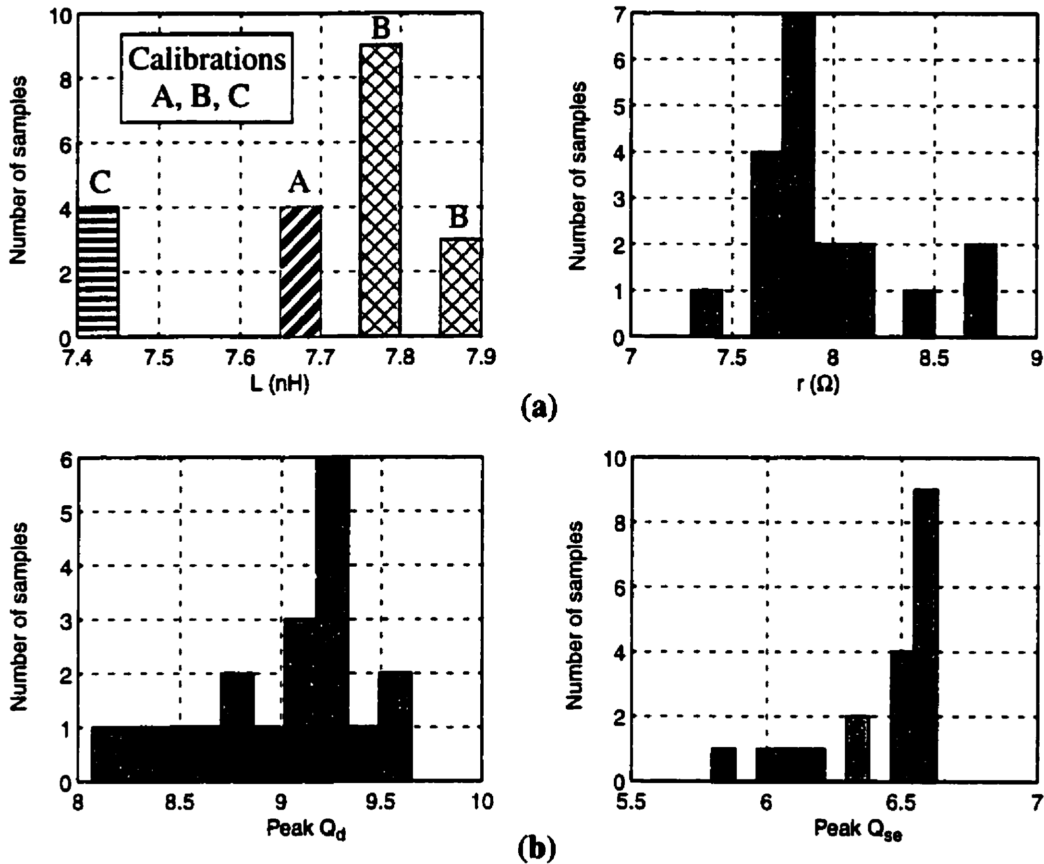


Fig. 61. Inductor structure histograms over 19 samples for **(a)** L and r at 500 MHz and **(b)** Q.

and a series resistance of 8.2 Ω. At a lower frequency (100 MHz), the average measured r was 7.3 Ω. Simulation gave 7.9 Ω while the DC resistance was 7.5 Ω. The inductance was approximately constant in the low frequency range (f < 1 GHz).

The Q-factors for the single-ended (Q_{se}) and differential (Q_d) configurations were derived from (7) using the appropriate input impedances. Fig. 61 (b) gives the peak Q values for each measured sample. Values of 9.3 and 6.6 for Q_d and Q_{se}, respectively, occurred with the greatest probability (30-50%). For subsequent discussions, a representative sample will be shown with the above Q values.

Figure 62 compares the line parameters obtained from measurement, full-wave EM simulation, and the new inductor model (Table 6). Analysis of these parameters helps to compare the overall performance of the inductor, considering information such as the Q-factor differences between simulated and measured data. The inductance curves are very similar, whereas the series resistances differ significantly at higher frequencies. The low frequency

substrate capacitance gives the oxide capacitance value. The measured data shows a large error in this range.

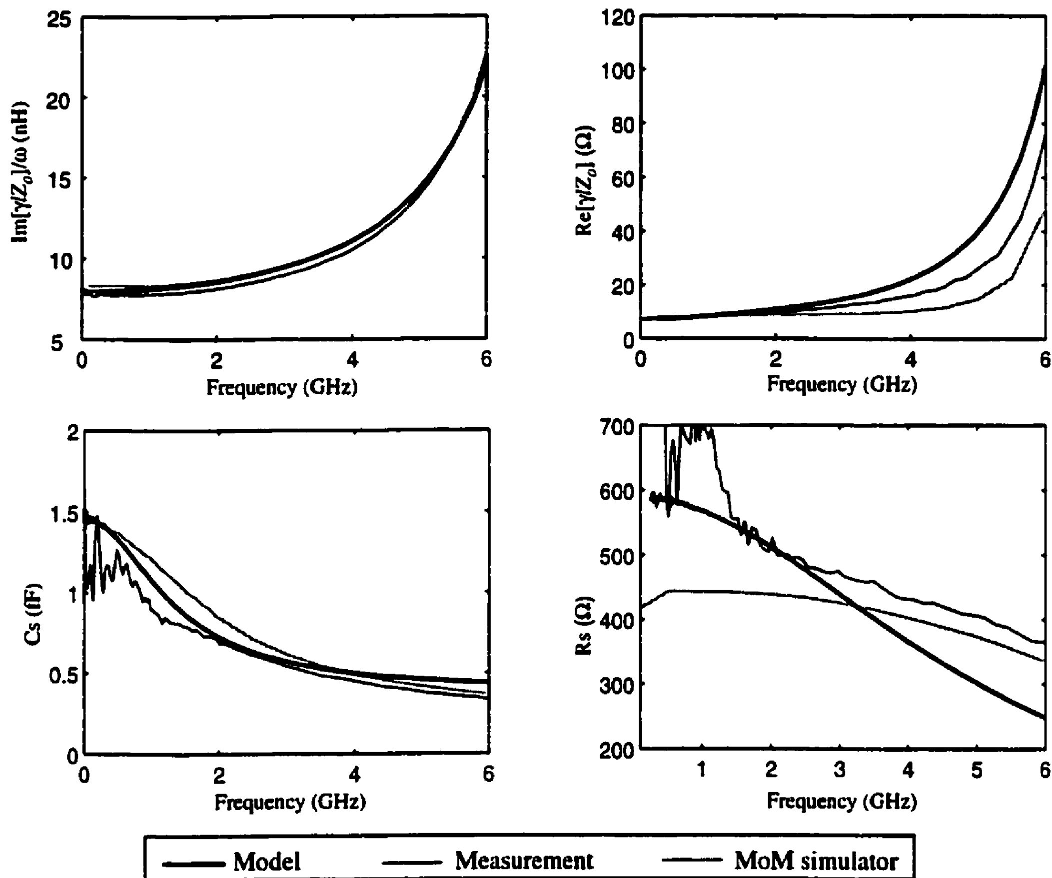


Fig. 62. Transmission line equivalent parameters for the 8 nH symmetric inductor.

A comparison between the experimental measurements, full-wave EM simulation, and the new inductor model for the input impedance and the Q-factor are shown in Figs. 63 and 64. At lower frequencies, the difference in Q between the differential and single-ended excitations is not significant (<1%) because the shunt capacitive parasitic components do not affect the low frequency input impedance. Hence, the two cases can be represented by a series L-r model. However, as the frequency increases, the difference between the input impedances becomes substantial: Z_d is much lower than Z_{se} by an increasing factor. This is caused by the lower substrate parasitics present in the differentially excited case, as previously described. As shown in Fig. 64, the difference between Q-factors in the differential and single-ended cases illustrates this point. The peak in the Q-factor is a result of the shunt parasitics resonating with

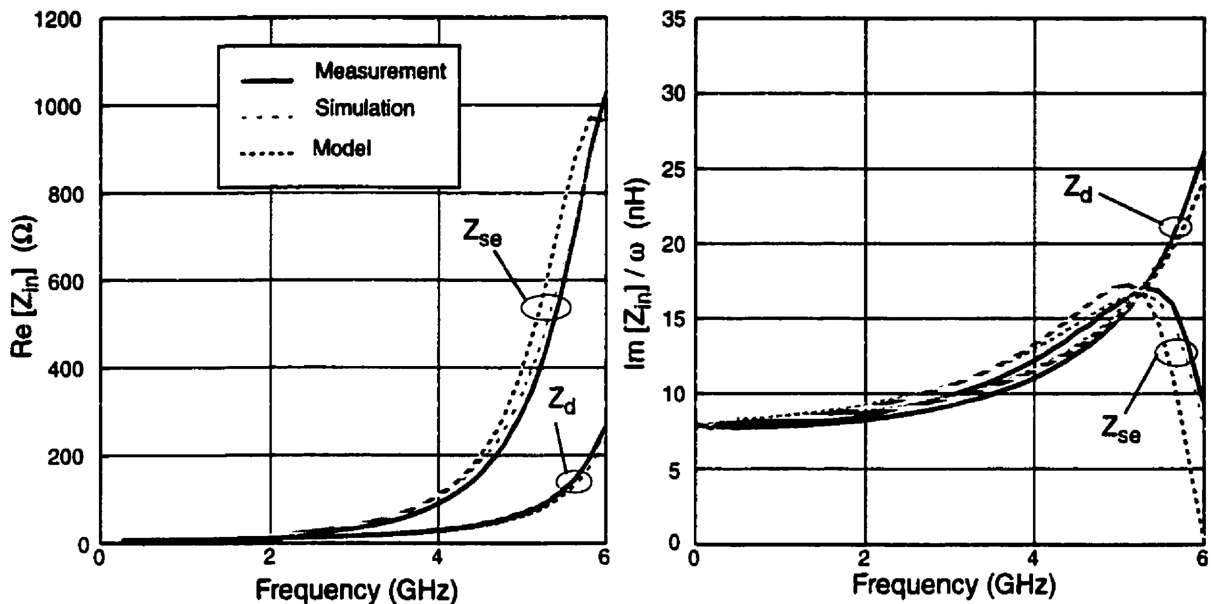


Fig. 63. Measured and simulated resistive and inductive parts of input impedances for single-ended and differential connections.

the inductance. Lower parasitics for differential excitation result in a higher peak Q-factor and broadening of the Q peak, when compared with the conventional single-ended connection.

Table 7. Peak Q-factor comparisons for single-ended and differential excitations.

Results	Q_{se} **(1.6 GHz)**	Q_d **(2.5 GHz)**	**% increase**
Measurement	6.6	9.3	41%
Simulation	6.6	10.3	56%
Model	5.9	8.7	47%

Table 7 gives the corresponding peak Qs for the single-ended and differential excitation cases. As seen in Fig. 62, the main difference between the model and the measurement values results from the change in oxide capacitance. Due to a lower series resistance and a higher low frequency inductance, the simulated data have the highest Q-factor. For the single-ended case, the simulated Q_{se} value is compensated for by the lower measured substrate capacitance, and hence measured and simulated Qs have the same value. The peak Q occurs at frequencies of 1.6 GHz and 2.5 GHz for the single-ended and

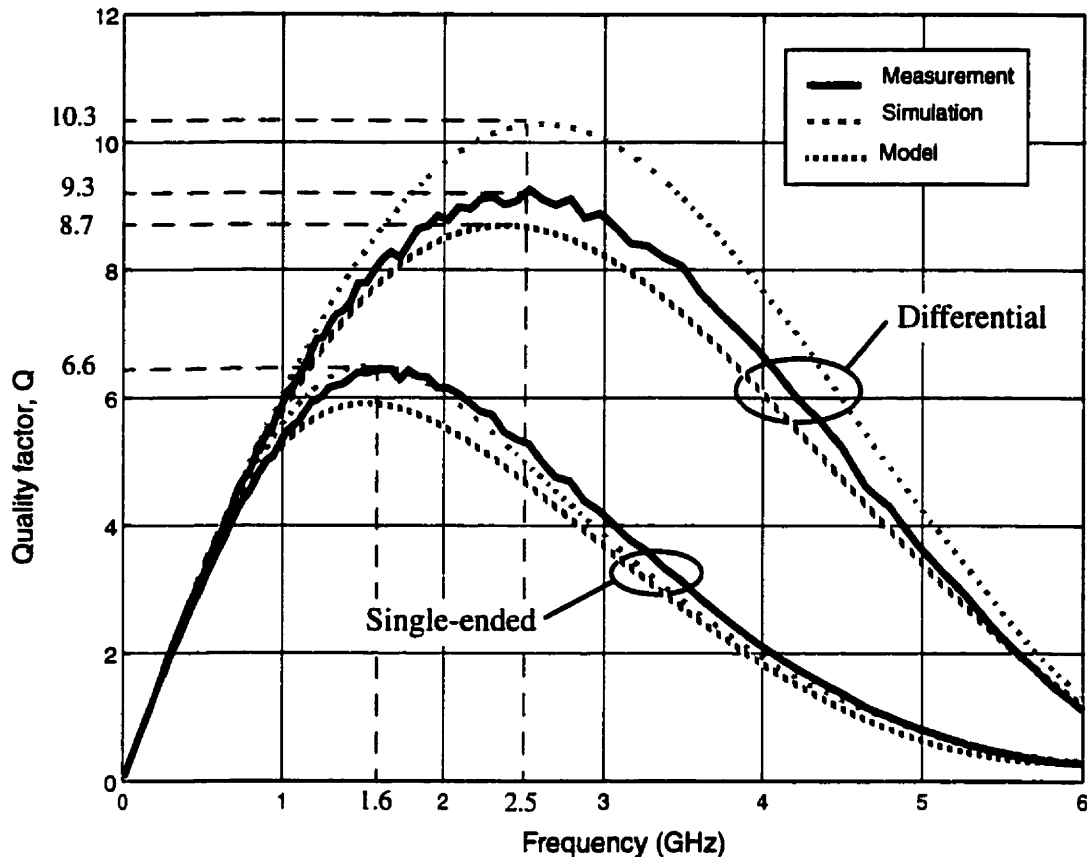


Fig. 64. Measured and simulated Q-factors for single-ended and differential excitations.

differential excitations, respectively, which results in a 56% increase. As seen from Table 7, a 50% increase in the peak Q can be realized without modification to the fabrication process. Achieving a comparable Q value in the single-ended connection would require approximately a twofold increase in the top metal thickness. (For a 4 μm metal, the resulting Q for a single-ended excitation would be 8.5 (simulated) and 9.2 (modeled) at 1.2 GHz.) At frequencies beyond the peak, an increase of greater than 50% can be achieved. It should be noted that because they are greater in magnitude, Q values for the differential case are much more sensitive to slight variations in the measured or simulated input impedance. Thus, near the peak Q for the differential case, the relative effect of an error in either the measurement or simulation is more pronounced. Because of lower capacitive parasitics, the inductor self-resonance is increased from 6.3 GHz for the single-ended case, to 7.1 GHz for the differential excitation.

4.9.3 Sources of Error

As previously discussed, calibration, de-embedding structure parasitics, and probe contact resistance are all sources of error that can alter the measured DUT parameter values. Inaccuracies due to imperfections in the connectors, cables, temperature and frequency drifts within the network analyzer, calibration, and test devices add to the random measurement errors [94].

Other errors are caused by variations in the fabrication process. An important factor is the top metal thickness, which can vary within ±10%. After a 10% increase in the metal thickness, R_{dc} is 6.8 Ω, and the simulated series resistance becomes 7.6 Ω at 500 MHz, compared with the measured value of 7.7 Ω. For a submicron IC process, the metal lines are defined photolithographically to within 0.1 μm, which has a negligible effect on the line inductance and resistance. Simulations were performed for a ±0.2 μm strip width variation, and no significant changes (< 2% in the peak Q) were observed. For a ± 1 μm change in oxide thickness and a ±50% change in silicon resistivity, simulations also predict a ±5% variation in the self-resonant frequency and in the peak Q.

Inaccuracies in the electromagnetic simulation are mainly caused by improper meshing of the structure which is a contributing factor to an approximation of the actual device. Moreover, present simulators do not account for variations in temperature of the metal in a spiral inductor.

4.9.4 Optimized Equivalent Circuit Models

Figure 65 shows a lumped-element model for the symmetric inductor that was fit numerically over a broad band of frequencies (0.5-6 GHz) for both the single-ended and differential connections. Tables 8 and 9 give the element values for measured and simulated results. Here, L is the low frequency inductance, and r is the series resistance at

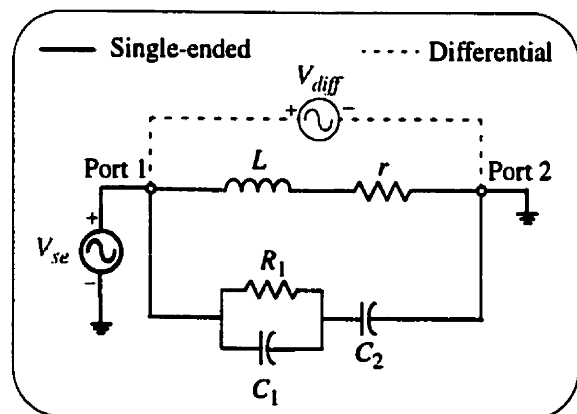


Fig. 65. Optimized equivalent circuit model for both configurations.

500 MHz.

Table 8. L and r values for Fig. 65.

Elements	Measured	Simulated	Modeled
L (nH)	7.8	8.3	8
r (Ω)	7.8	8.2	7.7

Table 9. Substrate parasitic parameters for single-ended and differential excitations.

	Elements	Single-ended	Differential	Fraction*
Measurement	R_1 (Ω)	358	1000	2.8 times
	C_1 (fF)	135	85	53%
	C_2 (fF)	162	75	46%
Simulation	R_1 (Ω)	358	1000	2.8 times
	C_1 (fF)	135	95	70%
	C_2 (fF)	162	62	38%
Model	R_1 (Ω)	500	1200	2.4 times
	C_1 (fF)	135	80	59%
	C_2 (fF)	210	80	38%

* Fraction from differential over single-ended component values

As seen from Table 9, if both single-ended and differential equivalent parameter values are compared, the resistive element is more than twice as high, and the shunt capacitances are 40-60% of those in the single-ended case. The modified values for the lumped element models differ from the equivalent circuits shown in Figs. 49 and 50 due to the distributed nature of the actual inductor, which cannot be modeled accurately by a single lumped-element section for both one and two-port configurations. The model proposed in Fig. 65 is an approximation for which the parasitic values do not represent the actual substrate shunt elements C_{ox}, C_{si}, and R_{si}.

4.9.5 Comparisons with the Literature

In Table 10, the symmetric spiral inductor is compared with other Q enhancement techniques previously described in Section 4.2. The inductor in a differential connection not

only has a higher Q-factor, but also can be implemented in all of the aforementioned technologies to further enhance the overall Q and obtain an even broader bandwidth.

Table 10. Comparisons of published references with the differential symmetric inductor.

Inductor type	Reference	ρ_{si} (Ω-cm)	t_M (μm)	L (nH)	Q_{peak}
1-level metal	Long [25]	10	1-3	1.88	6-10 @ 4 GHz
2 stacked metals	Park [80]	2 k	2	13	12 @ 3 GHz
3 stacked metals	Burghartz [77]	12	4.3	2.2	16 @ 2 GHz
Ground shield	Yue [29]	10-20	2	8	7.2 @ 1.5 GHz
Membrane	Chi [83]	2 k	1 (Au)	0.9 1.2	20 @ 4.3 GHz f_{sr}: 70 GHz
Etched oxide/Si	Rieh [85]	10 k		2	f_{sr}: 30 GHz
Differential Single-ended	Danesh / Long	15	2	8	9.3 @ 2.5 GHz 6.6 @ 1.6 GHz

4.10 Application

This section describes a circuit application incorporating monolithic inductors. Inductors can be used as tuned loads or feedback elements in differential circuits such as amplifiers, oscillators, and mixers.

For the purpose of this thesis, the 8 nH symmetric inductor will be incorporated into an oscillator designed for the 2.4-2.48 GHz ISM band WLAN market. The intermediate frequency IF for this application is specified at around 350 MHz. Therefore, a local oscillation frequency of 2.05 to 2.1 GHz is required. First, a Colpitts oscillator is used to show the implementation of the inductor in a single-ended connection. The oscillator performance is compared using measured and simulated data, and the new inductor model. Second, a differential version of the Colpitts as a cross-coupled oscillator will illustrate the advantages of the symmetric inductor over the integration of two identical asymmetric inductors.

4.10.1 Oscillator Design

For an oscillation to occur, a resonator, consisting of an inductor in shunt with a capacitor (and their associated parasitics), is connected to an active circuit, as shown in Fig. 66. For sustained oscillation, the real part of the impedance seen looking into the active

circuitry must be a negative resistance -R that is equal to or less than the R_{eq} of the resonator. The frequency of oscillation, determined by the resonance frequency of the *LC* tank, is given approximately as

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{eq} \cdot C_{eq}}} \text{ (Hz)}. \quad (29)$$

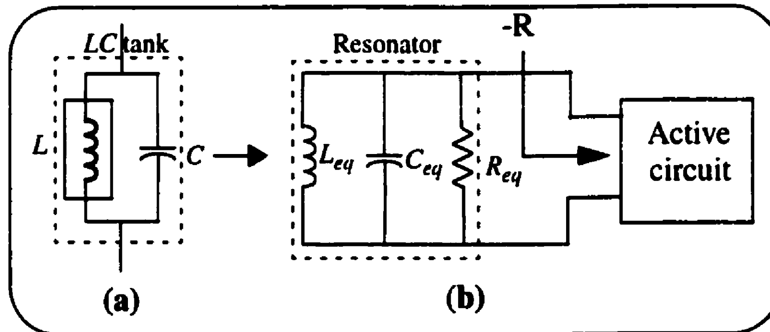


Fig. 66. (a) *LC* tank and (b) equivalent resonator in a one-port oscillator.

4.10.2 Colpitts Oscillator

The Colpitts oscillator is the most commonly used design because only one inductor is needed. Moreover, incorporating one active device into the circuit minimizes the noise sources. The Colpitts oscillator shown in Fig. 67 uses collector to emitter feedback. At

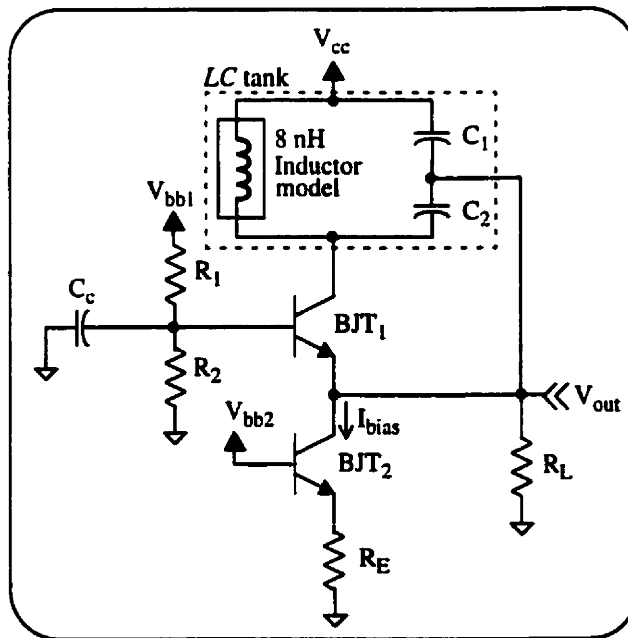


Fig. 67. Colpitts oscillator circuit.

resonance, the impedance of the resonator is real. The total phase shift of the signal fed back from the collector to the emitter is zero. The *LC* tank shown in Fig. 67 consists of an 8 nH symmetric inductor in parallel with C_1 and C_2 in series. Here, R_L is the load due to another circuit such as a mixer in a wireless transceiver, and BJT_2 provides the bias current for the oscillator.

a) Operating Points

With a 3 V supply, the DC voltage at the collector of BJT_1 is also 3 V. For transistor BJT_2 to be in the forward active region, its collector voltage must be higher than 0.9 V because the base-emitter voltage V_{be} is approximately 0.9 V. The voltage at the base of BJT_2 V_{bb2} is $V_{be}+I_{bias}R_E$. Therefore, the voltage at the base of BJT_1 should be between 1.8 V and 3 V, depending on the values of I_{bias} and R_E.

For an oscillation to occur at 2.1 GHz with an 8 nH inductor, C_{eq} must be equal to 0.72 pF, given by (29). However, because of added parasitic capacitances introduced by the monolithic inductor, a lower C_{eq} must be chosen. It has been shown that the best phase noise performance is obtained for the Colpitts with the ratio C_2/C_1 equal to 4 [95]. Table 11 gives the final component and voltage source values. A current bias I_{bias} of 0.68 mA results, such that the current flowing into BJT_1 is 1.13 mA.

Table 11. Element and source values for the Colpitts oscillator.

C_1	C_2	R_L	R_E	R_1	R_2	C_c	V_{cc}	V_{bb1}	V_{bb2}
0.6 pF	2.4 pF	2 kΩ	200 Ω	1.5 kΩ	2.5 kΩ	10 μF	3 V	3 V	0.95 V

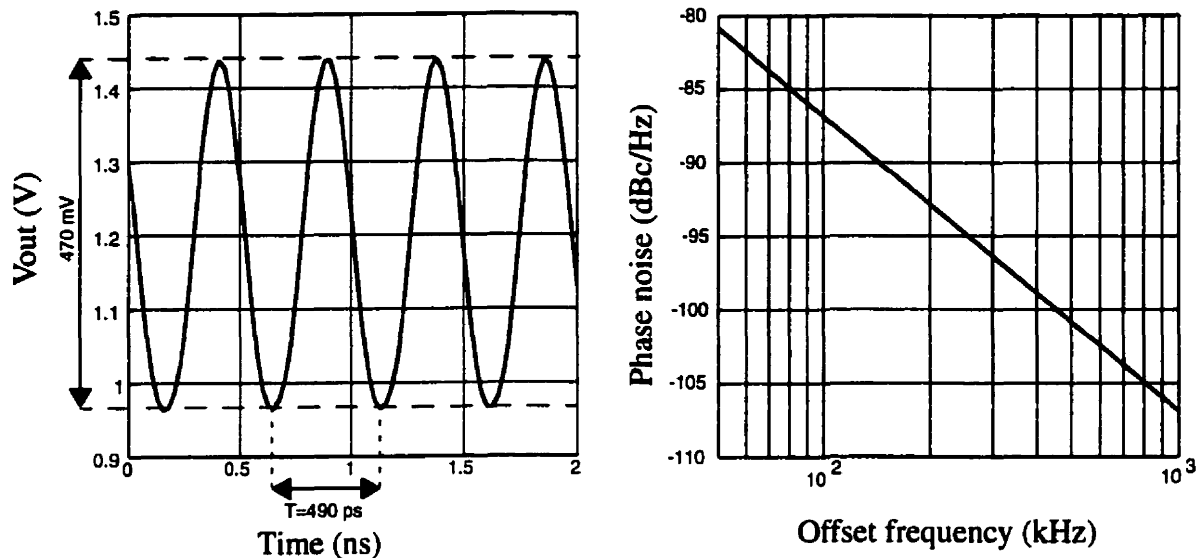


Fig. 68. Output oscillating voltage and phase noise for the Colpitts shown in Fig. 67.

b) Results

The 8 nH symmetric inductor model presented in Section 4.7 was used for electrical simulation of the oscillator circuit. Both HSPICE and HP-ADS circuit simulators were used for transient and frequency harmonic analysis, respectively. R_{eq} of the resonator is approximately 770 Ω, which is higher than the negative resistance -R of -185 Ω. Figure 68 shows the output voltage and the phase noise of the Colpitts design for the parameters listed in Table 11. The output voltage swing is around 470 mV, which is close to a typical design specification for radio applications. The total phase noise is -106.9 dBc/Hz at a 1 MHz offset frequency. The oscillation frequency is found to be 2.057 GHz. The total output power P_{out} is -2.6 dBm, and the third harmonic power is -38.4 dBm. The overall performance of the Colpitts design was also simulated using the compact models for the inductor (see Fig. 65) obtained from measurement, and the full-wave EM simulation. Oscillation frequency, output voltage swing, and phase noise are all within 1% of each other, which demonstrates the validity of the inductor model proposed in Chapter 3 of this thesis.

4.10.3 Cross-coupled Oscillator

As shown in Fig. 69, the Colpitts oscillator circuit was also designed using two transistors in a symmetric configuration. This cross-coupled design is a fully differential circuit. Although there is an increase in the number of noise sources due to the two transistors, this circuit has the advantages of common-mode power supply noise rejection, lower

harmonic generation, and higher output voltage swing. The resonator associated with BJT_1 consists of L_1, C_3, and C_1. Capacitors C_1 and C_2 provide regenerative feedback from the output to the base of BJT_1 and BJT_2 [96].

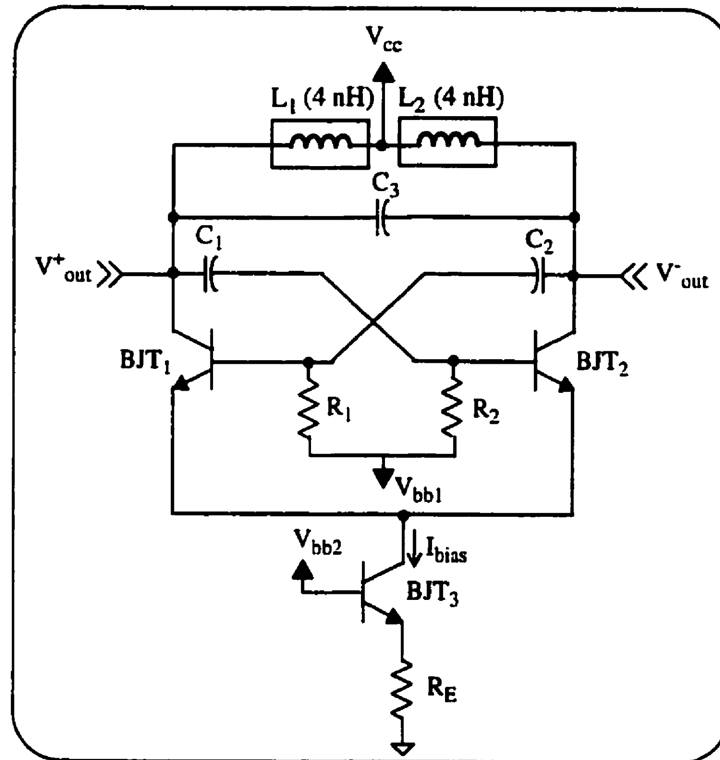


Fig. 69. Cross-coupled oscillator circuit.

a) Operating Points

The supply voltage V_{cc} is chosen to be 3 V for this design. In the forward active region of BJTs 1 and 2, V_{bb1} must be less than V_{cc}, but greater than the voltage at the collector of $BJT_3 + V_{be\ 1,2}$. The *LC* tank consists of L_1 and $2C_3$. For a resonance to occur at 2.1 GHz, C_3 should be approximately 0.72 pF, but due to the effect of C_1 in the feedback path, C_3 must be reduced in value. R_1 and R_2 must be large to isolate the voltages at the bases of BJT_1 and BJT_2 from RF signals. The bias current for each transistor BJT_1 and BJT_2 has been chosen to be the same as in the Colpitts example. Table 12 summarizes the final component values.

Table 12. Component values for the cross-coupled oscillator.

C_1	C_2	C_3	R_1	R_2	R_E	V_{cc}	V_{bb1}	V_{bb2}
1 pF	1 pF	0.6 pF	5 kΩ	5 kΩ	65 Ω	3 V	2.5 V	1 V

b) Results

The cross-coupled oscillator performance is compared for two different spiral inductor configurations. As shown in Fig. 47, one design incorporates the two 4 nH conventional spiral inductors, and the other, a single 8 nH symmetric inductor. Characteristics of the asymmetric 4 nH spirals and the 8 nH symmetric inductor are given in Table 13. The process parameters of Table 5 were assumed for both inductors. The spacing between the two 4 nH adjacent spirals is assumed to be much greater than 40 μm, so that coupling between the inductors is minimized. A model for the 4 nH conventional spiral was determined. The 8 nH symmetric inductor was excited differentially whereas the two 4 nH conventional spirals were each connected in the single-ended configuration, as described in Section 4.4.1.

Table 13. Comparisons between 8 nH symmetric and 4 nH conventional inductors.

Characteristics	8 nH symmetric	4 nH asymmetric
OD / N	250 μm / 5	210 μm / 3.5
Inner gap	150 μm	140 μm
Total length	4 mm	2.44 mm
R_{dc}	7.5 Ω	4.56 Ω
Q @ 2.1 GHz	8.6	7.5

For the differential output $-R$ of -290 Ω in the 2 GHz range, R_{eq} of the 8 nH symmetric inductor is 2 kΩ, whereas for the 4 nH asymmetric inductor, it is 800 Ω. Figure 70 shows the differential output voltage and the total phase noise for electrical simulations of the differential oscillator using both inductor configurations. Table 14 compares the performance of the oscillator with each inductor configuration.

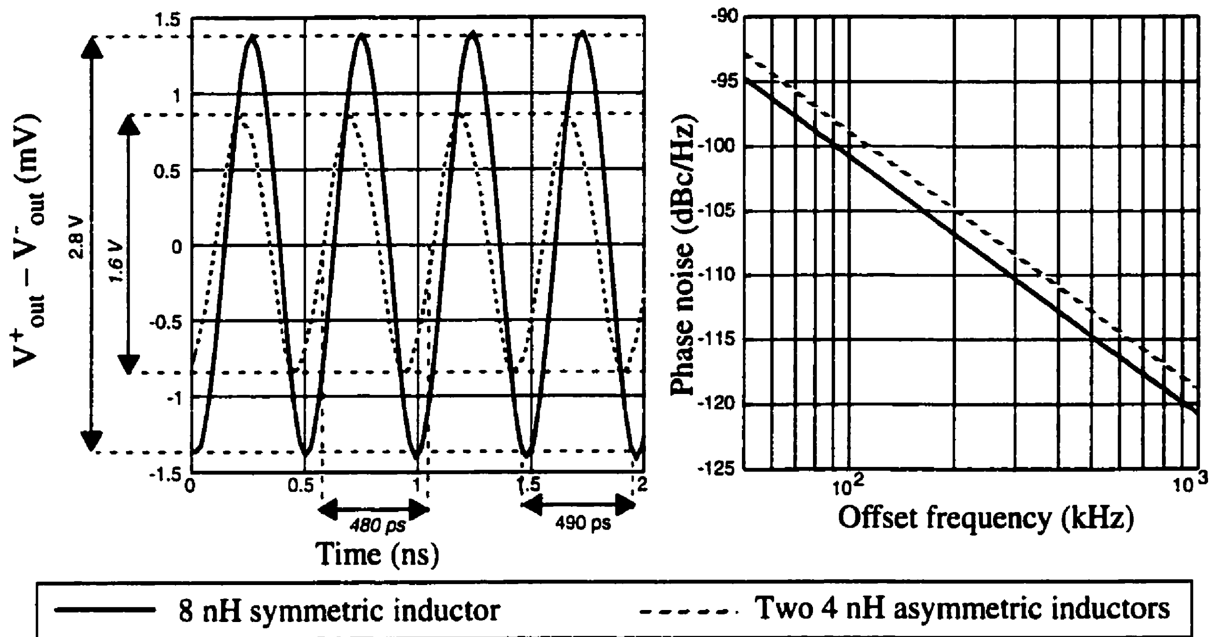


Fig. 70. Differential output voltage oscillation and phase noise for the 8 nH symmetric inductor and two 4 nH asymmetric spiral inductors.

Table 14. Comparison of cross-coupled oscillator performance for both inductors.

Parameters	8 nH symmetric	4 nH asymmetric
f_{osc} (GHz)	2.061	2.114
V_{out} swing (V)	2.8	1.6
Phase noise (dBc/Hz) @ 1 MHz	-120.7	-118.9
P_{out} (dBm)	7.1	5.4
3rd harmonic P_{out} (dBm)	-30.9	-29.1

Due to the differences between the series resistance and substrate parasitics for the conventional spiral and the symmetric spiral, a lower output swing and a poorer phase noise result. The optimized compact models shown in Fig. 65 for the measured and simulated symmetric inductors compare within 3% for the overall oscillator performances.

Chip area is another important issue. As mentioned in Section 4.4.2; the symmetric inductor reduces the total area by 35% when compared with two 4 nH conventional inductors with a 40 μm spacing. A differential oscillator, as in [97], could be redesigned using a single

symmetric inductor to realize a substantial reduction in the overall chip area.

Thus, a symmetric inductor can be excited differentially, and it has been shown that this results in a higher peak Q-factor. Moreover, a single symmetric inductor can replace two conventional single-ended spirals to improve electrical performance and save chip area. The oscillator described in this chapter performed better with the single symmetric inductor than with two asymmetric spirals.

Chapter 5

CONCLUSIONS

This thesis examines single and coupled microstrip transmission lines on silicon dioxide/silicon substrates and the spiral microstrip inductor. A basic understanding of the electrical behaviour of the microstrip line required representations of the electromagnetic field propagation. Current silicon processes have low to medium resistivities which considerably influence the behaviour of the fields in the substrate, and hence, the characteristics of the strip line. These propagation modes are defined by the quasi-TEM, slow-wave, and skin-effect modes. For typical bipolar/CMOS processes, the slow-wave mode and transitions from the slow-wave to quasi-TEM or skin-effect mode regions are the most common in the low GHz frequency range.

Lumped element equivalent circuits are required to model microstrip structures in circuit simulators such as SPICE. The model used in this thesis is a π-type lumped element equivalent circuit. Closed-form expressions for the inductance and series conductor resistance are utilized in the model, in which the inductance is considered to be a constant, and the series resistance is a frequency dependent parameter that takes the skin-effect and the conductive silicon effect into account. For deriving the substrate parasitics, that is, oxide and silicon capacitances, and conductive substrate resistance, several methods have been proposed in the literature, most of which use static approximations. The single microstrip line model agreed to within 5% of the simulated Q-factor results. The influences of all the lumped elements with respect to the substrate resistivity and line widths were discussed.

Analysis of single microstrip lines provided the underlying basis upon which a model for spiral inductors was developed. Several inductor modeling techniques have been previously reported in literature, however, in this thesis, a simpler method was presented. This inductor model extends the principles of the single microstrip line model to groups of multiple coupled lines that form a spiral inductor. Transmission line parameters and the resulting inductor Q-factor compared well with the measured data for conventional spirals fabricated in various processes for a range of physical layouts. Moreover, this model can be easily integrated into an RF circuit simulator.

Symmetric differential circuits are one of the existing topologies used in amplifiers, mixers, and oscillators that implement spiral inductors. Current differential circuits use two spiral inductors placed adjacent to each other in the physical layout. A single symmetric inductor can replace both conventional asymmetric spirals in a differential connection. The total chip area is reduced when a symmetric circuit layout is used. Moreover, the symmetric inductor geometry is better suited for interconnection with other components, such as transistors, which are usually smaller in size.

The primary benefit of differentially excited inductors is that they are less affected by substrate parasitics. Therefore, resulting Q-factors are higher than in the single-ended case. For a 5 turn, 8 nH symmetric inductor, it was shown that the peak Q increases by 50% and even more after the peak frequency. The inductor self-resonant frequency also increases by about 10%, and a broader operating bandwidth for the differentially excited inductor is achieved. A model for the symmetric inductor, based on the conventional spiral inductor model, was also developed. The symmetric inductor models were validated using measurements and simulations for which the Q-factors agreed to within 10%. Enhancement of the inductor Q is obtained without modification of the process parameters. However, to achieve better circuit performance, techniques such as metal stacking and multilevel spiral designs can be applied to the symmetric inductor. Moreover, performance improvement in differentially excited inductors was demonstrated for a production silicon technology, and this technique is equally applicable to other substrates, such as GaAs.

Finally, a single-ended and a differential Colpitts oscillator were designed for the 2 GHz range to demonstrate the application of the inductor models. The single-ended Colpitts oscillator used the symmetric inductor in a single-ended connection. For the differential oscillator, two kinds of differentially excited inductor configurations were simulated, the 8 nH symmetric inductor and a series connection of two identical 4 nH conventional spirals. It was shown that the symmetric inductor yields better oscillator performance, that is, better phase noise and higher output voltage swing, as well as a chip area reduction.

Contributions. The contributions of this thesis are:

1) A new spiral inductor model for silicon technology, based on the compact model representation of a spiral inductor, which enhances the computational efficiency;

2) A parameter extraction technique that is obtained directly from the layout geometry and fabrication process specifications, which includes:

   a) A series resistance expression due to metallization that takes into account the conduction current distribution in the silicon substrate;

   b) A new substrate capacitance extraction method;

   c) An overall line-to-line capacitance which is a combination of the interwinding and underpass capacitances;

3) A new symmetric inductor design that is suitable for differential circuits;

4) An analysis of differentially excited microstrip structures;

5) An inductor Q-factor enhancement of 50% or more where the Q peaks and for frequencies beyond the peak;

6) A wider operating bandwidth for differential circuits;

7) The replacement of a pair of conventional asymmetric inductors by a symmetric inductor, which reduces the total chip area of the circuit.

REFERENCES

[1] A. A. Abidi, "Low-Power Radio-Frequency IC's for Portable Communications", *Proceedings of the IEEE*, Vol. 83, No. 4, April 1995, pp. 544-569.

[2] R. A. Pucel, "Design Considerations for Monolithic Microwave Circuits", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 29, No. 6, June 1981, pp. 513-534.

[3] H. Sobol, "Applications of Integrated Circuit Technology to Microwave Frequencies", *Proceedings of the IEEE*, Vol. 59, No. 8, August 1981, pp. 1200-1211.

[4] N. M. Nguyen and R. G. Meyer, "Si IC-Compatible Inductors and LC Passive Filters", *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 4, August 1990, pp. 1028-1031.

[5] N. D. Arora, J. R. Hauser and D. J. Roulston, "Electron and Hole Mobilities in Silicon as a Function of Concentration and Temperature", *IEEE Transactions on Electron Devices*, Vol. 29, No. 2, February 1982, pp. 292-295.

[6] H. A. Wheeler, "Transmission-Line Properties of Parallel Strips Separated by a Dielectric Sheet", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 13, No. 2, March 1965, pp. 172-185.

[7] M. V. Schneider, "Mircostrip Lines for Microwave Integrated Circuits", *The Bell System Technical Journal*, May-June 1969, pp. 1422-1444.

[8] H. A. Wheeler, "Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 25, No. 8, August 1977, pp. 631-647.

[9] D. M. Pozar, *Microwave Engineering*, Addison-Wesley Publishing Company, Reading: MA, 1990, pp. 184-190.

[10] H. Hasegawa, M. Furukawa and H. Yanai, "Properties of Microstriplines on Si-SiO_2 System", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 19, No. 11, November 1971, pp. 869-881.

[11] S. Chaki, S. Aono, N. Andoh, Y. Sasaki, N. Tanino and O. Ishihara, "Experimental Study on Spiral Inductors", *1995 IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, Orlando (FL): USA, May 16-20 1995, pp. 753-756.

[12] J. N. Burghartz, "Integrated Multilayer RF Passives in Silicon Technology", *Multilayer Microwave Circuits Workshop, 1998 IEEE International Microwave Symposium*, Baltimore (MD): USA, June 8 1998, pp. 67-86.

[13] H. Guckel, P. A. Brennan and I. Palócz, "A Parallel-Plate Waveguide Approach to Micro-miniaturized, Planar Transmission Lines for Integrated Circuits", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 15, No. 8, August 1967, pp. 468-476.

[14] R. J. Luebbers and K. S. Kunz, *The Finite Difference Time Domain Method for Electromagnetics*, CRC Press: Boca Raton, 1993, pp. 11-49, 391-426.

[15] T. Uwano and T. Itoh, *Numerical Techniques for Microwave and Millimeter-Wave Passive Structures*, T. Itoh (Editor), John Wiley & Sons: New York, 1989, pp. 334-380.

[16] D. Myrshekar-Syahkal, *Spectral-Domain Method for Microwave Integrated Circuits*, Wiley: New York, 1990.

[17] V. K. Tripathi and H. Lee, "Spectral-Domain Computation of Characteristic Impedances and Multiport Parameters of Multiple Coupled Microstrip Lines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 1, January 1989, pp. 215-221.

[18] T-C. Mu, H. Ogawa and T. Itoh, "Characteristics of Multiconductor, Asymmetric, Slow-Wave Microstrip Transmission Lines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 34, No. 12, December 1986, pp. 1471-1477.

[19] J. P. K. Gilb and C. A. Balanis, "MIS Slow-Wave Structures Over a Wide Range of Parameters", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 12, December 1992, pp. 2148-2154.

[20] A. R. Djordjevic and T. K. Sarkar, "Closed-Form Formulas for Frequency-Dependent Resistance and Inductance per Unit Length of Microstrip and Strip Transmission Lines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 2, February 1994, pp. 241-248.

[21] C. P. Yue, *On-Chip Spiral Inductors for Silicon-Based Radio-Frequency Integrated Circuits*, Ph. D. Thesis, Stanford University, July 1998.

[22] T. Becks and I. Wolff, "Analysis of 3-D Metallization Structures by a Full-Wave Spectral Domain Technique", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 12, December 1992, pp. 2219-2227.

[23] H-S. Tsai, J. Lin, R. C. Frye, K. L. Tai, M. Y. Lau, D. Kossives, F. Hrycenko and Y-C. Chen, "Investigation of Current Crowding Effect on Spiral Inductors", *1997 IEEE MTT-S Symposium on Technologies for Wireless Applications Digest*, Vancouver (BC): Canada, February 1997, pp. 139-142.

[24] J. Craninckx and M. S. J. Steyaert, "A 1.8 GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 5, May 1997, pp. 736-744.

[25] J. R. Long and M. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 3, March 1997, pp. 357-369.

[26] M. Kirschning, R. H. Jansen and N. H. L. Koster, "Measurement and Computer-Aided Modeling of Microstrip Discontinuities by an Improved Resonator Method", *1983 IEEE MTT-S International Microwave Symposium Digest*, Boston (MA): USA, May 31-June 3 1983, pp. 495-497.

[27] R. D. Lutz, Y. Hahm, A. Weisshaar, V. K. Tripathi, A. Grzegorek, W. McFarland and J. Meyer, "Modeling of Spiral Inductors on Lossy Substrates for RFIC Applications", *1998 IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, Baltimore: USA, June 7-12 1998, pp. 1855-1858.

[28] W. H. Hayt, *Engineering Electromagnetics*, McGraw-Hill: New York, Fifth edition, 1989, pp. 422-426.

[29] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 5, May 1998, pp. 743-752.

[30] K. O, "Estimation Methods for Quality Factors of Inductors Fabricated in Silicon Integrated Circuit Process Technologies", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 8, August 1998, pp. 1249-1252.

[31] A. M. Niknejad and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 10, October 1998, pp. 1470-1481.

[32] M. Danesh, J. R. Long, R. A. Hadaway and D. L. Harame, "A Q-Factor Enhancement Technique for MMIC Inductors", *1998 IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, Baltimore (MD): USA, June 7-12 1998, pp. 183-186.

[33] W. R. Eisenstadt and Y. Eo, "S-Parameter-Based IC Interconnect Transmission Line Characterization", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 15, No. 4, August 1992, pp. 483-490.

[34] J. C. Maxwell, *A Treatise on Electricity and Magnetism*, Dover Publications: New York, Third edition, Vol. 2, 1954, republication of the Clarendon Press, Third edition, 1891.

[35] W. H. Hayt, pp. 298-303.

[36] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors", *IEEE Transactions on Parts, Hybrids, and Packaging*, Vol. 10, No. 2, June 1974, pp. 101-109.

[37] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*, Dover Publications: New York, 1962, republication of the D. Van Nostrand Company, 1946.

[38] D. M. Krafesik and D. E. Dawson, "A Closed-Form Expression for Representing the Distributed Nature of the Spiral Inductor", *1986 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, Baltimore (MD): USA, June 1-3 1986, pp. 87-92.

[39] E. Pettenpaul, H. Kapusta, A. Weisberger, H. Mampe, J. Luginsland and I. Wolff, "CAD Models of Lumped Elements on GaAs up to 18 GHz", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 36, No. 2, February 1988, pp. 294-304.

[40] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press: New York, 1998, pp. 48-49.

[41] S. S. Mohan, C. P. Yue, M. del Mar Hershenson, S. S. Wong and T. H. Lee, "Modeling and Characterization of On-Chip Transformers", *1998 International Electron Devices Meeting Technical Digest*, San Francisco (CA): USA, December 6-9 1998, pp. 19.3.1-19.3.4.

[42] C. Wei, R. F. Harrington, J. R. Mautz and T. K. Sarkar, "Multiconductor Transmission Lines in Multilayered Dielectric Media", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 32, No. 4, April 1984, pp. 439-450.

[43] W. H. Hayt, pp. 144-154.

[44] T. G. Bryant and J. A. Weiss, "Parameters of Microstrip Transmission Lines and of Coupled Pairs of Microstrip Lines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 16, No. 12, December 1968, pp 1021-1027.

[45] J. I. Smith, "The Even- and Odd-Mode Capacitance Parameters for Coupled Lines in Suspended Substrate", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 19, No. 5, May 1971, pp. 424-431.

[46] D. W. Kammler, "Calculation of Characteristic Admittances and Coupling Coefficients for Strip Transmission Lines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 16, No. 11, November 1968, pp. 925-937.

[47] F. Medina and M. Horno, "Capacitance and Inductance Matrices for Multistrip Structures in Multilayered Anisotropic Dielectrics", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 35, No. 11, November 1987, pp. 1002-1008.

[48] K. S. Oh, D. Kuznetsov and J. E. Schutt-Aine, "Capacitance Computations in a Mutlilayered Dielectric Medium Using Closed-Form Spatial Green's Functions", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 8, August 1994, pp. 1443-1453, Corrections: Vol. 44, No. 8, August 1996, p. 1517.

[49] J. Bernal, F. Medina and M. Horno, "Quick Quasi-TEM Analysis of Multiconductor Transmission Lines with Rectangular Cross Section", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 9, September 1997, pp. 1619-1626.

[50] W. Delbare and D. De Zutter, "Space-Domain Green's Function Approach to the Capacitance Calculation of Multiconductor Lines in Multilayered Dielectrics with Improved Surface Charge Modeling", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 10, October 1989, pp. 1562-1568.

[51] G. W. Pan, G. Wang and B. Gilbert, "Edge Effect Enforced Boundary Element Analysis of Mutlilayered Transmission Lines", *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 39, No. 11, November 1992, pp. 955-963.

[52] C. D. Taylor, G. N. Elkhouri and T. E. Wade, "On the Parasitic Capacitances of Multilevel Parallel Metallization Lines", *IEEE Transactions on Electron Devices*, Vol. 32, No. 11, November 1985, pp. 2408-2414.

[53] W. Sun, W. W-M. Dai and W. Hong, "Fast Parameter Extraction of General Interconnects Using Geometry Independent Measured Equation of Invariance", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 5, May 1997, pp. 827-836.

[54] L. Wiemer and R. H. Jansen, "Determination of Coupling Capacitance of Underpasses, Air Bridges and Crossings in MICs and MMICs", *Electronics Letters*, Vol. 23, No. 7, March 26th 1987, pp. 344-346.

[55] S. S. Bedair, "On the Odd-Mode Capacitance of the Coupled Microstriplines", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 28, No. 11, November 1980, pp. 1225-1227.

[56] J. C. Maxwell, *A Treatise on Electricity and Magnetism*, Dover Publications: New York, Third edition, Vol. 1, Part II, 1954, republication of the Clarendon Press, Third edition, 1891.

[57] B. D. Popovic and D. N. Filipovic, "Theory of Power-Frequency Proximity Effect for Strip Conductors", *Proceedings of the IEE*, Vol. 122, No. 8, August 1975, pp. 839-842.

[58] R. Faraji-Dana and Y. L. Chow, "The Current Distribution and AC Resistance of a Microstrip Structure", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 38, No. 9, September 1990, pp. 1268-1277.

[59] P. Waldow and I. Wolff, "The Skin-Effect at High Frequencies", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 33, No. 10, October 1985, pp. 1076-1082.

[60] P. Waldow and I. Wolff, "Dual Bounds Variational Formulation of Skin Effect Problems", *1987 IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, Las Vegas (NE): USA, June 9-11 1987, pp. 333-336.

[61] Y. Eo and W. R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-Parameter Measurements", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 16, No. 5, August 1993, pp. 555-562.

[62] Sonnet Software Inc., *User's Manual*, Release 4.0, Volume 1, September 1 1996, *Xgeom User's Manual*, pp. 91-92, *Em User's Manual*, Chapter 7, pp. 37-39.

[63] C. P. Yue, C. Ryu, J. Lau, T. H. Lee and S. S. Wong, "A Physical Model for Planar Spiral Inductors on Silicon", *1996 International Electron Device Meeting Technical Digest*, December 1996, pp. 155-158.

[64] W. H. Hayt, p. 177.

[65] E. Tuncer and D. P. Neikirk, "Highly Accurate Quasi-Static Modeling of Microstrip Lines Over Lossy Substrates", *IEEE Microwave and Guided Wave Letters*, Vol. 2, No. 10, October 1992, pp. 409-411.

[66] D. Halliday, R. Resnick and J. Walker, *Fundamentals of Physics*, John Wiley & Sons: New York, Fifth Edition, Part 3, 1997, p. 659.

[67] R. Groves, D. L. Harame and D. Jadus, "Temperature Dependence of Q and Inductance in Spiral Inductors Fabricated in a Silicon-Germanium/BiCMOS Technology", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 9, September 1997, pp. 1455-1459.

[68] HP EESof Series IV, *HP Momentum User's Guide*, Hewlett-Packard Company, 1995, p. 9-2.

[69] Sonnet Software, *User's Manual*, Release 4.0, Volume 1, September 1 1996, *Em User's Manual*, p. 1, p. 11.

[70] R. A. Lawton, N. S. Nahman and J. M. Bigelow, "A Solid-State Reference Waveform Standard", *IEEE Transactions on Instrumentation and Measurement*, Vol. 33, No. 3, September 1984, pp. 201-205.

[71] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek and S. Moinian, "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 1, January 1996, pp. 4-9.

[72] E. Frlan, S. Meszaros, M. Cuhaci and J. S. Wight, "Computer Aided Design of Square Spiral Transformers and Inductors", *1989 IEEE MTT-S International Microwave Symposium Digest*, Long Beach (CA): USA, June 13-15 1989, pp. 661-664.

[73] I. Huynen, J.-P. Raskin, R. Gillon, D. Vanhoenaker and J.-P. Colinge, "Integrated Microwave Inductors on Silicon-on-Insulator Substrate", *27th European Microwave Conference Proceedings*, Vol. II, Jerusalem: Israel, September 8-12 1997, pp. 1008-1013.

[74] P. R. Gray and R. G. Meyer, "Future Directions in Silicon ICs for RF Personal Communications", *IEEE 1995 Custom Integrated Circuits Conference*, May 1995, pp. 83-90.

[75] L. E. Larson, "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions", *IEEE 1997 Custom Integrated Circuits Conference*, Santa Clara (CA): USA, May 5-8 1997, pp. 169-176.

[76] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, Dordrecht: The Netherlands, 1998, Chapter 5, pp. 121-159.

[77] J. N. Burghartz, M. Soyuer and K. A. Jenkins, "Integrated RF and Microwave Components in BiCMOS Technology", *IEEE Transactions on Electron Devices*, Vol. 43, No. 9, September 1996, pp. 1559-1570.

[78] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins and Y. H. Kwark, "Spiral Inductors and Transmission Lines in Silicon Technology Using Copper-Damascene Interconnects and Low-Loss Substrates", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 10, October 1997, pp. 1961-1968.

[79] A. C. Reyes, S. M. El-Ghazaly, S, J, Dorn, M, Dydyk and D. K. Schroder, "Coplanar Waveguides and Microwave Inductors on Silicon Substrates", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 9, September 1995, pp. 2016-2022.

[80] M. Park, S. Lee, H. K. Yu, J. G. Koo and K. S. Nam, "High Q CMOS-Compatible Microwave Inductors Using Double-Metal Interconnection Silicon Technology", *IEEE Microwave and Guided Wave Letters*, Vol. 7, No. 2, February 1997, pp. 45-47.

[81] J. Y-C. Chang, A. A. Abidi and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-µm CMOS RF Amplifier", *IEEE Electron Device Letters*, Vol. 14, No. 5, May 1993, pp. 246-248.

[82] A. Rofougaran, J. Y-C. Chang, M. Rofougaran and A. A. Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 7, July 1996, pp. 880-889.

[83] C-Y. Chi and G. M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 4, April 1995, pp. 730-738.

[84] Y. Sun, H. van Zeijl, J. L. Tauritz and R. G. F. Baets, "Suspended Membrane Inductors and Capacitors for Application in Silicon MMIC's". *IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, San Francisco (CA): USA, June 16-19 1996, pp. 99-102.

[85] J-S. Rieh, L-H. Lu, L. P. Katehi, P. Bhattacharya, E. T. Croke, G. E. Ponchak and S. A. Alterovitz, "X- and Ku-Band Amplifiers Based on Si/SiGe HBT's and Micromachined Lumped Components", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 5, May 1998, pp. 685-694.

[86] T. H. Lee, pp. 292-295.

[87] R. S. Pengelly, "Hybrid vs. Monolithic Microwave Circuits: A Matter of Cost", *Microwave System News*, January 1983, pp. 35-55.

[88] G. G. Rabjohn, *Monolithic Microwave Transformers*, M. Eng. Thesis, Carleton University, April 1991.

[89] D. C. Ahlgren, G. Freeman, S. Subbanna, R. Groves, D. Greenberg, J. Malinowski, D. Nguyen-Ngoc, S. J. Jeng, K. Stein, K. Schonenberg, D. Kiesling, B. Martin, S. Wu, D. L. Harame, and B. Meyerson, "A SiGe HBT BiCMOS Technology for Mixed Signal RF Applications", *1997 Bipolar Circuits and Technology Meeting*, Minneapolis (MN): USA, September 28-30 1997, pp. 195-197.

[90] H. Cho and D. E. Burk, "A Three-Step Method for the De-Embedding of High-Frequency S-Parameter Measurements", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 38, No. 6, June 1991, pp. 1371-1375.

[91] GGB Industries Inc., Picoprobe Dual Model 40 A, *http://www.picoprobe.com/dual.html*

[92] Cascade Microtech Inc., Impedance Standard Substrate, *http://www.cascademicrotech.com/cmicro/html/accessories_index_data_0.html.*

[93] P. J. van Wijnen, H. R. Claessen and E. A. Wolsheimer, "A New Straightforward Calibration and Correction Procedure for "On Wafer" High Frequency S-Parameter Measurements (45 MHz - 18 GHz)", *1987 Bipolar Circuits and Technology Meeting*, Minneapolis (MN): USA, September 21-22 1987, pp. 70-73.

[94] Hewlett Packard, "Increasing Measurement Accuracy", *HP 8753D Network Analyzer User's Guide*, September 1995, p. 5-2.

[95] T. H. Lee, Section 16.3.4, p. 497.

[96] B. Razavi, *RF Microelectronics*, Prentice Hall, Upper Saddle River (NJ): USA, 1998, Section 7.5.1, p. 229.

[97] L. Dauphinée, M. Copeland and P. Schvan, "A Balanced 1.5 GHz Voltage Controlled Oscillator with an Integrated LC Resonator", *1997 IEEE International Solid-State Circuits Conference Digest*, San Francisco (CA): USA, February 1997, pp. 390-391.