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Development and Applications of a New Deep Level Transient Spectroscopy Method and New Averaging Techniques

by

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Abstract

In this thesis, we report new advancements in the field of Deep Level Transient Spectroscopy (DLTS) which is a powerful method for investigation of electrically active point defects in semiconductors. We demonstrate these advancements by building a state-of-the-art DLTS system and performing extensive measurements on several types of field-effect transistors (FETs).

We introduce a new approach to digital signal processing in DLTS systems. The problems of signal recovery from noise and efficient data storage are addressed separately from the transient signal analysis. We combine two complementary digital averaging techniques which substantially improve the DLTS digital signal processing. Compared to other digital DLTS systems, the new averaging techniques offer an improved time resolution at the beginning of the transient, improved signal-to-noise ratio, and more efficient data storage. At the same time it offers real-time observation of essentially noise-free transients and real-time data processing.

We designed and fabricated a new feedback circuit which solves the speed and sensitivity problems of constant-capacitance (CC-)DLTS. The speed of the feedback circuit is demonstrated by comparing recorded traces from CC-DLTS with conventional capacitance-transient DLTS. Sensitivity is demonstrated with measurements of the interface trap density of virgin and hot-carrier stressed metal-oxide-semiconductor (MOS)FETs. After a slight modification, the same feedback circuit makes technically possible a new method which we call constant-resistance (CR-)DLTS.

The new CR-DLTS method is similar to the conductance DLTS, but it is more sensitive and it does not require other measurements for calculation of the trap concentrations. Unlike the conductance or current DLTS, in the new CR-DLTS technique the test transistor operates at very low current levels and stressing of the device is avoided. In addition, the

CR-DLTS signal is largely independent of the transistor size, thus allowing measurements of very small-size transistors. Since the sensitivity of CR-DLTS is proportional to the gain of the transistor (or the aspect ratio), it is completely independent of the area of the test device which is not true for CC-DLTS. We demonstrate this new method by measurements of virgin submicron MOSFETs, but the technique can be used also to study other field-effect transistors.

Next, CR-DLTS is demonstrated with measurements of proton radiation-induced traps in buried channel MOSFETs which are used as CCD output amplifiers. The unique structure of these devices offers extended opportunities for studying the space distribution of the radiation induced defects. In addition, we show a variation of the CR-DLTS technique using back-gate driving, which is applicable for studying the channel-substrate p-n junction, and the results are compared with those obtained from CC-DLTS measurements.

Finally, CR-DLTS was also successfully applied to study virgin and radiation-damaged Si and Ge junction field-effect transistors (JFETs). CR-DLTS was confirmed to be a simple, very sensitive, and area independent technique which is well suited for measurement of a wide range of deep level concentrations. Comparisons have been made again with the CC-DLTS and conventional DLTS. In addition, new possibilities for defect profiling in the channel have been demonstrated.

We expect, that the results from this thesis will be useful for many new applications of DLTS, previously not available. Also, the described averaging and data reduction techniques can be useful for many other applications involving transient data recording and analysis.

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Dedication

To my family, my wife Vera and my daughter Peki.

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CHAPTER 1

INTRODUCTION

1.1 IMPORTANCE OF IMPURITY CHARACTERIZATION

The rapid advances in semiconductor technology during last few decades are closely related to the success in achieving significant increase of the semiconductor material purity [223]*. The ability to detect and measure the properties of a very small amount impurity atoms or structural defects in the semiconductor material and in the active regions of semiconductor devices is of fundamental importance for this progress. The electrical properties of these impurities or defects are of particular interest for the performance and reliability of the semiconductor devices [73,181,223].

Shallow impurities in semiconductors generally contribute extra free carriers, electrons or holes. By intentionally incorporating shallow impurities in the semiconductor material, the type and magnitude of the conductivity of the material is controlled. The properties of the shallow impurities related to the host semiconductor material are considered to be well understood. Still, even for the best known semiconductor, silicon, some details of the interaction of the shallow impurities with the host atoms were just recently found [107].

Other imperfections in the crystal structure, such as other impurities atoms, lattice point defects and impurity-defect complexes are referred as *deep centers*. Their role is primarily to control the generation, recombination, and lifetime of the current carriers. Despite the significant progress in the last two decades, deep centers have proven to be far more difficult to investigate than the shallow impurities. In many cases, the physical nature of the center causing the appearance of a deep level is poorly understood or unknown [181].

*. References are listed at the end of the thesis in alphabetical order.

1.2 DEEP LEVEL TRANSIENT SPECTROSCOPY

Deep Level Transient Spectroscopy (DLTS) [138] is a well established research technique for characterization of electrically active centers deep in the semiconductor bandgap [16,199]. It is known for its high sensitivity and direct relation to the measured properties of the defects. In the last two decades, many variations of the method were developed and adapted for studying the defect properties of a variety of materials and devices. Still, new modifications and further improvements of the already existing DLTS techniques are regularly reported [3,19,34,54,76,95,150,152,179,187,202].

Despite the large variety of modifications, the method is not yet accepted as a standard characterization technique in the semiconductor industry. There are many reasons for this limited acceptance. First, in order to extract the properties of the traps, there is need for a wide variation of the temperature of the sample. Second, a standard describing the settings and the parameters of the measurement instrumentation is not established. Third, the wide variety of test structures and the dependence of the signal magnitude on the size of the test device prevents the establishment of a standardized approach which is convenient for industrial applications. With the continued scaling down of the device dimensions in the semiconductor integrated circuits and the emergence of new technologies such as SiGe hetero-junction bipolar technology, silicon-on-insulator (SOI), porous silicon, thin-film transistors, or copper metallization for VLSI and ULSI, the importance of accurate measurement and control of the defects which introduce deep levels will progressively increase. Therefore, steps toward further improvement and refinement of the DLTS method and instrumentation have important practical applications.

1.3 GOALS OF THIS RESEARCH

This thesis describes new and improved digital techniques for transient data processing which offer better sensitivity and more effective data storage. This approach is

applicable for all variations of DLTS and can be easily adapted to other experiments involving recording and analysis of transient signals. Also, it opens up opportunities for further development of the group of isothermal DLTS techniques which rely on the analysis of the transient decay for extraction of the characteristic time constant and not on the thermal scan. Second, a new feedback circuit is described which allows for fast and sensitive operation in one very attractive and technically challenging variation of the method - Constant Capacitance (CC-)DLTS. It is important to note that this variation produces a signal with a magnitude that is independent of the area of the device and therefore, the method is better suited for routine parametric control in the semiconductor industry. Third, a new technique, termed constant-resistance (CR-)DLTS is presented. This new technique is well-suited for measurements of field-effect transistors (FETs) regardless of their size and without compromise to the sensitivity of the measurement. Unlike CC-DLTS, because the sensitivity is dependent of the gain of the transistor (thus, of the channel width-to-length ratio and not of the active area) it allows for sensitive measurement of very small, deep-submicron devices which are the basic transistors in the advanced microelectronics circuits and systems.

For corroboration of this technique, the results are compared to the obtained from conventional DLTS and CC-DLTS measurements. While the method has been applied to three different types of field-effect transistors, it can be easily used for a wider range of FETs. Illustrations are made with measurement of proton- and neutron-induced damages in metal-oxide-semiconductor (MOS) FETs and silicon and germanium junction FETs. Also the possibilities for measurement of interface trap density in the active interface of regular MOSFETs, and for defect profiling using the new technique are demonstrated.

In this thesis the emphasis is on the development of the semiconductor metrology and instrumentation using mixed analog, digital, and software engineering. The experimental results are mainly used for illustration of the new techniques and are not self-contained and complete studies.

1.4 ORGANIZATION OF THE THESIS

In Chapter 2, the basics of the DLTS method are introduced and various techniques and instrumentation are described. The existing large variety of DLTS makes any attempt for classification a very complex task. Nevertheless, an attempt to define the criteria which can be used for classification of the DLTS techniques is made. Following these criteria, a classification scheme is demonstrated with examples using well known and less popular DLTS techniques. One potential benefit of this classification is the identification of techniques and conditions which allows the reader to quickly tailor the setup to fit the specific properties of the device or material under investigation.

In Chapter 3, two complementary digital signal processing techniques which are well suited for DLTS applications are presented. These techniques are new in the processing of digitized DLTS transients and can be used in virtually any DLTS experiment. Furthermore, their application can be easily extended to the data processing in other physical experiments which produce transient signal. A mathematical model is presented and error analysis is made of pseudo-logarithmic averaging, the technique which is less known in digital signal processing. Because of the substantial increase of the signal-to-noise ratio and efficient data reduction, these techniques may increase interest in the isothermal DLTS techniques [2,109,118,176,177,255].

The latest developments in the feedback circuit used for CC-DLTS are presented in Chapter 4. This improved feedback circuit is essential for the successful implementation of the new constant-resistance (CR-)DLTS technique. The speed of the feedback is demonstrated by comparison of recorded traces from standard capacitance-transient DLTS, CC- and CR-DLTS. Guidelines are given for design of the feedback circuit and its setup during CC- and CR-DLTS measurements. The sensitivity achieved using the feedback circuit is demonstrated with measurements of interface-trap density of submicron MOSFETs.

A description of the new CR-DLTS technique is given in Chapter 5. This new technique is similar to the conductance DLTS, but it is more sensitive and it does not require simultaneous measurement of the transconductance g_m , or surface mobility μ of the transistor for calculation of the trap concentrations. An important advantage is that the DLTS signal is independent of the transistor size, which allows for measurements of very small transistors. In this chapter, the technique is demonstrated with measurements of submicron enhancement-mode MOSFETs. The body effect on CR-DLTS is demonstrated and CR-DLTS is compared with CC-DLTS by using a multi-transistor structure containing 400 transistors connected in parallel.

In Chapter 6, the new CR-DLTS technique is demonstrated with measurements of radiation-induced traps in buried channel MOSFETs which are used as CCD output amplifiers. These devices exhibit a unique structure which offers extended opportunities for studying the spatial distribution of the defects. In addition to the normal front-gate mode of operation, the back-gate mode of operation is demonstrated, and this mode is applicable for studying the channel-substrate p-n junction. The results are compared with CC-DLTS data. Complementary measurements using front-gate and back-gate operation of CR-DLTS can be useful to resolve the difficulties in the analysis of DLTS data from structures with symmetrical p-n junctions.

In Chapter 7 of this thesis, the CR-DLTS technique is applied to study virgin and fast neutron irradiated junction field-effect transistors (JFETs). The technique is demonstrated with measurements of three groups of devices: commercially available discrete silicon JFETs, virgin and high-level neutron-irradiated silicon JFETs made by a specific monolithic technology [35], and commercially available discrete germanium p-channel JFETs. CR-DLTS is demonstrated to be a very sensitive and area independent technique applicable for measurement of a wide range of deep level defect concentrations. Comparisons are made with the CC-DLTS and standard capacitance DLTS. Possibilities for defect

profiling in the channel are also demonstrated.

Chapter 8 summarizes the accomplishments described in the thesis and recommends directions for future work. It also gives references to follow in future research in this field and propose some attractive applications of the developed system.

At the end of the thesis is presented an extended list with references and appendixes which include schematics of electronic blocks, program listings and mathematical transformations.

CHAPTER 2

REVIEW OF THE DEEP-LEVEL TRANSIENT SPECTROSCOPY METHOD

2.1 INTRODUCTION

In this chapter we review the basics of the deep-level transient spectroscopy - the subject of investigation, methods for DLTS signal detection and data processing. First, the kinds of imperfections that can be studied with DLTS are described and some important results of the generation-recombination statistics are reviewed. Then, several detection techniques, based on the effect of trapped charge on measurable electrical parameters are presented. Next the standard capacitance-transient DLTS method is introduced. This is followed by a general description of the main stages in the DLTS experiment. This definition of the stages in the DLTS helps the reader to understand better the options for design of an experiment and serve as a basis for a classification scheme. The chapter concludes with a demonstration how a given technique could be classified according to this new classification scheme and a few examples are given for illustration.

2.2 DEFECTS, IMPURITIES AND ENERGY LEVELS

2.2.1 Shallow Impurities

The explosive growth of the electronic industry during last few decades is based on the significant increase in the accumulated experience to manipulate the properties of the crystalline semiconductors. This manipulation is done by tight control of the purity and perfection of the crystal lattice and intentional incorporation of atoms extrinsic to the host semiconductor material. Shallow impurities in semiconductors introduce minor perturbations in the lattice, creating bound states in the band gap of the host material very close to the band edges. They generally contribute extra charge carriers - electron or holes. The primary role of intentionally incorporating shallow impurities in the semiconductor material

is to control the type and magnitude of the conductivity in the material. The *ionization energy* E_{sh} is the amount of energy that the foreign atom needs to release a free current carrier in the host material. It is clear that for conductivity due primarily to the extrinsic atoms, this ionization energy must be less than kT (k - Boltzmann constant, T - absolute temperature) or much smaller than the band gap energy E_g of the host material which determines the amount of intrinsic free carriers at a given temperature.

For example, if electron conduction is required, the extrinsic atom must “donate” an electron and therefore is called a *donor*. Similarly, if hole conductivity is required, the extrinsic atom must “accept” an electron from the host material, thus creating a free hole, and the extrinsic atom is called an *acceptor*. In Table 2.1 are listed some experimentally

Table 2.1: Ionization Energies of Shallow Impurities in Si and Ge.

Impurity element	E_{sh} in Si [eV]		E_{sh} in Ge [eV]
	Thermal	Optical	Thermal
Donors			
Li	0.033	-	-
P	0.044	0.045	0.0120
As	0.049	0.053	0.0127
Sb	0.039	0.043	0.0096
Bi	0.069	-	-
Acceptors			
B	0.045	0.046	0.0104
Al	0.057	0.067	0.0102
Ga	0.065	0.071	0.0108
In	0.16	0.154	0.0112

determined (using thermal and optical methods) ionization energies of shallow impurities in silicon and germanium [121]. Since Si and Ge are group IV of the periodic table, most donors are from group V, which substitute for the Si or Ge atoms and have one remaining

electron in the upper, valence shell from which an electron can be easily released to contribute to the electron conduction. In a similar way, the elements from group III are acceptors, since they require an extra electron to complete the upper, valence shell and taking this electron from the lattice, they will produce a free hole. In general, the presence of shallow level impurities is well understood: the potential in the crystal lattice is essentially Coulomb-like and the impurity states are very closely related to the states of the hydrogen atom [158,181]. The properties of the shallow impurities related to the host semiconductor material were essentially determined by the end of 1950s both theoretically (effective-mass theory) and experimentally using mainly optical absorption techniques. However, even for the best known semiconductor, silicon, details are still being revealed [107].

2.2.2 Deep Level States: Electron, Hole Traps and Recombination Centers

Other impurities and point lattice defects such as vacancies, self-interstitials, anti-site defects etc., induce more severe local perturbations of the potential in the crystal lattice, creating bond states more localized and deeper in the band gap. Such imperfections in the crystal structure, as impurity atoms, lattice point defects and impurity-defect complexes are referred to as *deep centers* [97,158,181,223]. As opposed to shallow impurities, they act primarily as charge carrier traps or recombination centers and thus, they control the lifetime of current carriers. When a center in the forbidden energy gap interacts mainly with electrons from the conduction band, it is defined as an *electron trap*; in the case when the center interacts mainly with holes in the valence band, it is defined as a *hole trap*; and in the case when both type of carriers can interact with the center, it is called *recombination center* (see Fig. 2.1 and Refs. [161,196,199,223]). Since the probability for electron or hole emission is exponentially dependent on the energy separation to the corresponding conduction or valence band, the most effective recombination centers are those with energy levels around the midgap which have nearly equal probabilities for electron or hole emission. For the same reason, at relatively low temperatures, deep levels above the midgap usually act as electron traps (or donor-like) and those below the midgap as hole traps (acceptor-like)

[97,158,199,223]. However there are many exceptions to this rule at higher temperatures.

Deep centers have proven to be far more difficult to investigate than the shallow impurities. In many cases the physical nature of the center causing the appearance of a deep level is poorly understood or unknown [181]. As a common characteristic, bulk induced

Figure 2.1 Illustration of relaxation processes; a) direct band-gap recombination; b) relaxation processes involving a deep level

defects exhibit one or more well defined discrete energy levels and often are called *deep levels** [97,158,181,182,199,223]. In contrast, surface related defects usually generate a continuum of energy levels spread over the whole bandgap [16,173,119,223] and are commonly referred to as *interface traps*.

In addition to the shallow impurities and deep centers, the semiconductor lattice may contain extended defects, such as dislocations, stacking faults, precipitates, and grain boundaries. In most cases they behave electrically as large-concentration deep centers, and in general, crystals free of dislocations are desired for electronic and optoelectronic applications [181].

2.2.3 Effects of the Deep Centers on the Device Performance

As mentioned above, deep levels control primarily the lifetime of the excess charge carriers. In devices where long carrier lifetime and stability is desired, deep centers usually are unintentionally incorporated and have a negative effect. Leakage currents in p-n junctions [33], Schottky barriers, and related devices [158], minority carriers lifetime degradation [80], charge losses in CCD cells [169] or DRAM capacitors, reduced efficiency and degradation of solar cells [192,193,198] and high electron mobility transistors (HEMTs) [157], contact quality [181], performance degradation [158] and low-frequency noise [83, 170,171] may be attributed to deep centers. For VLSI technology, as the dimensions shrink and die area increases, the defect density must be decreased appropriately, and so very low deep center concentrations must be detected and eliminated [187]. Furthermore, the new technology trends are for using deep trenches filled with a dielectric having quite different mechanical properties from the host semiconductor. As a result, consecutive thermal treatment may generate stress-induced lattice defects [181]. Annealing of these defects [103] is not a simple task, since other important requirement, the need to keep the p-n junctions

*. Here and elsewhere, we use the short form *deep levels* to stand for *deep level centers*.

shallow, calls for lowering the temperature and shortening the time of the thermal processing. Recently, in a number of models, native defects at the interface were attributed to the Fermi-level pinning observed at Schottky contacts [181].

For optoelectronic devices, non-radiative transitions through deep levels may substitute for the radiative transitions thus degrading photon yield by up to a few orders of magnitude [182]. Therefore, deep level control is of particular importance for III-V devices and especially for solid-state lasers, such as GaAs/AlGaAs lasers [137]. Recent success in the development of SiGe heterojunction devices is particularly exciting for the future of the silicon-based electronics - this may provide two properties missing in crystalline silicon microelectronics, but inherent for III-V devices: bandgap engineering and light emission. Because of the lattice mismatch between Si and Ge, thin $\text{Ge}_x\text{Si}_{1-x}$ layers may generate a significant amount of deep levels which can lead to a significant deterioration of some desired device properties, mainly carrier mobility [137]. Studying deep levels is also important for optimization of III-V devices [69-72].

On the other hand, in devices where short lifetime is beneficial or recombination is light emitting, such as in fast switches or light-emitting diodes (LEDs) respectively, deep centers can be introduced intentionally. For example, nitrogen and oxygen introduced in GaP are responsible for the radiative recombination in commercial LEDs, and gold-doping is used to reduce the switching time in fast Si-based bipolar devices [181]. Another example of possible benefits of deep levels is Cr-doping used to reduce the conductivity and obtain semi-insulating GaAs substrates. Nevertheless, in these technologies the control of non-intentional contaminants is required, since they can impede the role of the wanted impurity. In all cases, the ability to identify the deep centers and to measure their concentration, and sometimes their spatial distribution (impurity profile), is a necessary requirement.

2.3 GENERATION-RECOMBINATION STATISTICS

2.3.1 Phenomenological Overview

In an ideal semiconductor material, there are no allowed energy states inside the bandgap. As outlined above, they are created by incorporation of shallow impurities and deep defect states. The later are also referred to as traps, generation-recombination (G-R) centers, deep levels, deep centers, deep impurities, deep imperfections etc. Although in many cases, the use of a specific term is justified, this abundance of names might sometimes be confusing. Further complication arises from the fact that the same defect state can be a trap or a G-R center depending on the temperature and the energy level in the bandgap. In Fig. 2.2 are defined electron and hole traps, and a recombination center [161]. The probability for a given transition is illustrated by the width of the arrow defining this process. From Fig. 2.2 is clear that the complete description of a particular defect does not define it only as a trap for electrons or holes but as a deep level with specific capture cross sections

Figure 2.2 Definition of electron trap, hole trap and recombination center

for electrons σ_n and for holes σ_p . Then the capture rate coefficients c_n and c_p are defined as [78,206]

$$c_n = \sigma_n \langle v_n \rangle \quad \text{and} \quad c_p = \sigma_p \langle v_p \rangle \quad (2.1)$$

where $\langle v_n \rangle$ and $\langle v_p \rangle$ denote the average thermal velocities for electron and holes respectively. Considering that the capture rate itself equals the capture coefficient multiplied by the concentration of the free carriers, i.e. $c_n n$ for electrons, it is obvious that a given defect with specific capture cross sections σ_n and σ_p can be a trap or recombination center depending on the free carrier concentrations.

2.3.2 Some Results from Shockley-Read-Hall (SRH) Theory

Let consider the simple case when only one kind of deep center exists in the material. A deep center may be occupied by an electron or hole. The concentrations of deep centers occupied by electrons n_t , and those occupied by holes p_t must equal the total concentration of the deep centers N_t , i.e. $N_t = n_t + p_t$. When free electrons and holes are generated and trapped, the electron concentration in the conduction band n , the hole concentration in the valence band p , n_t , and p_t are functions of time. The time rate of change of these concentrations is described by SRH theory [78,206]. The *emission rate* for electrons e_n represents the number of electrons, emitted from charged deep centers per second. Similar is the definition of the *emission rate* for holes e_p . The *capture rates* c_n and c_p are defined above using (2.1). In general, the rate of change of n_t or p_t are described by non-linear differential equations. Either of these equations can be linearized and solved in two cases: 1) in the reverse-biased space charge region, where the free carrier concentrations n and p are small and can be neglected, and 2) in the quasi-neutral region, where n and p are essentially constant. For the last case the solution for $n(t)$ gives [199]

$$n_t(t) = n_t(0) \left[\exp\left(-\frac{t}{\tau}\right) \right] + \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_t \left[1 - \exp\left(-\frac{t}{\tau}\right) \right] \quad (2.2)$$

where $n(t)$ is the concentration of the deep center occupied by electrons at $t=0$, e_n and e_p are the emission rates for electrons and holes, $c_n n$ and $c_p p$ are their respective capture rates, and $\tau = 1/(e_n + c_n n + e_p + c_p p)$. Equation (2.2) is difficult to solve without additional simplifications because e_n , e_p , c_n , and c_p are not known, and n and p vary with time and distance in the material. However, some important simplifications can be made for extrinsic semiconductors in the case of one-sided p-n junction or Schottky barrier [161,199].

In an n-type semiconductor, to a first approximation, p can be neglected. If we consider a Schottky diode on an n-type substrate with electron traps in the active region, then at zero bias the capture rate dominates the emission rate and the steady-state concentration is $n_t = N_t$. After applying a reverse bias pulse, within several picoseconds, the free electrons are swept out of the space-charge region (SCR) and emission dominates since $c_n n \approx 0$. Then $\tau_{ne} = 1/e_n$ and (2.2) reduces to

$$n_t(t) = n_t(0) \exp\left(-\frac{t}{\tau_{ne}}\right) \approx N_t \exp\left(-\frac{t}{\tau_{ne}}\right) \quad (2.3)$$

However, at the edge of the space-charge region (the so called Debye tail) the electron concentration is not negligible, $c_n n$ is not zero, e_n is not constant, and so the time dependence of $n(t)$ can be non-exponential if the contribution of that effect to the total transient is not small enough.

When the diode is pulsed back to zero bias, the free electrons flow back in the space-charge region, and if the previous emission pulse was long enough to empty most of

the electron traps, then capture dominates, and the concentration $n(t)$ is given by

$$n_t(t) = N_t - [N_t - n_t(0)] \exp\left(-\frac{t}{\tau_{nc}}\right) \quad (2.4)$$

where $\tau_{nc} = 1/c_n n$ and $n_t(0)$ is the initial steady-state concentration.

Considering equilibrium conditions, the *principle of detailed balance* requires the rates of emission and capture processes to be balanced. Thus [199],

$$e_{no} n_{To} = c_{no} n_o p_{To} = c_{no} n_o (N_T - n_{To}) \quad (2.5)$$

where n_o (the index $_o$ denotes equilibrium values) is

$$n_o = N_c \exp\left[-\frac{E_c - E_F}{kT}\right] \quad (2.6)$$

and

$$n_{To} = \frac{N_T}{1 + \exp[(E_t - E_F)/kT]} \quad (2.7)$$

where E_c is the conduction band energy level, E_t is the deep-center level energy, T is the absolute temperature and k is Boltzman's constant. Using (2.7) from (2.5) we obtain

$$e_{no} = c_{no} N_c \exp\left[-\frac{E_c - E_t}{kT}\right] = c_{no} n_1. \quad (2.8)$$

In similar way can be obtained the emission rate for holes e_{po} . Next, an important assumption is made. The deviation from equilibrium state is considered small, the new state is referred to as quasi-equilibrium and the *new non-equilibrium emission and capture rates are considered equal to their equilibrium values*. This is expressed as

$$e_n = c_n n_1 \quad \text{and} \quad e_p = c_p p_1 \quad (2.9)$$

where

$$n_1 = N_c \exp\left[-\frac{E_c - E_t}{kT}\right] \quad (2.10)$$

and

$$p_1 = N_v \exp\left[-\frac{E_t - E_v}{kT}\right]. \quad (2.11)$$

In the reverse biased junction where a strong electric field exists, this is certainly a poor approximation and capture cross sections determined under these condition generally do not give reliable results [199]. Nevertheless, the assumption is commonly made and the accuracy of all results remains in the limits of this uncertainty.

Considering equations (2.9) and (2.10), the expression for the emission rate e_n of electrons trapped in centers with energy level E_t below the conduction band is

$$e_n = \sigma_n v_n N_c \exp\left(-\frac{\Delta E_t}{kT}\right), \quad (2.12)$$

where N_c is the effective density of electron states in the conduction band and $\Delta E_t = E_c - E_t$. Here and further in the text we omit the brackets around $\sigma_{n,p}$ for brevity. Similarly, for hole traps in p -type semiconductor, we obtain

$$e_p = \sigma_p v_p N_v \exp\left(-\frac{\Delta E_t}{kT}\right), \quad (2.13)$$

where N_v is the effective density of hole states in the valence band and $\Delta E_t = E_t - E_v$. The expressions for the emission rates (2.12) and (2.13) are the fundamental equations in the DLTS method. Since the sample material is known, v_n and N_c (or v_p and N_v respectively) can be easily calculated over a wide range of temperatures. Then, it remains to determine experimentally the characteristic defect parameters σ_n (or σ_p) and ΔE_t . Each one of these equations links two unknown parameters of a deep center with two measurable variables - emission rate and temperature. Therefore, one has to measure the dependence of the emission rate from the temperature in order to obtain the deep center parameters. Alternatively, the capture cross section can be determined from the capture process kinetics [88,180,242], the emission rate can be measured, and ΔE_t determined at a constant temperature (isothermal measurement). However, for a wide range of deep levels the emission rate at room temperature is too fast or too slow in order to be accurately measured conveniently with sensitive instrumentation. Considering the exponential dependence of the emission rate on the temperature, as indicated in (2.12) and (2.13), the relative distance from the corresponding band edge, and the speed of most frequently used instrumentation, the useful temperature range can be estimated to be 50 to 450 K. This means that control of the sample temperature and, most likely, cooling well below the freezing point might be required even for isothermal measurement of the deep level parameters.

2.4 DETECTION OF THE EMISSION OF THE TRAPPED CHARGE

2.4.1 Capacitance Transient

For simplicity, the case of a one-sided abrupt p-n junction or Schottky barrier will be considered in the following sections. The specifics of MOS structure will be also discussed where applicable. Let us consider the space-charge region (SCR) of a

Figure 2.3 Reverse-biased p^+-n junction with one deep level at E_t . V_B is the built-in potential, V_R is the reverse bias, E_d is the donor level: a) with a donor-like deep level; b) with an acceptor-like deep level, where $\circ$ is neutral, $+$ is positive ion, and $-$ is negative ion.

reverse biased p^+-n junction or a Schottky barrier on n -type semiconductor [161]. In Fig. 2.3 is shown only the SCR in the lightly doped n -type material, since the SCR spreads mainly on this side of the junction. In ideal n -type material, the SCR contains only the charge of the ionized donors. Let us assume that donor-like deep levels are present in the SCR and they are charged with trapped electrons, for example, after a pulse to zero or a slight forward bias. Applying reverse bias again will sweep out the free electrons in few picoseconds and for $0 < x < y$ in the SCR, the charge trapped in the deep levels will be added to that of the ionized donors. Within that part of the SCR the electronic transition will be entirely an emission process since there are no free electrons and the capture rate will be zero [223]. More complicated is the situation in the transition region at $y < x < w$ where both generation and recombination processes contribute to the equilibrium occupation of the deep level traps [161]. One should also remember, that the transition to the

Figure 2.4 Capacitance transient due to a majority carrier trap in a p^+n diode.

quasi-neutral region in the bulk is not abrupt, but has some width determined from the diffusion of free electrons into the SCR. This transition is also known as the Debye tail region [161,189,223]. When the width of the SCR is much larger than the width of the transition region, the emission process described by (2.12) will dominate and the junction capacitance can be used to monitor this process. Because the traps inside $0 < x < y$ cannot be charged with electrons at reverse bias, it must be alternated with a bias at which electron capture will dominate. This is usually accomplished by applying for some short period of time a slight forward or zero bias, which is commonly referred to as a trap *filling pulse* [199]. During this filling pulse, the capture rate dominates because of the large concentration of free electrons. In Fig. 2.4 this is the second event in the sequence. After this pulse

(event 3 in Fig. 2.4), the bias is set back at V_R but the capacitance is below the quiescent (event 1 in Fig. 2.4) because of the compensation effect of the trapped majority carriers, electrons in this case. Next, at the moment $t = 0^+$ these trapped electrons will be emitted at a rate defined by (2.12) and after a sufficiently long time the system will restore to its quiescent state with the corresponding steady-state capacitance value. This relaxation of the system can be observed through the capacitance transient ΔC shown in the central part of Fig. 2.4 and corresponding to event 4.

When the trap in the n-type material is acceptor-like, the situation can be more complicated [161]. As it is shown in Fig. 2.5 a forward bias pulse can be used to inject minority carriers (event 2 in Fig. 2.5) in order to populate the deep levels with holes, which can be subsequently emitted (event 4 in Fig. 2.5). This emission of holes is defined by (2.13) and can be monitored as a capacitance transient ΔC shown in Fig. 2.5. From Figs. 2.4 and 2.5, it is clear that the sign of ΔC indicates whether the emission is from a majority or from a minority carrier trap. In the case of a voltage bias or photo-injection pulse, a complication arises from the fact that the pulse introduces both majority and minority carriers in the depleted region, thus two capture processes govern the population of the deep levels. Also, deep levels near the midgap may emit carriers to both conductance and valence bands [161]. Experiments with variation of the injection level or other modifications [125] may help to reduce this ambiguity. Nevertheless, because of these complications, it is generally accepted that the DLTS method based on capacitance-transient measurements is mostly a majority-carrier method [16]. Its strength is that each deep level can be distinguished through its unique set of activation energy and capture cross section, and can be studied independently [12].

One important requirement in order to obtain a simple relation between the measured capacitance transient ΔC and the emitted charge is $\Delta C \ll C$ where C is the total capacitance of the diode. It can be shown [199] that this condition is satisfied when the

Figure 2.5 Capacitance transient due to a minority carrier trap in a p^+-n diode.

deep level concentration is $N_t \ll N_d$ where N_d is the donor concentration. Then, the expression for time dependence of the capacitance $C(t)$ toward its steady-state value C_o is simplified to

$$C(t) = C_o \left[1 - \frac{n_t(t)}{2N_d} \right] = C_o \left[1 - \frac{n_t(0)}{2N_d} \exp\left(-\frac{t}{\tau_{ne}}\right) \right]. \quad (2.14)$$

Assuming complete trap filling and using (2.14), it is simple to show that $\Delta C/C = N_t/2N_d$. Therefore, for sensitive measurements of trap concentrations orders of magnitude below the shallow impurity concentration, the ability to measure very small relative changes in the capacitance of the diode is required.

2.4.2 Current Transient

Another means to detect the charge emission from the traps in the previous cases is to measure the current transient [18,197,231]. Indeed, the electrons emitted from the traps cause a current transient [199] which is given by

$$I(t) = \frac{qAW_0}{2\tau_{ne}} \cdot \frac{n_t(0)\exp(-t/\tau_{ne})}{[1 - (n_t(0)/2N_d)\exp(-t/\tau_{ne})]} - I_l \quad (2.15)$$

where W_0 is the width of SCR from which the current transient originates and I_l is the leakage current which is eliminated in differential measurement mode [251]. In the above expression, the validity of the approximation $N_t \ll N_d$ was assumed. Expression (2.15) is not a simple function of τ_{ne} since the time constant appears both in the nominator and in the denominator. When the second term in the denominator is small compared to unity, it can be neglected and (2.15) regains the usual exponential time dependence.

The main advantage of measuring the current transient is that the detection instrumentation can be faster than typical capacitance meters, and the current transient can be obtained from structures with relatively small area. However, using the current transient as a probe for detection of the emitted charge from the traps has two major disadvantages as compared to the capacitance transient technique. First, current response is related to the change in the trap occupancy with charge through dQ/dt while the capacitance transient is directly proportional to ΔQ . Second, there is no distinction between emission of majority or minority carriers. For these reasons, current transient measurements are used for of samples with large leakage current [43] or with small area [85] since these samples cannot be measured using the capacitance transient technique.

2.4.3 Charge Transient

The charge emitted from the traps can also be measured directly. A circuit for this type of measurement is proposed in [63]. This circuit is essentially an analog integrator of the current transient described above. Therefore, the integration time constant of the integrator $\tau_F = R_F C_F$ must be much larger than the largest time constants of measured transient τ_{ne} . Then, neglecting the second term in the denominator of (2.15) and considering an integrator with a time constant $\tau_F \gg \tau_{ne}$, the emitted charge can be detected as a voltage transient [63,199] which is given by

$$V(t) \approx \frac{qAW_0}{2C_F} \cdot n_t(0)[1 - \exp(-t/\tau_{ne})] + \frac{I_1 t}{C_F}. \quad (2.16)$$

Comparing (2.16) with (2.15), we see that τ_{ne} is eliminated from the denominator in the exponential prefactor, thus simplifying the analysis [227]. Another advantage is much the simpler instrumentation needed to measure fast decaying transients.

2.4.4 Voltage Transient

When the volume of the space charge region can be held constant by applying a voltage to compensate for the emitted charge, this voltage is directly proportional to the emission of the trapped charge. The simplest method to keep the volume of the SCR constant is to maintain the capacitance C of the diode constant by adjusting the reverse bias [52,68,99,101,160,204,122]. The compensation voltage needed to maintain the capacitance constant is a voltage transient [52,199] and is given by

$$V(t) = \frac{q\epsilon_s A^2}{2C^2} \left[N_d - n_t(0) \exp\left(-\frac{t}{\tau_{ne}}\right) \right] + V_{bi} \quad (2.17)$$

where ϵ_s is the dielectric permittivity of the semiconductor, A is the diode area, and V_{bi} is the built-in junction potential. Unlike the expression for the capacitance transient, (2.17) is valid even when the condition $N_t \ll N_d$ is not satisfied. In other words, (2.17) can be used even for large trap concentrations comparable with that of the shallow level impurity. Another important advantage of using this method for detecting the emitted charge is that it does not depend on the area of the diode, since the signal depends on A^2/C^2 according to (2.17). A similar area independence also exists when the traps are located at the interface of a MOS structure. Because of their continuous distribution in the bandgap, interface traps are measured with their energetic density of states per unit area $D_{it}[\text{eV}^{-1}\text{cm}^{-2}]$. When the decaying transient $V_G(t)$ is measured at two delay times t_1 and t_2 with $t_2 > t_1$, and the capture cross section is considered independent on the energy and temperature, the interface trap density is given as

$$D_{it} = \frac{C_{ox}}{qkT A \ln(t_2/t_1)} [V_G(t_1) - V_G(t_2)]. \quad (2.18)$$

Disadvantages of this method are considered to be the reduced speed and sensitivity of the measurement because of the instrumentation needed to maintain the capacitance constant [199]. However, the recent developments of the feedback circuit [204,122] which is used in conjunction with a fast capacitance meter have effectively eliminated this disadvantage. One should note, that even using this detection method often does not produce ideal exponentially decaying transients since the approximations which were used to obtain (2.12) and (2.13) are not valid - the reason is a considerable capture rate in the Debye tail [189].

Besides the constant-capacitance technique, we note also other methods used to keep the volume of the SCR constant. The constant-resistance method uses the dependence of the threshold voltage (or pinch-off voltage) of a field-effect transistor on the volume of

the SCR and the balance of the total charge within it [123]. Another technique, convenient for bipolar transistors, could possibly use the Early voltage as a tool to probe charge emission from the traps localized in the collector-base SCR. In general, virtually any device where the SCR can affect some device parameter may offer an opportunity to compensate for the charge emitted from the traps localized inside the SCR by adjusting the applied voltage. Then this compensation voltage should display a transient described by (2.17) or another expression related to (2.12) and (2.13). Therefore, further developments in this technique might be expected.

2.4.5 Other Methods

In the above methods the test structure was a one-sided abrupt p-n junction or Schottky barrier diode and the detection of the change in the trapped charge was based on the measurement of some electrical parameter of the diode. However, there are about 200 different effects in semiconductors relating their electrical, optical, magnetic, acoustical, thermal and mechanical properties. Many of these may be related to the charges trapped in the deep level centers in the bandgap and thus may be used to probe its changes. For example, the transverse component of the acousto-electric voltage generated by a surface acoustic wave (TAV) has been used as a such probe [224,225]. The Hall effect has been also used [105]. In both cases, the new technique was used to study semi-insulating GaAs where the concentration of free carriers is too low for standard DLTS measurements. It can be speculated, that deep levels may play a crucial role in the appearance and magnitude of some effects. Therefore, finding a convenient method to study deep levels may have a significant practical value. In principle, this is a largely unexplored area and the limited application of other detection methods can be attributed to both the limited knowledge about the influence which charge emission from deep levels has on any particular semiconductor effect, and the lack of suitably developed instrumentation.

2.5 DETERMINATION OF THE DEEP LEVEL PARAMETERS

2.5.1 Uncertainties in Determination of the Deep Level Parameters

There are three major deep-level parameters of interest: energy level position, capture cross section and concentration [12,31,74,191]. Sometimes, it is also important to know the spatial distribution of a trap in the bulk of the semiconductor [147,205,213] or the energetic distribution of interface traps in the bandgap [102,119,208,210]. Finding the energy level position and the capture cross section is most important since these are major steps in the process of trap identification [13,31,113,159,223,240]. However, these parameters may not suffice and a close look at the production history of the test structure may be required [12].

Equations (2.12) and (2.13) for the emission rate of the trapped charge describe a thermally activated process. The standard approach is to measure the emission rate at different temperatures, to construct an *Arrhenius plot* (i.e. $\log(1/\tau_{en,p})$ versus $1/T$), and to determine the activation energy and the exponential prefactor. It seems straightforward to consider the energy level difference to the corresponding band edge ΔE_t as the activation energy and from the prefactor to determine the capture cross section $\sigma_{n,p}$. Unfortunately, this is not precisely true for several reasons.

First, the exponential prefactor in (2.12) and (2.13) contains thermally dependent entities. N_c is dependent on temperature as $\sim T^{3/2}$ and v_n as $\sim T^{1/2}$ which is easily accounted by plotting $\log(1/T^2 \tau_{en,p})$ versus $1/T$. However, $\sigma_{n,p}$ and its thermal dependence is not known. For determination of $\sigma_{n,p}$ it is better to use the filling pulse technique [21,88,138,185,180,199,260] at several temperatures and to find its thermal dependence. Often this gives an additional term in the exponent [161,199] and, as a result, the Arrhenius plot does not accurately give the energy level position or the capture cross section. Other complications arise when $\sigma_{n,p}$ and ΔE_t are electric-field dependent [39,139,130,153,196,

237]. When thermodynamic considerations are taken into account, it is shown [59,199] that the thermal activation energy is related to the enthalpy, whereas the energy difference in (2.12) and (2.13) is related to the entropy. This difference can be accounted for by introducing a degeneracy factor g in these equations, but this degeneracy factor is not well known for the deep levels [138,139,199].

There is a large variety of techniques used to investigate deep levels by measuring their effect on some property of the host semiconductor material [44,75,120,133,158,161,196,199]. Here we concentrate on the technique which investigates the transient phenomena during emission of the charge trapped at deep levels or interface traps.

2.5.2 The “Rate Window” Concept

For measurement of the activation using Arrhenius plot technique, one has to obtain the relation between the time constant of the measured transient and the temperature. Considering the fact that the transient signal itself is frequently very noisy and is often superimposed on some background constant level which is orders of magnitude larger than the magnitude of the transient, monitoring a fast signal decay usually in the millisecond range is not a trivial measurement task. A major breakthrough occurred in 1974, when D. V. Lang introduced so called “rate window” concept and applied it to the method that he named Deep Level Transient Spectroscopy or DLTS [138]. In essence, this is an electronic filter for a decaying transient signal with a particular time constant, selected by the user. The filtering property is independent of the magnitude of the tested signal. When the sample’s temperature is varied, the emission rate of each trap with energy in the bandgap varies accordingly to (2.12) or (2.13). When the emission rate is within the “rate window”, i.e. the time constant of the decaying transient equals that of the system filter, then the event is indicated by appearance of a peak in the system output signal. When the range of variation of the temperature is large enough, each trap will be indicated by a characteristic peak depending on the specific properties of the trap: activation energy and capture cross sec-

Figure 2.6 The concept for a time-constant filter known as “rate window”.

tion. Thus, the output signal will look like a spectrum produced by an optical measurement. For this reason the method was named *transient spectroscopy*, and a plot of the output signal versus temperature is called a *DLTS spectrum*. In principle, it is enough to change the system time-constant filter just once and to repeat the measurement, since two data points for the Arrhenius plot can define a straight line. Frequently, more measurements are needed in order to improve the accuracy of the measurement.

2.5.3 The Digital Alternative

Although the method for detection of the time constant of the measured signal described above was historically implemented first, even then, it was realized that the signal information is contained *in the time variation* of the decaying transient. This means, that if the decaying transient is recorded itself and without noise, “no other experimental

method can possibly provide superior raw data” [161]. Indeed, the ability “to see” the recorded transient without noise allows the emission rate to be exactly determined at a *fixed* temperature by simply calculating the slope of the signal on a semi-logarithmic plot. This can be combined with filling pulse methods for measurement of the capture cross section [199] and the energy level position can be determined at a fixed temperature [176]), thus avoiding all the uncertainties associated with the thermal dependence of the capture cross section or energy level position [108]. We note this digital alternative in particular, since the new digital averaging techniques described in Chapter 3 are used to obtain, reduce significantly the noise, and record the transient itself.

2.6 CONVENTIONAL DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

As mentioned above, in real instrumentation, the capacitance decay waveform is corrupted with noise; indeed, it is sometimes even below the noise level. The essence of DLTS is the extraction of the waveform parameters in some automated manner from the noisy signal [16,138,199]. This is a correlation technique, which is a signal processing method where the input signal is multiplied by a reference signal, the weighting function $w(t)$, and the product is filtered (averaged) by a linear filter. In the conventional DLTS method (see Fig. 2.7), $w(t)$ is a *boxcar function*. The capacitance transient is monitored in two moments with delay times t_1 and t_2 from the start of emission pulse at $t = 0$, the difference is averaged and plotted versus the temperature T . The setup of delay times t_1 and t_2 determines the rate window $1/\tau$ of the system and τ is given by [138]

$$\tau = \frac{(t_2 - t_1)}{\ln(t_2/t_1)}. \quad (2.19)$$

As the temperature changes, the time constant for a given center $\tau_{n,p}$ changes according to equations (2.12) or (2.13) and, at some temperature T when $\tau_{n,p} = \tau$, the output signal of the boxcar averager reaches a peak corresponding to that center. In Fig. 2.8 a)

Figure 2.7 Setup for conventional capacitance-transient DLTS.

are shown examples of DLTS scans with different rate windows. By doing measurements with several rate windows, one obtains data points for an Arrhenius plot (Fig. 2.8b), from which the activation energies ΔE_t and the effective capture cross sections are extracted. Then, with t_1 , t_2 and ΔE_t known, the impurity concentrations are calculated from the peak

Figure 2.8 a) DLTS spectra with different rate windows defined with $1/\tau$.
b) Arrhenius plots of the traps in a).

magnitudes of the spectra. The great convenience of the DLTS spectrum is that during the experiment the spectrum gives a qualitative information on the relative concentrations and energy levels of several traps [199].

2.7 MAIN STAGES IN THE DLTS EXPERIMENT

Here, a more general view on the DLTS experiment will be presented. The logical sequence of events will be followed in order to distinguish and define the objectives at each stage of the measurement. The methods and instrumentation used to achieve these objectives will be discussed.

2.7.1 Excitation (Filling Pulse)

The main objective of the excitation is to fill all traps with carriers and to avoid re-emission of the trapped charge, thus ideally $n_t(0) = N_T$. The first condition is satisfied by increasing substantially the capture rate as compared to the emission rate. Since the capture rate is dependent on the concentration of free carriers [78,206], it is obvious that the excitation techniques are designed specifically to attract free charge in the vicinity of the deep levels. The simplest and probably the most effective technique is a bias pulse, which attracts free carriers from the quasi-neutral bulk of the semiconductor into a region that can be subsequently depleted. Since at room temperature and below, the reaction of the deepest levels is relatively slow, then the second condition is satisfied with applying relatively short filling pulses [161]. Therefore the name *filling pulse* in most cases means simply a forward, accumulation, strong inversion, or zero bias pulse [248,141,32,233].

When free carriers are not available, as in semi-insulating GaAs or other, heavily-compensated compound semiconductors, they must be created in some way and attracted near the deep levels. Most frequently, the excitation pulse is a direct [30,56,92,188] or indirect [1,132] “bandgap” light beam which generates electron-hole pairs near the traps. Since

both types of current carriers are created, there are complications related to electron-hole annihilation [256,257,24] and re-trapping of the emitted charge [9,10,132,228]. The need to create significant concentrations of free carriers requires intensive light which can be supplied by a laser beam, which was used, for example, to excite free carriers in high-purity, detector grade Ge [15] and Si [145]. Other methods used to excite free carriers are electron beam excitation using a scanning electronic microscope [20,89,183] and acousto-electric RF pulses [224,225].

Depending on the magnitude of the applied bias pulse, the intensity or wave-length of the light beam, or the focus bias of the electron beam the excitation can be non-selective (large-signal) or selective. Selective excitation occurs when only a small fraction of the traps in the volume observed during the emission pulse are populated. For example, when the filling pulse magnitude is small and very close to the reverse bias during the emission pulse, the Fermi level scans only a fraction of the interface traps. Thus, the acquired signal originates only from traps within a few kT above the steady-state Fermi level, which is a powerful tool for investigating the interface trap density [99,119,57,58,134,200,201,208,248]. An alternative technique is to combine two consecutive filling pulses with slightly different magnitudes in pairs, and to consider the difference in the corresponding emission pulses. This is a differential rather than selective population technique and is known as double-correlation or DDLTS [101,143]. This technique is useful for obtaining the deep level depth profile in the depleted region. For horizontal profiling, an electron beam in a scanning electron microscope can selectively populate only fraction of the traps in some particular area of the device [183].

2.7.2 Detection (Emission Pulse)

Detection techniques are based directly or indirectly on the transient phenomena discussed above in section 2.4. Their main objective is to convert the charge emission from the deep levels into measurable electrical transient signal which is almost exclusively a

voltage. For example, in the conventional DLTS technique, the capacitance transient is converted into a voltage transient by a custom built [140,239,20,164] or a commercial [263,262] capacitance meter. Capacitance meters are most commonly used for DLTS measurements. In our opinion, the latest model of Boonton Electronic. Corp. Boonton 7200 is the best available at this time [262]. Sometimes, a commercial capacitance meter can be modified to fit the DLTS application better [27,173,122]. Commercial capacitance meters are also part of commercial DLTS systems [264]. A compromise is made in selecting the test frequency of the capacitance meter. The need to integrate more pulses in a short time interval for better sensitivity and to obtain larger signal, limits the low threshold frequency at about 1 MHz. At the same time, the bulk resistance of the material and its associated series resistance, phase delays in the cables connecting the capacitance meter with the test structure inside the cryocooler, and skin effect require the test frequency to be kept not too high, usually below 10 to 20 MHz. It seems that 1 MHz, which is a standard frequency for high-frequency capacitance-voltage (C-V) measurements in MOS industry, has become widely accepted. The test level is most frequently 15 mV_{p-p}, but it can be selected at higher levels up to 100 mV_{p-p} [262].

A current transient is detected with a fast, large-gain amplifier, such as EG&G PAR 181 current sense amplifier [17] or a custom made circuit [242]. Detection of the current transient has been calculated to be about 10 times more sensitive than detection of the capacitance transient [187]. However, as mentioned earlier, current transient spectroscopy (CTS) [17,231,250] has two major disadvantages. First, there is no distinction between emission of majority and minority carriers. Second, the signal magnitude is dependent on the time constant. In addition to the transient current, the displacement current caused by the expansion of the SCR and leakage currents are present, and these currents create a dc level which is difficult to eliminate. Suppressing the parasitic transients associated with the transition from filling to emission pulse further complicates the measurement. In general, current transients are more difficult to analyze than capacitance transients.

To be precise, only capacitance and current transients are direct methods for observation of the charge emission from the deep levels. Charge measurements are in fact processing of the transient current with a simple integrator circuit [63,116]. The integration performed by a circuit similar to that shown in Fig. 2.9 eliminates the appearance of time constant in the denominator of (2.15), and then the more convenient expression can be used. In addition, the instrumentation is simpler and less expensive than a fast, sensitive capacitance meter or non-saturating current sense amplifier. Potential problems for the switching from filling to emission pulse can be eliminated, for example, by applying the methods described in Refs. [66,156] and the circuit can be further improved using analog memory circuits [122,204,238].

Figure 2.9 Integrator circuit for charge transient measurements.

Just as the charge transient is a result from electronic processing of the current transient, the voltage transient is obtained when the capacitance is maintained constant by an electronic feedback circuit [52,68,99,101,160,204,122] which is used in combination with a fast and sensitive capacitance meter. Unlike the charge transient circuit, this feedback circuit does not process the signal but it *changes the experimental conditions*, i.e. the applied bias. Because of the very high gain of the feedback circuit ($>1,000,000$), the actual capacitance change needed to produce the compensation voltage is negligibly small and the term

Figure 2.10 Setup for constant-capacitance voltage transient measurements CCVT.

'constant-capacitance' is completely justified. In Fig. 2.10, a setup for constant-capacitance measurements is shown. The reference capacitor C_f is set to be equal to the sample's capacitance during the filling pulse, and C_e is set to balance the sample capacitance during the emission pulse. Thus, when the switch SW alternates between two reference capacitors C_f and C_e connected to the differential terminals of the capacitance meter, the feedback amplifier OA produces a bias applied to the sample which is precisely the one needed to balance the corresponding reference capacitor. For dc and low frequencies, this feedback loop is negative, but for high frequencies, the delay introduced primarily by the capacitance meter, makes the feedback positive, causing large oscillations in the feedback loop. In order to avoid these oscillations, a low-pass RC filter is integrated into the feedback amplifier. This filter is adjustable, since the setup depends on the specific effective gain of the sample dV/dC , whose gain may vary with the temperature during the measurement.

During the filling or emission pulse, the capacitance is largely stable. If for some reason it changes, a compensation voltage is immediately produced by the feedback amplifier to compensate for the change. Thus, the charge emitted from the deep levels is pre-

cisely balanced by the voltage applied to the structure. This constitutes the voltage transient. Probably the most important consequence of maintaining a constant volume of the depleted region is the avoidance of the requirement that $N_t \ll N_d$ (equation (2.17) is valid for arbitrary N_t). This feature eliminates a severe restriction on sample purity and effectively solves the problems associated with a non-exponential transient analysis [40, 95, 202, 172, 184, 177, 241, 81, 115]. Furthermore, it allows deep level profiling to be implemented easily and regardless of the relative trap concentration compared to the doping concentration N_d . In [205], it was demonstrated how the constant-capacitance technique can be used for profiling simultaneously both the dopant and several deep traps by scanning the depleted region while varying the reference capacitor C_e . Similar scanning of the emission pulse level was also used for energy-resolved interface trap measurements [233].

Although the constant-capacitance technique is an indirect probe method, it is directly related to the emitted charge from the traps. There are many other indirect detection techniques which have much more complicated relations to the emitted charge. Conductance DLTS [32, 154, 155] detects the transient of the threshold voltage caused by charge emission from traps in the depleted region of a field-effect transistor by measuring the corresponding changes in the transconductance g_m . For the same purpose, rather than the transconductance, the variation in the drain current can be measured [85]. Although a less sensitive technique, it is possible to measure the small-signal conductance transient in high-resistivity samples and to relate this signal to the emitted charge from the traps [65]. Photovoltage [136, 165, 166] and Hall voltage [105] measurement have been also used in DLTS techniques to detect the charge emitted from the traps.

2.7.3 Averaging

The main objective of the averaging process is to improve signal-to-noise ratio (SNR) and possibly, to reduce the number of data points [127]. There are two main approaches at this stage of the experiment: analog and digital techniques. In analog tech-

niques, the averaging is performed simultaneously with the next step - transient analysis. For this reason, as a representative of the analog methods, here only the averaging function of a single boxcar averager will be discussed.

The equivalent circuit of a boxcar channel is simple - it is just a low-pass filter with a time constant $T_c = RC$ and a switch SW (Fig. 2.11). With the switch permanently closed, the response [251] v_o of the low-pass filter is

$$\frac{dv_o}{dt} = \frac{(v_{in} - v_o)}{T_c} \quad (2.20)$$

a)

c)

Figure 2.11 Averaging performed by a boxcar channel:

- a) equivalent circuit;
- b) transient with SW closed permanently;
- c) transient with SW closed only during the intervals T_a .

where v_{in} is the input voltage. If $v_o = 0$ then the response of a voltage step is similar to that shown in Fig. 2.11 b). If the switch SW is closed periodically with a period T_p only for a short time T_a which is called aperture, then the response is similar to that in Fig. 2.11 c). A dashed line in Fig. 2.11 c) shows the effective time constant T_{ceff} which has been increased T_p/T_a times. This allows for a substantial increase of the SNR. But more important is the fact that the sampling can be synchronized easily with the exciting pulse to give the averaged value in some particular moment after the beginning of the emission transient. In that way, by varying this delay time and waiting long enough for the averaging to become close to the actual value, the whole transient can be extracted from noise.

When the signal at the output of the detection instrumentation is digitized, then most frequently, a pre-selected number N of transients are averaged arithmetically by the system controller. Here, it is useful to remember that the SNR improves as $\sim\sqrt{N}$, so in most cases this number is set below 300. A new combination of averaging techniques which is a major contribution in this field is described in Chapter 3.

2.7.4 Transient Analysis

The ultimate goal of the DLTS experiment is extraction of the trap parameters from the components of the decaying transient. This is the objective of the transient analysis. Again, there are two main groups of analytical techniques: analog and digital.

Historically, the analog methods were implemented first. The filtering function of the “rate window” is a linear operation [161] over the emission rate $e(t)$ described by

$$e_o(Tp) = \int_0^{Tp} e_1(t)w(t)dt, \quad (2.21)$$

where $w(t)$ is known as a *weight function*. The boxcar averager [138], lock-in amplifier

[111] and exponential correlator [162] functions are the most commonly used. They are shown in Fig. 2.12. A good comparison has been reported in Refs. [53,162]. The boxcar function has a superior selectivity for traps with closely spaced time constants, but it has the worst SNR. At opposite, the exponential correlator has a superior magnitude sensitivity but a very poor selectivity for time constants. The lock-in amplifier's performance is between that of the boxcar averager and exponential correlator. Sometimes [42,162], the lock-in amplifier is considered to be equivalent to a boxcar averager with special setup. The preference in using a lock-in amplifier is given because it is easily available and inexpensive instrument. The main advantages of the analog methods are their high sensitivity and continuous control during the experiment. The main disadvantage is the necessity to conduct more than one thermal scan in order to collect data for the Arrhenius plots of the

Figure 2.12 Three most popular weight functions used for SNR improvement and transient analysis of analog DLTS signals.

traps. Other analog techniques rely on the analysis of the shape of the spectra [84,142,177], analog signal processing [232], or use more sophisticated weight functions to obtain better time-constant selectivity [6,40].

With the advancement of the computer and digital electronics, the popularity of the digital methods increases. For transient analysis, Spectral Analysis DLTS (SADLTS) [167,168], Fourier Transform Analysis [93,178,249], nonlinear least square fitting [81], the modulation function method [235], the method of moments [115,94], the correlation method of linear predictive modeling [203], the inverse Laplace transform [174], etc. are used. Isothermal methods are also gaining popularity, since the measurement is conducted at few fixed temperatures [63,255,219,176]. The main advantages of the digital methods are that they record the whole transient and that only one thermal scan is necessary for transient analysis. The main disadvantages are, in general, lower sensitivity and lower resolution of the magnitude.

In the transient analysis, the problem often is to separate the contribution to the transient response of two or more deep levels with comparable emission rates since they are signatures of different types of defects. Assuming that the transient signal is a sum of exponents with different magnitudes and time constants, the solution of this problem, in principle, is to perform inverse Laplace transform which produces a sum of delta functions with parameters the time constants of the traps [174]. Unfortunately, a well-behaved numerical method for inverse Laplace transform that can be used for DLTS does not exist. The main reason for this is that the exponential functions which are basic in the Laplace transform are not orthogonal along the real axis. In other words, the contribution of each exponent cannot be calculated in a simple way, as is done, for example, in the case of Fourier Transform Spectroscopy methods where the basic functions are sinusoids with constant magnitudes.

Still, an accurate algorithm for inverse Laplace transform was proposed to be adapted for DLTS analyses in Ref. [174]. There is an interesting discussion of the above problem which is illustrated with simulation results, showing that the rate window techniques used for analog transient analysis have inherently limited resolution, while the inverse Laplace transform has theoretically unlimited resolution. Unfortunately, the proposed algorithm for inverse Laplace transform is extremely sensitive to noise, which in practice, limits the resolution obtained from a DLTS signal with a typical signal-to-noise ratio to only about two times better values compared to that obtained using the best rate window technique. Since the averaging techniques proposed in Chapter 3 offer unprecedented improvement in the signal-to-noise ratio of the raw transient, this can be translated into a very high energy resolution by applying inverse Laplace transform for the transient analysis.

2.8 A NEW CLASSIFICATION SCHEME FOR DLTS METHODS

Since its introduction in 1974, a large number of variations and modifications of the DLTS method have been reported (for example, see Refs. in [199], chap. 7). Few and limited attempts for classification have been made [16,199]. In the previous sections, the main stages in the DLTS experiment and a large variety of techniques for each stage were presented. Obviously, when they are combined as appropriate, their diversity is very large. There are four main stages of the experiment which should be noted when classifying a technique: excitation, detection, averaging and transient analysis. For a detailed classification, the magnitude or the selectivity of the excitation pulse should be noted.

For example, the conventional DLTS technique introduced by Lang [138] is a: (1) large pulse, bias excitation, (2) capacitance detection, (3) boxcar averaging, (4) Arrhenius plot transient analysis technique. The acousto-electric DLTS [224,225] is an: (1) acousto-electric excitation, (2) transverse acousto-electric voltage (TAV) detection, (3) lock-in amplifier averaging (4) Arrhenius plot transient analysis technique. The transient spectros-

copy based on the Hall effect [105] is an: (1) over band-gap light excitation, (2) Hall voltage detection, (3) digital averaging (4) Arrhenius plot transient analysis technique.

From the above, it is clear that for designing an appropriate technique, most important are the choices of (1) and (2), while (3) and (4) depend more on the availability of instrumentation and sometimes, on personal preferences. It is also obvious, that (3) and (4) can be fixed and only (1) and (2) can be varied to fit the specific properties of the investigated material. In this sense, the choice of (1) and (2) in most cases can be considered specific to the experiment, while the choice of (3) and (4) refers to the data processing methods used. The following chapters in this thesis describe a new feedback circuit and a new detection technique, thus both related to (2), and new averaging techniques, which improve and enrich the choice for (3).

2.9 OTHER METHODS AND COMPARISONS WITH DLTS

Besides DLTS, there are many other techniques for characterization of deep level traps located in the bulk of the semiconductor or at the interface between two materials. In the silicon industry, for example, *charge pumping* [75] is more popular than DLTS because this method can be applied as a wafer level reliability test. Originally, the charge pumping technique was designed to give the total interface trap concentration N_{it} of an MOSFET. With modified bias pulses which allow the traps at the Si-SiO₂ interface to be selectively populated, D_{it} and $\sigma_{n,p}$ can be measured and D_{it} sensitivity up to $\sim 10^9 \text{eV}^{-1} \text{cm}^{-2}$ can be achieved. The method is applicable mainly for interface traps more than $\sim 0.2 \text{eV}$ from the midgap of Si and is restricted only to a specific group of devices. DLTS is applicable to a wider range of devices and offers alternative methods for energy resolution, allowing D_{it} to be measured. In addition, DLTS using MOS devices can measure traps closer to the midgap and is not restricted only to the interface region. Charge pumping can be used to obtain spatial profiles of N_{it} along the MOSFET channel [135,148,149]. DLTS can be used also for measurement of spatial profiles of a particular discrete trap or D_{it} along the channel [99,

123,183]. Significant advantages of the charge-pumping techniques are its technical simplicity, high sensitivity for small gate area devices and no need for temperature variation in large temperature interval. As compared to the current DLTS, it may have higher sensitivity and simplicity because the integration of the trap response occurs *in situ*, i. e. the signal is an averaged response of the interface traps and only a DC current meter is required. Drain current DLTS requires a fast current meter or a feedback circuit plus a voltmeter and additional hardware/software averaging and filtering. In general, most of the selective trap filling charge-pumping techniques used for energy resolved detection are applicable with some form of DLTS as well, which can supply additional information.

For investigation of the interface traps at the Si-SiO₂ interface, *quasi-static capacitance-voltage (C-V) method [133] and high-low frequency C-V method [173]* are still very popular and are often used as routine characterization techniques in VLSI development and production. For these methods, there is an industry standard and high quality instrumentation is readily available. D_{it} sensitivity for a good system is usually around $\sim 10^{10} \text{ eV}^{-1}\text{cm}^{-2}$. Like the charge-pumping technique, change of the temperature is not required and the integral response of the interface traps is measured. However, there is an inherent energy resolution since only the response of those traps in the vicinity of a few kT/q around the Fermi level are detected. It can be compared with a DLTS which uses the Fermi level as a probe to obtain energy resolution [99,119,120] but it also needs surface potential calculations in order to relate the gate bias to the Fermi level at the silicon surface. Both C-V methods and small-signal DLTS are sensitive to the surface potential fluctuations. Large signal DLTS with selective trap filling can be used to avoid the surface potential fluctuation or the fluctuation can be extracted from a curve fitting of $\Delta V_G(V_G)$ [119]. Quasi-static method scans almost the entire bandgap without any interruptions in the mid-gap region and only a MOS capacitor is needed. DLTS requires a minority carriers source for scanning both sides of the bandgap and fails around the midgap because of generation of current carriers opposite to those emitted from the interface traps. C-V methods require a

high quality electrometer, are sensitive to leakage currents, and apply to MOS structures. DLTS method can be more sensitive (about $\sim 10^9 \text{ eV}^{-1}\text{cm}^{-2}$), is less sensitive to the leakage currents and can be applied to various test structures. Combining quasi-static C-V and DLTS methods gives more complete results for D_{it} because DLTS covers ranges of the bandgap where uncertainty in calculation of the surface potential affect strongly the accuracy of the quasi-static measurements.

Conductance-voltage (G-V) method (sometimes called impedance spectroscopy) [173], is based on the measurement of the parallel conductance component G_p of a MOS capacitor as a function of bias and frequency. The conductance G_p results from the interface capture and emission of carriers, and is a measure for interface trap density. Conductance method is highly sensitive $\sim 10^9 \text{ eV}^{-1}\text{cm}^{-2}$, gives the capture cross section for majority carriers, but is tedious, time consuming and gives D_{it} close to the bandgap edges, but not in the midgap region. It is also sensitive to the surface potential fluctuations. With elaborate procedures, the effect of these fluctuations can be estimated by fitting curves to the experimental data. A similar approach is used in the small-signal DLTS [119]. Because of the similar sensitivities, conductance and conventional DLTS method are considered to complement each other; for time constants faster than one millisecond, the conductance method is used and for slower time constants, DLTS is used [119]. Similar to the conductance method, the transconductance method is one which can be used for MOS transistor measurements [38].

Except for the conductance method, the methods listed above are designed to measure the deep levels in the surface region of the device. For bulk deep levels, **thermally stimulated capacitance (TSCAP) and current (TSC)** measurements were used before the introduction of DLTS [25,173]. They are compared as a DC analog of DLTS and because of their low sensitivity ($n_i > 0.1 N_d$) and limited range ($\Delta E > 0.3 \text{ eV}$), they have been largely replaced with DLTS [199]. For the special case of measurement of charge coupled devices

(CCDs), *charge transfer efficiency* can provide valuable information about the deep levels [82,83,169].

Optical methods as *photoluminescence (PL)* can be applied only to those impurities for which radiative recombination has been observed [199]. Because of the high sensitivity of the detection instrumentation, PL can be used even when radiation is dominated by another recombination mechanism. Compared to DLTS, PL allows easier impurity identification, but is more difficult for concentration measurement. Non-radiative bulk and surface recombination complicate correlation of a given PL spectral line with the concentration of the impurity corresponding to that line. The sample's volume detected by PL is determined by the absorption depth of the exciting laser light and the diffusion length of the minority carriers, and this does not allow for deep level profiling. In some cases, PL can complement DLTS as a tool for investigation of the shallow levels but that is complicated because of the different test structures used for PL and DLTS. PL has the advantage of being a non-destructive, contactless method, which allows deep level mapping on large area samples. It also requires complex and very expensive instruments such as argon ion laser, helium refrigerator, spectrometer and photon counting and detection system [199].

Recently, *low-frequency noise measurements* of current or voltage noise spectrum are also used for characterization of deep levels [36,44,46-51,104,129,169-171,236]. The total noise is regarded as a superposition of noises originated in several noise sources [36, 44]. The thermal and shot noise are considered to be fundamental sources whose contribution can be minimized by appropriate device design and operating conditions such as bias and temperature. Added to those sources are excess noise components as flicker ($1/f$), generation-recombination (G-R) and random telegraph signal (RTS) noises. These three sources are common for many devices, and their spectral densities and amplitude distributions are well defined [236]. The intensity of the G-R noise is proportional to the concentration of the electrically active deep levels and at given temperature, it peaks at some

characteristic frequency, depending on activation energy of the deep level. The variation of the peak with the temperature then gives the Arrhenius plot. At a some other temperature, the actual peak may be above the observation limit of the measuring instrument and then the results may be incorrectly interpreted. This is a Fermi level probe method and can be compared to the small-signal variations of the DLTS.

In Table 2.2, some of the most popular techniques for interface and bulk deep level measurements are summarized.

Table 2.2: Comparison of DLTS with different methods.

Method	Bulk sensitivity [cm ⁻³]	Surface sensitivity [cm ⁻² eV ⁻¹]	Energy range	data for σ	Temp. scan needed	Test device	Deep levels	Interface states	Optical properties
DLTS methods	$\sim 10^9$	$\sim 10^9$	$E_c - 0.1$ eV ~ midgap ~ $E_v + 0.1$ eV	+	+	space-charge region; resistor; MOS structure;	+	+	+
C-V methods	N/A	10^{10}	$E_c - 0.1$ eV ~ $E_v + 0.1$ eV	+	-	MOS capacitor	-	+	-
charge pumping	N/A	$\sim 10^8$	$E_v + 0.1$ eV ~ midgap	+	-	MOS transistor	-	+	-
G-V method	N/A	$\sim 10^9$	$E_v + 0.05$ eV ~ midgap	+	-	MOS capacitor	-	+	-
Low-freq. noise method	N/A	N/A	$E_c - 0.1$ eV ~ midgap	+	a few points	same as DLTS	+	-	N/A
CCD's charge	N/A	$\sim 10^{10}$	$E_c - 0.05$ eV ~ midgap (minority cc.)	+	a few points	CCD	-	+	~ -
TSCAP	$> 0.1 N_d$	N/A	$\Delta E > 0.3$ eV	+	+	same as DLTS	+	-	+
TSC	$> 0.1 N_d$	N/A	$\Delta E > 0.3$ eV	+	+	same as DLTS	+	-	+

CHAPTER 3

AVERAGING AND RECORDING OF DIGITAL DLTS TRANSIENT SIGNALS

3.1 INTRODUCTION

Since the introduction of deep-level transient spectroscopy (DLTS) in 1974 by Lang [138], the method has been refined many times with new techniques for improving the sensitivity and accuracy, for adapting DLTS to the specific properties of new types of samples, and for simplifying procedures for measurement and data analysis. At present, DLTS is comprised of a large group of different measurement techniques applied to a variety of test devices and materials, and is considered to be among the most accurate and reliable tools for investigating the properties of electrically active point defects in semiconductors [12,199].

Because of the great variety of DLTS techniques and numerous possibilities for their combination, any attempt at a detailed classification easily becomes a formidable task. Nevertheless, in all these techniques, there are several common features identifying the technique as of DLTS type. First, it is a time domain measurement of a relaxation process, most often the emission of charges trapped in electrically active centers. Second, the process is considered to be thermally activated and the validity of the Shockley-Read-Hall theory [206,78] is assumed. Third, there is periodic alternation between filling of the traps with charge (filling pulse) and emission of the trapped charges (emission pulse). This last feature is used for synchronized measurement and integration - a basic method used for signal recovery from noise in electronic instrumentation [251]. The increased sensitivity, allowing detection of a signal immersed in noise, is the major advantage of DLTS over the previously used thermally stimulated current (TSC) [55], or thermally stimulated capacitance (TSCAP) [26] methods for the study of deep levels in semiconductors [195,196,197].

3.2 TECHNICAL OVERVIEW OF THE DLTS EXPERIMENT

The DLTS experiment can be regarded as a sequence of several steps. The first step is to populate the traps in the investigated volume with charges. The second step is to detect the change of the trap occupancy with electrons as a measurable change in some electrical parameter of the test structure. In classical DLTS, this is the small-signal high-frequency capacitance. The next steps are synchronous detection and averaging of this signal in order to improve the signal-to-noise ratio (SNR). There are two main approaches at this stage of the experiment - use of analog or digital signal processing methods (Fig. 3.1).

Figure 3.1 Classification scheme of the signal processing of DLTS transients. The shadowed areas indicate where the averaging techniques presented in this chapter belong.

3.2.1 Analog Methods

The noisy transient signal can be measured and integrated over many pulses using analog instruments such as a boxcar averager [138], a lock-in amplifier [111], or an exponential correlator [162]. In the classical setup, two boxcar channels are used to measure the signal at two different times in the transient, and these times define a time constant window of the instrumentation [138,161]. The averaging is performed by two boxcar channels and the difference of the signals from these channels versus the sample temperature is recorded, giving a DLTS spectrum. When the emission time constant of a deep level coincides with that of the instrumentation while scanning the temperature of the sample, the output signal indicates this coincidence with a peak in the spectrum. To apply the Arrhenius relationship to determine the energy level and the capture cross section of a trap, several temperature scans are needed using different settings of the time constant window of the instrumentation. Similarly, it is necessary to change the pulse frequency when using a lock-in amplifier, or the reference time constant when using an exponential correlator, and to repeat the temperature scan in order to obtain enough data for the Arrhenius plot technique. In all these cases, the averaging technique simultaneously achieves two different goals - increasing the SNR and analyzing the transient parameters.

One serious disadvantage of the analog techniques is the need to perform more than one temperature scan. This practical difficulty can be eliminated, for example, by using more complex (and more expensive) instrumentation, or by analyzing the shape of the DLTS spectrum [90,212,216] instead of just finding the peak temperature. Other disadvantages of the analog methods are their inherent limitations in resolving closely spaced energy levels of defects, and difficulties associated with the analysis of non-exponential transients. Nevertheless, the analog methods are simple to implement, they produce an analog signal in real time during the experiment, and plotting this signal versus the temperature gives spectra which are available for immediate interpretation.

3.2.2 Digital Methods

While the analog methods produce an integrated response to the transient signal, digital methods record the whole transient as a set of data points. The noisy signal is first digitized and then processed using various digital techniques [4,28,54,81,86,91,94,93,96,98,115,150,167,168,178,203,235,249,259]. Analysis of the transient parameters can take place during the experiment, or data can be stored for analyses later. In common with the analog methods described above, the transient can be digitally correlated with a boxcar, lock-in or exponentially decaying function, and used to build a set of DLTS scans [54]. Alternatively, the transient can be analyzed using Spectral Analysis DLTS (SADLTS) [167, 168], Fourier Transform Analysis [93,178,249], nonlinear least square fitting [81], the modulation function method [235], the method of moments [115,94], the correlation method of linear predictive modeling [203], or other digital methods described, for example, in Ref. [14]. Since the whole transient is recorded, then it is necessary to perform just one experimental temperature scan, and this greatly reduces the time needed to perform the experiment. This is a major advantage over the analog methods, in addition to the extensive possibilities for analysis.

However, digital methods have disadvantages as well. Because the whole set of data points representing the DLTS transient is recorded for each temperature, the total number of stored data points can be very large compared to that recorded using analog methods. Consider for example a digitizer fast enough to study transients with time constants below 0.5 ms. Commonly available 12-bit analog-to-digital converters (ADC) with conversion time below 10 μ s, which interface directly to a PC, are suitable for that purpose and their cost is below \$10. If operated at rate of 33.3 kHz, the time spacing between the data points would be 30 μ s and, for simultaneous observation of slow transients with time constants in the tens of milliseconds range, there will be several thousand samples for one transient recording. For example, if the emission pulse is 90 ms, there will be 3000 samples for each transient recording. If the transient is recorded in one degree intervals over a tem-

perature range 50 to 350 K, there will be a total of 900,000 samples, which occupy 1.8 Mbytes of disk space (each 12-bit sample occupies two bytes).

The problem, however, is not so much the required disk space, but rather the difficulties in processing this large amount of data, since many of the digital methods involve iterative numerical calculations. The need to transfer 6 kbytes of data in just 90 ms is one more obstacle when the system is based on IBM PC and the processor operates in real mode, known also as MS-DOS mode. Another disadvantage of the digital methods, as compared to analog methods, is the decreased SNR for long delay times. Assuming constant noise, as the transient progresses, the signal decay leads to decreased SNR at the input of the signal processing apparatus. The analog methods have various ways of dealing with this problem. The boxcar technique enables one to compensate for the decreased SNR by increasing the sampling aperture of the channel which is recording the second time delay point [115,42]. In the lock-in technique, an integral of the transient is processed and the high SNR at the beginning of the transient is averaged with the low SNR at the end. The correlator reference function, which multiplies the noisy signal transient before integration, also decays along with the signal, thus minimizing the influence of the low SNR at the end of the transient. However, in a digital system, the sampling aperture of the ADC remains constant, and so the SNR decrease in the tail of the transient cannot be compensated for.

In general, both analog and digital DLTS signal processing techniques are mainly focused on the transient parameter extraction and on the ability of the method to resolve closely spaced energy levels of defects. Averaging to improve the SNR is considered important, but is a secondary task. While in the analog techniques these two tasks are merged, in the digital techniques, the transient analysis is separate and usually performed *after* some simple digital averaging is done. Most often, this is the multiple time averaging of a selected number of successive transient recordings [54,167,168,178,81,115] and this number is usually in the range 100-300. This technique has three disadvantages. First, there

is a need to allocate a memory buffer large enough to accommodate the selected number of transients. In the above example it takes more than 300 kbytes, or approximately half of the conventional memory of an IBM PC. Second, after averaging, the buffer is cleared for processing of the new transient, and the old information is lost, thus making it more difficult to maintain high SNR. Third, the progress of the summed transient is not monitored as it accumulates in the allocated buffer and, if anything goes wrong and some adjustment and a restart are needed, one is not aware of the problem until the full sequence of the selected number of transients has been accumulated.

In our approach [126], we consider averaging of the noisy DLTS signal as a *separate* task from the extraction of the transient parameters. We present two different, but complementary averaging techniques offering an increased time resolution for short delay times, improved signal-to-noise ratio for long delay times, and more efficient data storage. In addition, the transient and the DLTS scan are available in real time for continuous observation and data analysis after the acquisition of each single transient.

3.3 PSEUDO-LOGARITHMIC AVERAGING

3.3.1 Theory

For detailed observation of an exponentially decaying signal, short sampling intervals are needed at the beginning of the transient, while much longer intervals are sufficient at the end. At the same time, high SNR of the processing instrumentation is much more important at the end of the transient, where the signal is weak, as compared to the beginning of the transient, where the signal is strong. One way to partly to fulfill these requirements is to use a high sampling rate and short emission pulse at high temperatures, and to lower the rate and increase the emission pulse width at low temperatures [178,81]. This is easily done by using a programmable digital scope as a digitizer. Although this approach doesn't allow the simultaneous monitoring of both fast and slow transients, it is still possi-

ble to optimize the time resolution setting of the measurement system for a given time constant of interest.

A much better way to satisfy the time spacing requirements is to use sampling with a logarithmic time base. This approach is not new in DLTS experiments. Morimoto et al. described selecting from the measured 512 data points a set of 195 data points having almost logarithmic time distribution [167,168,93]. The data points in [243] also appear to have a logarithmic time spacing. To our knowledge, the best published work on this subject is described in Ref. [54] where a high, but constant ADC sampling rate is used, all sampling results are transferred to the computer memory, and pseudo-logarithmically spaced data point are selected by specially written software. The pseudo-logarithmic storage scheme in [54] uses a logarithm with base 2 because of the ease of unsigned integer division by 2^n in binary arithmetic [64]. This simplicity is equally advantageous in hardware logic circuits and is used in our scheme as well. Another, probably less obvious advantage is the fact that the function 2^n is closer to $\exp(n)$ than the commonly used 10^n . In our system, the sampling rate is 100 kHz and therefore, the sampling intervals Δt are spaced 10 μ s apart. If the data is averaged over time intervals t_n , with each one twice as long as the preceding one, the second averaging interval is $2\Delta t$, and the n^{th} averaging interval starts at

$$t_n = (2^n - 1)\Delta t. \quad (3.1)$$

If, for convenience, we number the intervals starting from zero, which is a commonly used standard in programming and digital electronics, for $2^n \gg 1$ the index n can be expressed as

$$n \approx \log_2(t_n/\Delta t). \quad (3.2)$$

This represents a logarithmic dependence of the interval index on the interval time length, since the sampling interval Δt is fixed by the constant sampling rate of the ADC.

Unfortunately, the pseudo-logarithmic storage scheme proposed in Ref. [54] has several disadvantages. First, it is still necessary to allocate very large memory buffers, as the data points are selected after the full set of transient sampling points is recorded into the computer memory. Sampling each $10\ \mu\text{s}$, there are 131,072 sampling points which are stored into a 256-kbyte buffer. From this large set of data, only 768 data points are selected and used, while the remaining 130,304 points are discarded. Second, more buffers are needed for the multiple time averaging of successive transients as described above, and the result is available for observation *after* the selected number of transients are averaged. Third and most important, there is a substantial decrease in the SNR, especially in the tail of long transients, where the data point intervals are in the millisecond range, because the data points are selected from just $10\ \mu\text{s}$ long sampling intervals. In addition, recording of 768 data points for each degree in the 50 to 350 K range still requires almost 0.5 Mbytes disk space. Also, Direct Memory Access (DMA) transfer into memory blocks larger than 64 kbytes is complicated, since it requires continuous initialization of the DMA controller for crossing the memory page boundary [194].

The main difference between our pseudo-logarithmic averaging scheme and that described in [54] is the method of obtaining the data points. In Ref. [54], the data points are *selected* from the large set of sampling points, but in our system, the data points are *averages of the sampling points* inside the averaging intervals, which increase in a pseudo-logarithmic manner [7]. In this way, *all measured samples are used*. Although our electronic circuit implementation is different, the averaging principle (Fig. 3.2) is the same as in [7]. The logarithmic time spacing algorithm described above gives only about three data points per decade. To increase this number, the length of the averaging interval in the pseudo-logarithmic averaging scheme is doubled after a pre-selected number M of averaging operations, thus producing a linearly spaced train of M averaging intervals. In this way, the pure logarithmic time spacing is mixed with linear time spacing, and hence the name *pseudo-logarithmic*. The sampling interval remains the same, $10\ \mu\text{s}$ in our system, and the result is

Figure 3.2 Pseudo-logarithmic time averaging scheme. After each 5 data points the number of averaged samples 2^n doubles as n increases by 1.

a sequence containing $(N + 1)$ groups of averaging intervals m_n . Inside the group n , each interval m_n has the same length, but it is twice as long as an interval from the preceding group m_{n-1} , or half of the time of an interval from the succeeding group m_{n+1} . Since the maximum number M of averaging intervals m_n inside each group is the same for all the groups, the time lengths of the groups change in the same way. Therefore, we have $(N + 1)$ groups each one containing M equal averaging intervals m_n , but with the time length of the groups increasing as 2^n .

3.3.2 Error Analysis

At a first glance, this scheme for averaging of the sampling points may be understood as an approximation of the exponentially decaying function with a set of straight

lines connecting the obtained data points (picewise linear approximation). Indeed, the obtained set of data points does not contain explicitly any information about the time intervals between the data points - this information remains hidden in the summing results from which the data points were obtained. However, the data points themselves were obtained by summing of *the true experimental signal*, sampled each Δt , and dividing the result by the number of the samples in the averaged interval. For a given group with an index n , the largest error is always expected to occur in the first of the averaging intervals m_n with $m=1$, where the signal varies more rapidly as compared to its variation during the subsequent intervals from the same group with $m>1$. Therefore we need to consider only the worst case when the averaging is done from $ts_{n,M}=\Delta t \cdot M \cdot (2^n-1)$ to $te_{n,M}=\Delta t \cdot M \cdot (2^n-1)+\Delta t \cdot 2^n$. The result of the averaging process is assigned to the middle of the averaging interval defined as $tm_{n,M}=\Delta t \cdot M \cdot (2^n-1)+\Delta t \cdot 2^{n-1}$. Thus, the error function $Err(\tau)$ can be obtained by subtracting the magnitude obtained by averaging of the exponentially decaying function in this interval from the exact magnitude in the midpoint $tm_{n,M}$ as

$$Err(\tau) = C \cdot \exp\left[-\frac{tm_{n,M}}{\tau}\right] - \frac{C}{2^n} \cdot \exp\left[-\frac{ts_{n,M}}{\tau}\right] \cdot \sum_{i=1}^{2^n} \exp\left[-\frac{\Delta t}{\tau} \cdot i\right] \quad (3.3)$$

where C is the transient magnitude at the beginning of the transient. When $Err(\tau)$ is plotted versus τ for a given set of Δt and M , this function exhibits one sharp maximum at some τ_{m+} , which dominates short time constants for small n . At long time constants, this maximum is compensated for by another sharp minimum which begins to dominate for large n at some $\tau_{m-} < \tau_{m+}$. Away from these peaks, the error function is close to zero. We find these particular τ_{m+} and τ_{m-} by setting the first derivative versus τ equal to zero and solving numerically (appendix A) with convenient choice of the initial guess value for τ

$$\begin{aligned} & \frac{-C\Delta t}{\tau^2 \left(\exp\left(\frac{\Delta t}{\tau}\right) - 1 \right)^2} \cdot \left[(\gamma_{n,M} - 1) \cdot \exp\left(-\frac{te_{n,M}}{\tau}\right) - (\gamma_{n,M} - 2^{-n} - 1) \cdot \exp\left(-\frac{te_{n,M} + \Delta t}{\tau}\right) + \dots \right. \\ & \left. \dots + (\gamma_{n,M} - 2^{-n}) \exp\left(-\frac{ts_{n,M} + \Delta t}{\tau}\right) - \gamma_{n,M} \exp\left(-\frac{ts_{n,M}}{\tau}\right) \right] - \frac{Ctm_{n,M}}{\tau^2} \exp\left(-\frac{tm_{n,M}}{\tau}\right) = 0 \end{aligned} \quad (3.4)$$

where $\gamma_{n,M}$ is $M(2^n - 1)$.

Next, we replace the values obtained for τ_{m+} and τ_{m-} in (3.3) which gives the maximal errors $Err(\tau_{m+})$ and $Err(\tau_{m-})$ when using the averaged values in the m_n interval with $m=1$. This function was normalized relative to the initial magnitude C and plotted against τ_{m+} and τ_{m-} in Fig. 3.3 with parameters n and M for two values of Δt . There are two distinct reasons for the errors in this pseudo-logarithmic scheme.

First, the limited speed of the ADC gives an error which is strictly dependent on the sampling interval Δt , in our case $10 \mu s$, and it does not depend on the number of the aver-

Figure 3.3 Normalized absolute magnitude and time constant errors plotted versus the time constant τ_{max} at which these errors occur. The straight lines indicate independence from the group number n or number of equal averaging intervals inside the group M and dependence only on the sampling rate. Inverted triangles indicate sampling with 1 MHz rate and $M=10$. The right line with hollow symbols gives the errors in determining the time constant error sampling with 100 kHz.

aged samples 2^n or the number of the equal intervals inside the group M . This gives the straight line which demonstrates increased error for short time constants. Obviously, this error is not inherent to the pseudo-logarithmic averaging, and can be decreased only by using faster ADCs. The second type of error is more pronounced for longer time constants and it depends much more on M than on 2^n . Fig. 3.3 demonstrates that for time constants longer than 1 ms the errors are below 0.1% if the groups are divided into five or more averaging intervals. Calculations with a 10 times faster ADC sampling rate show a 10 times reduction of the errors for fast time constants.

For the transient analysis, it is attractive to use a boxcar function obtained simply by subtracting two data points with time delays t_1 and t_2 . Since each data point represents an average with time width W , it is interesting to evaluate the error in defining the rate window. We follow the procedure outlined in [42] with a slight modification. Instead of integral averages, we use summing averages in order to accurately model the actual function of our circuit, and to account for the limited rate of the ADC. Furthermore, we subtract only the first sub-intervals in two adjacent groups where the maximal error is expected to occur. The normalized output $S(\tau)$ is then given by

$$S(\tau) = \frac{C}{2^n} \exp\left[-\frac{tm_{n,M}}{\tau}\right] \cdot \sum_{i=1}^{2^n} \exp\left[-\frac{\Delta t}{\tau} \cdot i\right] - \frac{C}{2^{n+1}} \exp\left[-\frac{tm_{n+1,M}}{\tau}\right] \cdot \sum_{i=1}^{2^{n+1}} \exp\left[-\frac{\Delta t}{\tau} \cdot i\right]. \quad (3.5)$$

We find the rate window by differentiating $S(\tau)$ with respect to τ and setting the result equal to zero. The solution can be found numerically (Appendix B) to give τ_{max} . We calculated τ_{max} for variations of n and M and compared the values with those obtained using the Lang's expression using the midpoints of the averaged intervals, which is

$$\tau'_{max} = \frac{tm_{n+1,M} - tm_{n,M}}{\ln(tm_{n+1,M}/tm_{n,M})}. \quad (3.6)$$

The normalized error in determining $\tau_{err} = (\tau'_{max} - \tau_{max}) / \tau_{max}$ is also shown in Fig. 3.3.

One should mention that because of the logarithmic dependence from τ on the Arrhenius plot errors for τ in the range of 1% can be ignored [42].

3.3.3 Implementation

There are two possible ways to implement the averaging scheme described above. It might be possible to use the same hardware as described in [54]. Instead of selecting only 768 data points from the whole set of sampled points, fast software could be used to change the length of the averaging interval, perform the actual averaging of the sampled points inside the interval, and store the corresponding data points. Expression (3.3) could give the starting point for such an implementation. There are two potential problems with this approach. First, there may be some difficulties with the processing during the first three groups, when there is no averaging or only 2 or 4 samples are averaged per data point. In real mode of the processor, fast data transfer can only be done with Direct Memory Access (DMA). Since the DMA process actually “steals” cycles from the PC processor, an intensive DMA transfer can considerably slow down the program execution [194]. Thus, the DMA transfer can cause timing conflict with the real-time averaging routines. Therefore, we give preference to the hardware implementation shown in Fig. 3.4.

In our circuit, one can distinguish four functional blocks: an ADC, a pseudo-logarithmic pulse generator, an averager, and an interfacing block. The ADC operates continuously at a fixed rate of 100 kHz. The pseudo-logarithmic pulse generator (Appendix C) is constructed from programmable counters and shift registers. It incorporates a programmable divider of the clock frequency which is set at the beginning of the transient to divide by 2^0 , since for the first group $n=0$. Of course, in practice this means no division at all, since $2^0=1$. When the counter of linear pulses m reaches a predetermined number M , it is cleared to start counting again, and this produces a logarithmic pulse n , thus changing the setup of the programmable divider to 2^1 . This doubles the time between each one of the next M pulses. When the linear pulse counter reaches M again, n increments by one, and this sets

up the divider to divide the clock pulses by 2^2 . This sequence is repeated until the logarithmic pulse counter reaches the software-programmed number of groups N .

The averager is made by combining an accumulator, shift register, and a programmable down counter. The End-Of-Conversion (EOC) signal from the ADC triggers an adding operation which adds the result from the current conversion to the stored sum of the previous conversions. This accumulation of conversion results is repeated over the whole length of the averaging interval. When the new linear pulse arrives, it stores the accumulated result into the shift register, which must be large enough to accommodate the whole sum. Then the accumulator is cleared for storing the new sum while the result in the regis-

Figure 3.4 Block diagram representation of pseudo-logarithmic time base averaging circuit.

ter is divided by 2^n by being shifted right n bits by the down counter. Since the down counter is programmed by the same logarithmic pulse counter n , which is programming the clock frequency divider to divide by 2^n , the accumulated results are always properly divided.

After the averaging operation is over, an interfacing circuit signal requests the DMA controller of the PC to transfer the averaged result to the specified memory location. After the last result from the last octave is transferred to the PC memory, the logarithmic pulse counter is cleared and ready for the next transient. Simultaneously, the interfacing circuit produces a signal which triggers a hardware interrupt routine for performing the second averaging technique described later in this chapter. The operation of the whole circuit is synchronized by a 16 MHz system clock, and the ADC sampling frequency is obtained by dividing the system clock frequency by 160.

The maximum allowed numbers for N and M depend on the hardware circuit. In our system, $N_{max}=12$ and $M_{max}=16$ which gives a total of 208 pulses (13×16 , since N starts from zero). This is enough to store transients up to 1.3 s long, with 10 μ s and 20 μ s resolution, and with 32 data points in the first 0.5 ms. In addition, we have a programmable delay of up to 160 μ s in order to compensate for possible slow response of the capacitance meter. The intervals in the last group are 40.96 ms long, each one averaging 4096 samples. Therefore, the expected SNR improvement is $\sim\sqrt{4096}$ or 64 times [251]. However, it refers to points *inside* the averaging interval and not for the whole transient, and this implies that the SNR improvement will be less for low-frequency noise. If we use the averaging scheme proposed in [54], then each data point from the last group (the second half of the transient) would be just one selected ADC sampling result out of 4096 ADC samples. In our averaging scheme that same data point represents an average of 4096 ADC samples. This gives a major advantage of our averaging technique for long delay times over the previously used technique. Another advantage is the storage efficiency. Because of the signif-

icant SNR improvement, even long transients can be recorded with just 208 points and the disk storage space for a DLTS scan in the range 50 to 350 K occupies less than 125 kbytes. Other advantages are the reduced size of the required buffers (in our system we allocate just two 420-byte buffers) and the large amount of available time for the microprocessor to process and display the results while the measurement is in progress.

3.3.4 Demonstration

In order to demonstrate the benefits of using the proposed pseudo-logarithmic averaging scheme, we recorded a real DLTS signal when our system was operated in constant-capacitance mode. We used an analog memory feedback [122] which eliminates the distortion of the voltage transient introduced by the integration of the voltage step from the filling to the emission pulse, and provides a stable zero baseline [204]. This feedback was used in combination with a Boonton 7200 capacitance meter. The measured sample is a p-Si MOS capacitor with insufficient annealing after the ion implantation for correction of the threshold voltage. More details can be found elsewhere [122]. The traces in Fig. 3.5 were recorded using DMA transfer and a commercially available data acquisition board. Trace a) appears in the same way as the signal seen on the oscilloscope screen, and trace b) was obtained with multiple time averaging of 32 consecutive transients. This trace gives an idea of the expected improvement in SNR using a simple averaging technique. It should be noted that real-time observation of these traces on the computer screen was impossible. Also, we demonstrate our system mainly with a relatively weak DLTS signal and with 60 Hz electromagnetic interference present, in order to demonstrate better the complementary action of both averaging techniques presented in this chapter. For the same reason, we intentionally recorded transients longer than normally used in DLTS. In Fig. 3.6 are shown four traces. The trace denoted with $k=0$ (k will be defined later) was obtained using only pseudo-logarithmic averaging. At first glance, the advantage of using this technique alone is not obvious. Although the noise magnitude inside the averaging intervals is significantly reduced, the trace shape is substantially different from the expected exponentially decaying

Figure 3.5 a) Original signal sampled each 0.2 ms with 12-bit resolution; b) same signal after multiple time averaging of 32 consecutive transients.

transient. The reason for this unsatisfactory result is because the pseudo-logarithmic averaging technique is used *inside* the averaging intervals and therefore, it cannot suppress low frequency noise components. However, note the transition to longer averaging intervals around 320 ms and its effect on the curve shape. In order for the above digital averaging circuit to operate properly, it must be assured that essentially all the averaged transients are inside the limits of the ADC. We use a digital-to-analog converter to display the averaged data points on the oscilloscope screen, which helps us to detect ADC input overloading.

3.4 CONTINUOUS TIME AVERAGING

3.4.1 Theory

The pseudo-logarithmic averaging proposed above is a very efficient technique for

Figure 3.6 The signal of trace a) in Fig. 3.5 after pseudo-logarithmic time averaging alone for $k=0$. For $k>0$, pseudo-logarithmic time averaging is combined with continuous time averaging with time constants 2^k . The inset shows good time resolution during first 2 ms with $k=3$.

reducing the number of data points and for SNR improvement at relatively high frequencies and large delay times. However, it needs to be complemented with another averaging technique which can suppress low frequency noise components and improve the SNR at the beginning of the transient. We found that continuous time averaging [251] is a very convenient technique for these purposes. In addition, it has the advantage of allowing continuous transient display after each pulse and the size of the allocated memory buffer is independent of the number of averaged transients. The continuous time averaging mode is similar to the running average formed by a low-pass filter. In this mode, the result of the *last* n_t transients is available at any time for display and for other data processing. Unfortunately, it is not convenient to apply the low-pass filter directly to the multiple time averaging scheme because the data points it averages are consecutive in time. In contrast,

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multiple time averaging processes the whole set of transient data points in parallel, i.e. each data point is averaged with corresponding data points from the other transients which are at the same delay from the start of the transient. In this way, the data points to be averaged are separated by one or more pulse periods and are not consecutive in time. Therefore, we need a method to adapt the low-pass filter function to be applied separately for each data point of the transient.

For a simple asymmetrical first order low-pass filter consisting only of a resistor R and capacitor C , the voltage increment v_o is [251]

$$dv_o/dt = (v_{in} - v_o)/T_c, \quad (3.7)$$

where $T_c = RC$ is the filter time constant. Let us consider v_{in} digitized at short sample intervals δt . Then in discrete form, (3.7) becomes

$$\Delta v_o/\delta t = (v_{in} - v_o)/n_t \delta t, \quad (3.8)$$

where $n_t \delta t$ is the digital time constant corresponding to the analog time constant RC . Therefore, in order to implement a low-pass filter function on each data point of the transient, we have to replace the simple summing and dividing algorithm with

$$v_o \leftarrow v_o + (v_{in} - v_o)/n_t, \quad (3.9)$$

which means, that the value v_o of the data point stored in the computer memory buffer is updated after each new transient with a fraction of its difference from the corresponding data point v_{in} from the new transient.

If the starting value stored in the buffer is zero, then in the beginning of the averag-

ing process the difference is large, and the value in the buffer quickly grows as a new value is added to it after each new transient. As the value stored in the buffer approaches that of the new transient, the growth rate decreases and eventually when the stored value is nearly equal to that of the new transient, the growth terminates. After this, the value in the buffer becomes largely stable and it reflects only changes in the incoming transient which are sustained long enough to be comparable to the digital time constant. This evolution of the transient stored in the computer memory buffer is continuously monitored on the computer screen where each data point looks like it was produced by a separate “virtual” boxcar channel. This is not a surprise, since a real boxcar channel performs exactly the same averaging operation. Of course, our “virtual” boxcar channel differs from the real one. Each “virtual channel” has a fixed time delay and aperture. Fortunately, the pseudo-logarithmically averaged interval length, or the “virtual aperture”, is conveniently self-adjusted depending on the time delay, new “channels” can be easily created, and selecting the averaging time constant $n_t \delta t$ can be fully automated and varied throughout the experiment. Since δt remains constant, only n_t is varied. For convenience, in our system n_t is represented as 2^k and the actual change of the digital time constant is made by selecting k . Since the SNR increases with the square root of the number of averaged transients, it is expected that the SNR will depend linearly on k .

3.4.2 Demonstration

The results of the combined action of both techniques (pseudo-logarithmic and continuous time averaging with variation of k) are shown in Fig. 3.6 and Fig. 3.7. A high time resolution in the beginning of the transient is seen in the inset in Fig. 3.6, and a very good SNR is demonstrated in the inset in Fig. 3.7. The trace with $k=2$ seems almost identical to that with $k=3$ but in fact it contains more noise at low frequencies comparable to the inverse of the pulse period. Note the difference in the second half of the transient. Also, the trace with $k=4$ in Fig. 3.7, compared to the trace with $k=3$ in Fig. 3.6, appears more noisy because the scale of the vertical axes are different. The noise fluctuations in the inset in

Figure 3.7 Combined pseudo-logarithmic and continuous time averaging with different time constants 2^k . The inset shows very good SNR at the end of the transient with $k=10$. Input signal is seen in Fig. 3.5.

Fig. 3.7 can be estimated to be in the range of 10 to 30 $\mu\text{V}_{\text{p-p}}$. Compared with the noise magnitude as seen in Fig. 3.5 a), which is about 10 $\text{mV}_{\text{p-p}}$, the SNR improvement is substantial.

The 12-bit resolution of the ADC (or that of the pseudo-logarithmic circuit) is always much better than the vertical resolution of the computer screen; therefore, quantization errors are not visible. In addition, the 12-bit resolution can be effectively boosted by the averaging process to 16-bit resolution, since the computer operates with 16-bit “words” [251,54].

3.4.3 Implementation

The continuous time averaging routine [266] is activated by a hardware interrupt immediately after the transfer of the last pseudo-logarithmically averaged data point of each transient. For each data point of the received transient, the sub-program shifts left 4 bits, which is equivalent to multiplying by 16. Next, it subtracts the corresponding 16-bit value, stored in the reference memory buffer, then shifts right k bits and finally adds the result to the old buffer value to be stored as a new value. This is exactly the low-pass filter algorithm implied in (3.9). Because the averaging is performed over 16-bit digits, the digital time constant can be as large as $2^{15}-1$ or 32,767 which means the maximum increment or decrement to the 16-bit value stored in the buffer is just one bit. However, in practice this is a very inconvenient choice. Consider, for example, a relatively fast transient recorded during a 20-ms-long emission pulse period. There will be just 50 averaging steps per second, and to change the stored value e times will require $32,767s/50$ or roughly 11 minutes. To reach the new value within 1% error, one has to wait almost one hour. Besides, a 20-ms-long emission pulse period does not allow the pseudo-logarithmic averaging technique to be used efficiently.

3.5 APPLICATIONS

3.5.1 Long Transients

The averaging techniques suggested above are not limited only to the DLTS measurements. The main goals achieved by these techniques are substantial SNR improvement and the efficient reduction of the number of data points. In DLTS, these techniques should be considered as pre-processing steps followed by the actual transient parameter analysis, which can use all digital processing methods listed earlier [54,167,168,93,178, 249,81,235, 115,94,203]. Furthermore, because of the reduced number of data points and increased SNR, it can be expected that these techniques will give better results.

Alternatively, as demonstrated in [54], the weight functions well known in the analog methods, such as boxcar, lock-in amplifier, and exponential correlator, can also be used for the transient analysis. When signal-to-noise ratio is not of concern, the boxcar function is particularly attractive since it gives higher resolution of the peaks. In our system, we rely mostly on the use of the boxcar function with time delays $t_2=2t_1$ by simply subtracting two selected data points with the same index m but from different groups n and $n+1$. The corresponding DLTS scan is displayed in an inset on the computer screen during the thermal scan, overlapping the transient display. The time delays can be varied and the resulting DLTS scans can be seen in real time. Thus both the transient signal and the DLTS scan are updated on the computer monitor after each pulse, similar to what it would be if displayed on an oscilloscope screen. Since the data points for the Arrhenius plots can be obtained during the experiment, the analysis of a given trap can start as soon as the scan of the temperature interval corresponding to the measurable trap time constants is completed.

Fig. 3.8 shows several transients recorded for each degree of temperature change. The magnitudes of the traces were adjusted to fit in the same chart and are not to scale. This adjustment was made in order to demonstrate the benefits of the very high SNR which allows for making obvious the observed changes in the time constant. These results suggest the option of using isothermal analysis DLTS [176,255] which can minimize the effects of thermal dependencies of the capture cross-section and transient magnitude. For this purpose, we need to determine the emission rate without relying on its temperature dependence, for example, by displaying the transient on a logarithmic scale.

In Fig. 3.9 are shown several transients at the same temperature of 47 K, but with different settings of the reference capacitor and the corresponding different reverse steady-state bias voltage across the sample. For comparison, we also recorded a true exponential transient with the magnitude and the time constant adjusted to be close to the real DLTS signal. This true exponential transient was obtained by differentiating a square wave with

Figure 3.8 Temperature variation of the transient time constant as observed during measurements. The curves demonstrate the need for better temperature resolution at low temperatures. Magnitude is not to scale. The temperature was maintained with accuracy better than ± 0.1 K.

an appropriate RC filter. The slope of the traces gives time constants decreasing from 200 ms to 158 ms. The decreased transient time constants, corresponding to low values of the reference capacitor or higher reverse bias demonstrate the effect of field-enhanced emission [39]. It is important to note here that the change in the slope, and the corresponding change in the transient time constant, can be easily monitored at a fixed temperature. This allows for appropriate adjustment of the measurement setup during the experiment. For example, by adjusting the voltage and monitoring the slope of the trace, we can avoid the conditions of field-enhanced emission, and at the same time, obtain a large signal which improves the sensitivity of the measurement.

Figure 3.9 Time constant variation at fixed temperature of 47 K and variable reverse bias 0 to 8 V. The time constants calculated from the slope of the trace vary from 200 ms at zero bias to 158 ms at 4 V. Note the departure from the exponential behavior at 8 V bias during the first 50 ms. For comparison is shown a transient obtained by differentiating a square wave with an RC high-pass filter is also shown.

3.5.2 DLTS Spectra

In the measurements in Fig. 3.6 through Fig. 3.9, the pseudo-logarithmic settings were $N=11$ and $M=16$, the temperature variation was limited between 40 and 50 K, and all transients were associated with just one trap. Indeed, with less than two transient recordings per second and the digital time constant set to 2^9 , about 600 s were needed to obtain good averaging results. Clearly, these settings are not very convenient for a full-range ther-

Figure 3.10 Series of six boxcar DLTS spectra with channel delay ratio $t_2=2t_1$ obtained from one thermal scan. The change in the background level seen at 100 K is for $\tau=1$ ms and $\tau=2$ ms. The change in the magnitude for longer time constants is probably due to temperature variation of the capture cross section.

mal scan, and this setup is better suited for isothermal measurements when a significant noise reduction is essential. When the signal level is high compared to the noise, we set the digital time constant to 2^4 through 2^6 , and then we can store transients up to 1.3 s long for full range of thermal scan. For scanning temperature measurements of noisy transients, we use a setup of $N=8$ and $M=10$ which is enough to record a 50 ms long transients with just 90 points. With about 20 continuous time averages per second, this setup allows us to use digital time constants up to 2^{10} , depending on the temperature scanning rate. For example, if the setup is 2^{10} , then to change the values of the stored transient e times takes less than a minute. Recording the transient at each degree temperature, and with temperature scanning

Figure 3.11 Arrhenius plots obtained from the scan data file used in Fig. 3.10. The energy level positions of the hole traps are in eV above the valence band as indicated. Note the good linearity of the data points.

rate of 0.8 K/minute or less, there is still enough time for averaging, since the time constant of the transient varies far less than e times for each degree of temperature change. This is especially true at temperatures above 100 K where the DLTS signal varies slowly with the temperature.

Using this setup and the simple boxcar technique described above, a series of six DLTS spectra were obtained (Fig. 3.10). There are five well defined peaks present. The shape variation of the large peak at the highest temperature suggests the existence of a sixth peak which is dominated by the large peak. This peak appears more on the curves corresponding to a short time constant setup, and it is a rather strange result because it is well known that the DLTS peak resolution improves for setups of long time constant windows

[54]. However, further analysis shows that this false peak can be associated with the signal overloading, which affects the first half of the stored transient more than the second half.

In Fig. 3.11 are shown the Arrhenius plots obtained using the same data file. As outlined in [12], obtaining the energy level positions and capture cross sections is only the first step toward impurity or defect identification. We limit the scope of this chapter to demonstration of the averaging techniques. The trace in Fig. 3.9 with lowest influence of the field-enhanced emission is fitted well by an exponentially decaying signal with a time constant about 200 ms. In the rightmost Arrhenius plot in Fig. 3.11 for the trap around 50 K, this time constant corresponds to 47.6 K. This again supports the need to record more than one transient for each degree temperature at low temperatures.

Figure 3.12 Series of transients at the peak temperatures for setup $t_1 = 10.3$ ms and $t_2 = 20.4$ ms of the traps in Fig. 3.9 (same data file). Details of the first 2 ms are shown in the inset. Note the overloading at 251 K.

Figure 3.13 The data of Fig. 3.12 plotted on a semilogarithmic scale to display details at the beginning of the transient. The signal before 0.4 ms is distorted because of the instrument recovery after the filling pulse. The dots in the trace at 53 K show the data points evenly spaced on a logarithmic scale. For comparison is shown a CC-DLTS trace obtained from neutron irradiated junction field effect transistors and reduced 25 times in magnitude.

Using setup of $t_1=10.3$ ms and $t_2=20.4$ ms for the rate window, we have found the peak temperatures of the traps appearing in Fig. 3.10. The recorded transients at these temperatures are shown in Fig. 3.12. Signal overloading of the transient recorded at 251 K is seen at the beginning of the trace for delay times less than 5 ms. This is the reason for the false peak appearance on the low-temperature side of the large peak in Fig. 3.11. Therefore, the observation of the whole transient can easily prevent the incorrect interpretation of the shape variation mentioned above. In the inset of Fig. 3.11 are shown details of the same transients during the first 2 ms. This can further improve the rejection of incorrect data for

transient analysis. One simple way to check the transients distortions at the beginning of the transient that are difficult to see is to display the transient on a logarithmic time scale.

In Fig. 3.13 is shown the same series of transients as in Fig. 3.12, but on a logarithmic time scale. Here one considers the data above 0.4 ms since below this limit the recorded data points reflect the capacitance meter recovery process. The switching time of the feedback circuit is below one microsecond and it does not introduce any significant delay. Another possible source of relatively slow recovery time is high series resistance of the sample. From the point of view of demonstrating the averaging techniques, it is interesting to note the smooth shape of the curves during the instrument recovery. This is possible using only very high time-resolution with a good SNR in the beginning of the transient capture. One of the curves in Fig. 3.13 (curve at 53 K) is presented as a set of data points in order to demonstrate their even spacing on a logarithmic time scale. For comparison, another CC-DLTS trace recorded with the same setup is also shown. The measured sample was a junction field-effect transistor subjected to neutron irradiation. This trace proves that the feedback and the biasing circuit are not the source for the distortion in the remaining traces.

3.6 CONCLUSIONS

In this chapter, a new approach to the digital signal processing of DLTS signals by separating the noise and data reduction from the transient analysis was introduced. The combined action of two complementary digital averaging techniques to improve the DLTS digital signal processing was demonstrated. Pseudo-logarithmic time averaging is efficient in reducing the number of processed data points and improving the SNR for high frequency noise components and for the transient tail. Continuous time averaging is well suited for improving overall SNR, for continuous data display and processing, and it is more efficient in using the computer resources.

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The described combination of hardware and software tools for implementation of these techniques supplies continuously fresh data and does not require any synchronization with the main computer program. The proposed techniques allow one to combine the powerful transient analysis of the digital DLTS methods with the sensitivity and the convenience of the analog methods. Furthermore, the developed averaging techniques can be easily adapted to data processing in many other experiments, where the sampling is performed at a fixed rate, but the results can be adequately presented on a logarithmic scale.

CHAPTER 4

FEEDBACK CIRCUITS AND EXPERIMENTAL SETUP FOR CC-DLTS AND CR-DLTS

4.1 INTRODUCTION

Since the introduction of DLTS by Lang [138] a large variety of modifications and improvements have been reported. When a capacitance meter is used, there are two possible modes of operation. In Constant-Voltage mode, one can measure the Capacitance Transient (CVCT). The second way is to keep the Capacitance Constant by using a feedback circuit [180,68,100,160,146,52,120,204,122,123] and to measure the Voltage Transient (CCVT). Combining DLTS and CCVT modes has many advantages. As Johnson [99] has shown, because the capacitance is constant, the depletion layer width also remains constant and therefore the change of the net charge trapped in interface states is directly proportional to the measured voltage transient for any interface trap density. Furthermore, the proportionality factor does not depend on the temperature, doping concentration or doping profile. With double correlation technique, CCVT can be used for both deep imperfection profiles measurements [143] and energy-resolved interface trap measurements [99].

In the classical setup, shown in Fig. 4.1, the capacitance of the DUT is forced to be equal to that of the reference capacitor connected at the time. This is done by using a large-gain compensation amplifier OA in the feedback loop to adjust the bias voltage ΔV across the sample. In practice, for this purpose an integrator with a sufficiently long time constant $\tau = R_1 C_1$ is used to prevent any oscillation in the system, by reducing the total gain in the feedback loop for high frequencies. The cut-off frequency of the integrator is set depending on the properties of the sample at the quiescent point. However the reduced speed of the feedback amplifier causes the voltage transitions between the filling and emission pulses to be integrated, thus distorting the correct signal. The small voltage transient which compensates for the change in the trap occupancy with charge, is outweighed by a large transient

Figure 4.1. Classical setup for constant-capacitance measurements. The feedback loop contains: DUT, capacitance meter, and a high-gain compensation amplifier OA with cut-off gain for high frequencies set by $R_1 C_1$. Signal P is alternating the connection between the reference capacitor for the filling pulse C_f and that for the emission pulse C_e . Shown is also the voltage applied to the DUT containing fast (before moment t) and slow transients.

caused by the integration of the voltage step. In Fig. 4.1 this occurs mostly before the moment t . The distortion is significant for low-density impurities and for measurements with short delay times (before t in Fig. 4.1). Taking into account that most often the voltage step is in the range of hundreds of millivolts or even several volts, while the voltage transient caused by charge emission from the traps is usually below one millivolt, the distortion is a serious problem significantly reducing the useful part of the recorded transient. The large transient is difficult to be accounted since the effective gain dC/dV of the DUT is generally unknown and temperature dependent.

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A very good solution to this problem was proposed in Ref. [204]. In addition to the integrator in [52], an additional local feedback loop, which the authors call a “memory circuit”, was introduced. Its purpose is to store the bias applied on the sample at the end of each pulse and to apply this bias as a baseline at the beginning of the next cycle. Thus the slow integrator needs to follow only the transient caused by the traps and the summing circuit is used to combine the total bias voltage. Unfortunately, the sensitivity reported in [204] (about 1/500 of the dopant density) is too low for measurement of interface state densities at the Si/SiO₂ interface. Following the basic idea proposed in [204], a new “memory circuit” has been created with some improvements. The sensitivity has been increased up to 10⁻⁵ of the dopant density, and measurements with delay times as short as 50/100 μ s are still possible. Furthermore, the concept of alternating the feedback circuit configuration synchronously with the sequence of filling and emission pulses is the technical basis for the new variation of the DLTS technique which we called constant-resistance DLTS.

4.2 FEEDBACK CIRCUIT AND DETAILS ON THE SETUP FOR CC-DLTS

The feedback circuit is shown in Fig. 4.2 and it is similar to the circuit in Ref. [204]. It consists of an integrator OA, a summing amplifier Σ , and four sample and hold amplifiers S&H-1 through S&H-4. Using these sample and hold amplifiers, two parallel analog memories are built, each one providing the corresponding baseline voltage for filling or emitting pulses at the input of the summing amplifier. We call them “emission pulses memory” (S&H-1 and S&H-3 in Fig. 4.2) and “filling pulses memory” (S&H-2 and S&H-4 in Fig. 4.2). Only the noise introduced by the “emission pulses memory” is important for DLTS applications. In order to reduce this noise, two RC low-pass filters R_2C_2 and R_3C_3 are applied in the “emission pulse memory”. The time constants of the integrator R_1C_1 and the low-pass filters are adjusted with respect to the boxcar averager delay times. Further noise reduction is achieved by using commercially available sample and hold amplifiers. They are used in unity gain mode and are connected with large storage capacitors C_4 and

SWITCHING CONTROL

S_1 is closed for 50 μs at the beginning of each pulse. S_2 is closed during an emission pulse, S_3 is closed when S_2 is open. S&H-1 and S&H-4 are sampling just before the filling pulse for 10 μs . S&H-2 and S&H-3 are sampling just before the emission pulse for 10 μs . S_4 is connected to the output of the summing circuit during the emission pulse and to external bias during the filling pulse.

Figure 4.2 Improved feedback circuit - details. Shaded area denotes the “filling pulse memory” which can be omitted when the overloading during the filling pulse can be ignored.

C_5 ($\sim 2 \mu\text{F}$ high quality type, for example, polystyrene). These capacitors are connected via $\sim 1 \text{ k}\Omega$ resistors (not shown in Fig. 4.2) to further increase the acquisition time [261]. As a result, the acquisition time rises to several hundred milliseconds or more, and it can be adjusted by varying the resistance in series to the storage capacitors C_4 and C_5 . In the hold

mode, because the input current of the reading amplifier in the sample and hold circuits is very low, the voltage drop across these resistors can be neglected. The rise of the acquisition time does not affect the system performance, but the noise reduction for low-frequencies is significant. An additional benefit is the reduced distortion when large time constant windows are used. In Ref. [204] the distortion is reported to be 1 mV per second, while in our circuit it is less than 7 μ V/sec and can be neglected in most cases. With this control of the acquisition time, an ordinary S&H circuit behaves much like a boxcar channel. Alternatively, a boxcar channel could be used to provide the base line for the summing amplifier [238].

As it was explained in the previous section, the purpose of the feedback circuit is to bias the DUT in such a way, that its capacitance is equal to the corresponding emission reference capacitance C_e . A miniature electromechanical relay or a fast, low-capacitance diode is used for alternating C_e and C_f at the reference terminals. Another solution is to replace these reference capacitors with a varactor diode, biased separately from the DUT. The varactor diode replaces both capacitors, and its capacitance is alternated simply by applying voltage pulses to the external bias input of the capacitance meter or to an external biasing circuit [262,263]. The varactor diode is easy to switch and adjust, but it is neither an ideal switch nor a high quality capacitor. As an alternative, the reference capacitors can be selected to be high quality variable air-capacitors, but the switching device is slow (Reed-relay or mercury relay), or non-ideal, and operates over a limited voltage range (a diode or a analog semiconductor switch). Additional complications arise when the variation of the reference capacitor used for defect profiling is automated, since then a bank of reference capacitors combined frequently by a slow relay-matrix is used. The problem is that the relays in this matrix have their own parasitic capacitances. Inevitably, some compromises are needed and the choice is made on a case by case basis.

4.3 EXPERIMENTAL SETUP FOR CR-DLTS

In the setup for CR-DLTS shown in Fig. 4.3, the sample transistor is connected as a voltage-controlled resistor between the test terminals of a Boonton 7200 capacitance meter. On the differential terminals is connected a reference resistor R_{ref} which has a low conductance at the 1 MHz test signal frequency. In our case, this resistor is about 1 M Ω . The capacitance meter is used as a high-sensitivity amplifier of the difference in the channel conductance of the FET and the conductance of the reference resistor. This difference is detected by a phase-sensitive detector (PSD) and, through the conductance analog output of the capacitance meter provided on the rear panel, then applied to a feedback circuit.

An important property of the circuit is its dynamic configuration in response to the driving pulses. Essentially, the feedback output is connected to the gate of the sample FET by the switch SW only during the emission pulse. During the filling pulse, the feedback

Figure 4.3 a) Block diagram of the setup for CR-DLTS;
 b) connection for back-gate driving available for four-terminal devices;
 c) connection of two devices for simultaneous measurements (expandable to more).

loop is open and at the FET gate a constant bias from an external source is applied. During the emission pulse with the feedback loop closed, a high-gain compensation amplifier OA provides for almost exact matching of the channel conductance of the tested transistor to that of the reference resistor R_{ref} by continuously adjusting the gate voltage V_g . Since the value of R_{ref} is more than $1\text{ M}\Omega$, then the gate voltage can be considered to be at a value close to the pinch-off voltage, so that the transistor remains in the subthreshold region.

The exact value of the reference resistor is not critical and it can be adjusted in a wide range of values. This feature can be used for simultaneous measurements of many transistors. Since the voltage transient appears as a compensation voltage applied on the gate, one may consider that a transistor array comprising several devices with common source and gate is inconvenient to test using this kind of DLTS measurement. In fact, the actual tool for probing the change in the charge occupancy of the traps is the effect of the threshold voltage change on the channel conductance. Therefore, even if many devices have their gates connected together, the compensation voltage applied to these gates will depend only on the channel conductance of the transistor which participates in the feedback. Furthermore, this voltage will compensate only for the trapped charges lost from the gate-controlled part of the channel and not for the charge emitted from the source and drain space charge regions. In this way, CR DLTS is a convenient method for direct investigation of the active volume of the measured device. In Fig. 4.3 c), a possible connection of two transistors in series is suggested, but this connection can easily be expanded to include more devices. This is possible because the source-drain voltage is zero, and the reduction of the gain of the resulting multi-transistor test structure is compensated by the large gain of the capacitance meter and that of the compensation amplifier.

As in the setup for CC-DLTS, it is important that the analog memory provide a stable base line with low drop-out and low noise, since both errors will be added to the DLTS signal. For these reasons, in the actual circuit, which is based on the circuit shown in

Fig. 4.2, we use two commercially available sample and hold (S&H) integrated circuits, one for sampling the gate bias at the end of the emission pulse, and the other for baseline supply. The storage capacitors have large capacity and they are charged through extra resistors, making the memory circuit operate much like a boxcar channel. From this description, it is obvious that the function of the analog memory can be replaced with a boxcar channel sampling just before the end of the emission pulse. As seen in the circuit diagram on Fig. 4.3, the transient part of the gate voltage is separated from the total gate bias, forming a DLTS signal with a zero base line. This allows the signal to be easily amplified and digitized. The baseline voltage, which is close to the pinch-off voltage, is also available at the output of the analog memory circuit and can be recorded as a function of the temperature during the DLTS thermal scan.

This feedback circuit allows for extraction of transients in the microvolts range from the total gate bias, which can be several volts. This property of the feedback is crucial for successful implementation of the new CR-DLTS technique. We further increase the sensitivity of the new system by using advanced digital signal processing techniques for noise reduction and for storage of the transient at each degree of temperature with a limited number of data points [126]. This technique is described in the next chapter.

4.4 ILLUSTRATIONS

In Fig. 4.4 are shown three traces from three different DLTS modes but for the same device (neutron-radiation damaged JFET) and at the same temperature. These traces are very similar for delay times above 800 μs up to 1.3 sec. The CR-DLTS trace shows the recovery of the capacitance meter from its overloading during the filling pulse. Also, CT- and CC-DLTS traces below 100 μs show a slight distortion which is caused by the low-pass filter of the conditioning amplifier. All traces deviate from purely exponentially decaying transients which is readily seen when they are plotted on semi-logarithmic axes. This deviation is most likely caused by carrier trapping in the Debye tail of the space-charge region

Figure 4.4 Transients obtained from capacitance-transient (CT-DLTS), constant-capacitance (CC-DLTS), and constant-resistance (CR-DLTS) methods using the same device at the same temperature. The CR-DLTS trace below 800 μ s shows the recovery of the capacitance meter following its overloading during the filling pulse.

[175].

One problem often encountered both in CC- and CR- mode of operation is the variation of the effective gain of the measured device with temperature: in general, it increases at low temperatures. While this dependence does not need to be considered for quantitative DLTS measurements, it may still adversely influence the results. The problem is that this gain change modifies the total gain of the feedback loop in both methods, and thus may affect the condition for appearance of oscillations in the feed-

Figure 4.5 CR-DLTS transients of a microwave MOSFET which was stressed with hot carriers. Note the fading oscillations at the beginning of the traces at low temperatures. For illustration of the data point density, each point is represented with a dot in the trace taken at 100 K.

back loop (see Fig. 4.5). Setting the integrator's time constant ($R_1 C_1$ in Fig. 4.2) to a large value ensures that oscillations are avoided, but it simultaneously distorts the data at the beginning of the recorded transient. Therefore, a compromise is often made to adjust this time constant to a value which is just large enough to prevent the oscillations. Unfortunately, because of the variation of the effective gain of the device under test, the feedback circuit which seems stable at some temperature may start to oscillate at lower temperatures, causing complete data loss below this critical temperature. Note that in Fig. 4.5, the fading oscillations at the beginning of the traces increase at low temperatures. Obviously, the oscillations were nearly avoided leaving only negligible distortion, but the setup of the integrator time constant was too close to the critical value.

Figure 4.6 CR-DLTS spectra obtained from a virgin microwave transistor using the new feedback circuit. This is a demonstration of the good sensitivity of the measurement; the magnitude of the signal is just a few tens of microvolts.

In Fig. 4.6 is demonstrated the sensitivity obtained using the new feedback circuit. It allows for recording of voltage transients with a magnitude below 0.1 mV. Because the usual transconductance of the transistors in CR-DLTS mode contributes more to the total gain of the feedback loop than the effective gain of most capacitance structures in CC-DLTS mode, constant-resistance measurements are in general more sensitive. This allows us to obtain specific “features” of the spectrum which helps in determining the capture cross section using the Arrhenius plot technique. Then, as described in Ref. [100], it is possible to obtain the interface trap density shown in Fig. 4.7. For the calculation of the trap density, the capture cross section was assumed independent of temperature and energy in the range of a few kT [100]. This is an approximation, but since the variation of the capture

Figure 4.7 Interface trap density obtained from three different spectra on the same device. Since the energy-resolution increases at low temperature, we see a better coincidence of the curves. Repeating feature in the curves result from variations of the interface trap density.

cross section gives only a minor shift in the obtained interface-trap density spectra on the energy scale, in many cases this result is acceptable. For example, in Fig. 4.8 an increased interface trap density of a transistor located on the same die is demonstrated following hot-electron stressing for 100 hours and at maximum substrate current. As can be seen, the trap concentration increases toward the band edge in agreement with commonly accepted U-shape distribution found using other methods.

When the traps for minority charge carriers are of interest, in this case the traps for electrons, the filling pulse must drive the surface beneath the gate into strong inversion in order these traps to be populated. In Fig. 4.9, the interface trap density for electrons of the same microwave transistor as in Fig. 4.8 is shown after hot-electron stressing. The filling pulse was set at 2V which is enough to obtain strong inversion at all temperatures of

Figure 4.8 Interface-trap density for holes of a microwave transistor on the same die as the transistor measured in Fig. 4.7, after hot-electron stressing. The capture cross section was obtained for three temperatures using the Arrhenius plot technique and then was interpolated as shown in the figure.

Figure 4.9 Interface-trap density for electrons of the microwave transistor in Fig. 4.8, after hot-electron stressing. Note the difference with Fig. 4.8.

the DLTS scan.

Chapter 4: Feedback Circuits and Experimental Setup for CC-DLTS and CR-DLTS

One important remark has to be made about the difference between the measurement of traps for majority and for minority carriers. When measuring majority carrier traps, the space-charge region collapses during the filling pulse and the majority carriers flow into it and accumulate at the interface. The capture rate is high and both interface and bulk traps are filled. During the subsequent emission pulse, the traps will emit their charge to join the majority carriers into the substrate and both interface and bulk traps will be detected.

When minority carriers are injected from the source and drain during the filling pulse, the SCR remains essentially intact, since the inversion layer at the interface screens the electric field from penetration into the substrate. Therefore, traps for minority carriers will be charged only at the interface and during the emission pulse only these traps will respond by emitting their charge, while bulk traps for minority carriers located in the SCR will not be detected. If these traps are of interest, the strong inversion pulse applied at the gate during the filling pulse has to be combined with injection of minority carriers from the source and drain into the substrate by forward biasing the corresponding n^+ -p junctions. Then the bulk traps for minority carriers in the substrate can be populated and measured. While charges emitted from the traps for minority carriers in the SCR, which can contribute to the threshold voltage will be compensated, there will be no such compensation for the traps in the remaining areas of the source and drain p-n junctions. Then the variation of the volume of SCR will cause the traps for majority carriers also to be charged and detected which may complicate the interpretation of the measurement results. This is the problem that was encountered before in the measurement of traps for minority carriers using diode structure and conventional capacitance-transient DLTS.

4.5 CONCLUSIONS

In this chapter, new feedback circuits for CC-DLTS and CR-DLTS have been

Chapter 4: Feedback Circuits and Experimental Setup for CC-DLTS and CR-DLTS

presented. It was demonstrated that with the aid of these circuits, it is possible to record voltage transients without compromising the speed or the sensitivity of the measurement. Comments on technical difficulties when voltage transients are measured were presented. The feedback circuit operation was illustrated with measurements of the interface-trap density in MOSFETs and transient traces of a neutron-radiation damaged JFET.

CHAPTER 5

CONSTANT-RESISTANCE DLTS IN ENHANCEMENT MODE MOSFETS

5.1 INTRODUCTION

During the last two decades, deep-level transient spectroscopy (DLTS) [138] has proven to be among the most sensitive and accurate techniques applied for analyzing deep levels in semiconductors. The standard capacitance DLTS setup [140,161,111] uses a p-n or Schottky diodes as test structures and the emission of trapped charge from the deep levels in the forbidden gap is monitored by measuring the corresponding change in the depletion capacitance of the diode. A very high signal-to-noise ratio (SNR) can be achieved by averaging the measurement over many pulses, as this represents an application of the well known phase-sensitive detection (PSD) technique used for signal recovery from noise [251]. The significant improvement in SNR offered by the PSD technique made DLTS more successful than the previously used thermally stimulated capacitance method. In the standard capacitance DLTS instrumentation, there is already one level of PSD employed inside the capacitance meter. However, it has a substantially lower time constant which is designed to filter only capacitance changes which are much slower than the frequency of the test signal, usually set at 1 MHz.

For practical reasons, sensitive measurements are done by using relatively large area structures. Considering the best commercially available capacitance meters which are fast enough to respond to capacitance changes below the 1 millisecond range, it is possible to resolve capacitance variations in the range of ~ 0.1 fF with the aid of sensitive DLTS processing instrumentation. Therefore, for detection of trap concentrations in the range of 10^{10} cm^{-3} in test structures with background doping of 10^{15} cm^{-3} , the total depletion capacitance of the structure should be ~ 10 pF. In practice, this can be usually obtained using relatively large area test structures.

The various technologies for fabricating large area diodes are rarely complicated, and often, this has been considered rather as an advantage of the DLTS method. Nevertheless, the method was adapted for a number of other test devices that are available during electronic device fabrication or devices whose properties are of practical interest. Among these, the field-effect transistor (FET) has attracted the most attention, since the MOSFETs are the workhorse used in the integrated circuits.

5.2 OVERVIEW OF THE DLTS TECHNIQUES APPLIED FOR FETS

When relatively large FETs are available, the standard capacitance DLTS technique can be easily modified by reverse biasing of source and drain regions, and measuring the gate-substrate MOS structure [247]. Furthermore, unlike the simple MOS structure, the existence of the source and drain in a MOSFET, being large reservoirs of minority current carriers, allows measurements of minority carrier traps [245,246] although the data interpretation can be complicated by simultaneous trapping and emission of majority carriers [248].

Further modifications of the DLTS technique for measurement of FETs are needed because of the small size of the devices, resulting in a small total gate-substrate capacitance. Indeed, with the gate-substrate capacitance in depletion being only few or even less than one fF, measurements of capacitance transient due to charge emission from the traps located beneath the gate becomes practically impossible. More complications arise when the FET is fabricated on insulating or semi-insulating substrate, such as silicon-on-sapphire or FET on GaAs or other compound semiconductor material substrate. Then, the high series resistance of the depleted semiconductor material in the channel requires correction factors to be added to the measurement [22] before analyses are made. Besides, for thin film transistors, the thin silicon epilayer limits the change of the depletion region width and the corresponding capacitance change. Combined with the large series resistance in the depleted channel, this results a large free-carrier transient which complicates the

analysis of a much smaller transient due to the trapped carriers.

To avoid the above difficulties, the conductance DLTS [32] was proposed for measurements of MOSFETs. In this method, the small-signal ac channel conductance is used to monitor the emission transient of the trapped carriers, while the back-gate bias pulses are used to control the trap filling and emission. For trap concentration profiling, the back-gate bias controls the depletion width and bias pulses on the gate are used for controlling the population of trapped carriers. In Ref. [32], the ac channel conductance was measured at zero dc bias of drain to source using an HP 4271B LCR meter, which employs the PSD principle as mentioned above and can detect 0.01% conductance changes. However, for calculation of the trap concentration, the surface free carrier mobility was assumed constant over the entire measured temperature range. In addition, knowledge the flat-band voltage, doping concentration and oxide capacitance was required. Later, conductance DLTS was combined with C-V measurements to calibrate the theoretical characterization model for investigation of ion-implanted GaAs FETs [67]. The model was needed to eliminate common assumptions in other simpler characterization techniques, and with this more rigorous treatment, free-carrier, shallow-level donor, trap and mobility profiles were obtained.

Another modification of the DLTS technique, convenient for FET investigation is based on observation of the drain current transient caused by the effective change in the threshold voltage due to trap carrier emission [85]. Instead of measuring the small-signal conductance as in Refs. [32,67], a small drain-source bias was applied and the resulting current transient ΔI_d was measured, while keeping the gate bias V_g constant. This method benefits from using the gain of the measured transistor, requires simpler instrumentation, and can potentially reach lower time constants, as compared to the small-signal ac conductance DLTS. However, the sensitivity can be lower because of the elimination of PSD noise reduction, and for trap concentration measurements, the FET transconductance under the

same DLTS conditions must be monitored. In Ref. [85], this method was also called a conductance DLTS, which may create a confusion with the small-signal method described above. Essentially the same drain current transient technique combined with surface mobility (and therefore, transconductance) measurements was used later [77,154,155], and the method was correctly referred as a current DLTS.

In this chapter, we suggest a new DLTS variation, which we call a constant-resistance (CR-)DLTS. The preference over constant-conductance name, which is also correct, was given in order to distinguish it from another popular abbreviation, namely CC-DLTS, which stands usually for the constant-capacitance technique [102]. This new technique is similar to the conductance DLTS [32], but instead measuring the small-signal ac conductance directly, the result is applied as an input signal to an electronic feedback circuit. Some idea for this setup was found in Ref. [38], but there it was not used for DLTS measurements. The feedback circuit serves to provide the voltage needed to compensate for the charge losses from the traps during the emission pulse. Thus, additional measurement of the surface mobility or transconductance is avoided, and the benefit of using PSD noise reduction technique is combined with simple and straightforward analysis. The new technique is also similar to the constant capacitance DLTS in the way it compensates for the trapped carriers emission by adjusting the applied bias.

5.3 THEORETICAL BACKGROUND

Here we consider the case of donor-like level in a n-channel MOSFET. A similar formalism can be derived for acceptor-like levels in p-channel transistor with appropriate changes to the notation. In general, with a non-zero source-substrate bias V_{BS} , the threshold voltage V_T in the linear region is given as [45,223,234,253,254]

$$V_T = V_{FB} + 2\psi_B - Q_B/C_{ox} \quad (5.1)$$

where V_{FB} is the flat-band voltage, ψ_B is the Fermi potential in the substrate, and Q_B/C_{ox} is the gate voltage required to compensate for the charge of the ionized acceptor atoms in the space charge region Q_B given by

$$Q_B = -\sqrt{2\epsilon_s q N_A (2\psi_B + V_{BS})}. \quad (5.2)$$

In the above expressions, ϵ_s is semiconductor permittivity, q is the electronic charge, N_A is the effective substrate doping concentration and C_{ox} is the oxide capacitance per unit area defined as

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} \quad (5.3)$$

with T_{ox} being the oxide thickness and ϵ_{ox} the gate oxide permittivity. When there are charges trapped in impurities or defects centers in addition to the shallow dopant N_A , their total charge has to be added to the ionized acceptor atoms. If the total donor-like trap concentration is N_{TT} and all the traps are charged, which is the case after accumulation or filling pulse at the moment $t = 0$, the initial threshold voltage $(V_T)_i$ can be written using (5.1) as

$$(V_T)_i = A + B\sqrt{N_A - N_{TT}} \quad (5.4)$$

where A and B are defined as

$$A = V_{FB} + 2\psi_B \quad (5.5)$$

and

$$B = \frac{\sqrt{2\epsilon_s q (2\psi_B + V_{BS})}}{C_{ox}}. \quad (5.6)$$

In (5.5) and (5.6), the Fermi potential is assumed to remain approximately constant, independent of the temperature in the temperature interval around the DLTS peak. The trapped charge $N_T(t)$ vary with time during the emission pulse as

$$N_T(t) = N_{TT} \exp(-t/\tau) \quad (5.7)$$

where τ is the time constant of the traps according to Shockley-Read-Hall statistics [206,78]. After sufficiently a long time, all trapped charge (holes in this case) are emitted to the valence band, $N_t = 0$, and the threshold voltage $(V_T)_f$ with all traps discharged and neutral becomes

$$(V_T)_f = A + B\sqrt{N_A}. \quad (5.8)$$

The total change of the threshold voltage ΔV_T can be obtained by subtracting (5.4) from (5.8) and is given by

$$\Delta V_T = (V_T)_f - (V_T)_i = B(\sqrt{N_A} - \sqrt{N_A - N_{TT}}). \quad (5.9)$$

Since $N_{TT} \ll N_A$, then (5.9) can be reduced to

$$\Delta V_T \approx B \left(\frac{N_{TT}}{2\sqrt{N_A}} \right). \quad (5.10)$$

In our system, this is exactly the voltage change which is compensated by the feedback circuit when the emission pulse is long enough, and this is the magnitude of the recorded voltage transient. Because of the system delay, in practice, only the part of the voltage transient after this delay is measured and recorded. Therefore, it is useful to express the time variation of $\Delta V_T(t)$ using (5.7) and (5.10) as

$$\Delta V_T(t) \approx B \left(\frac{N_T(t)}{2\sqrt{N_A}} \right) = B \left(\frac{N_{TT} \exp(-t/\tau)}{2\sqrt{N_A}} \right). \quad (5.11)$$

Our feedback system provide a separate output, where the total voltage needed to maintain the drain-source small-signal ac conductance equal to some selected reference value G_{ref} can be measured and recorded. If this reference conductance is small enough, as in our case it is $G_{ref} > 1 \mu S$, then this voltage is approximately equal to the threshold voltage. The time variation of the threshold voltage can be found by combining (5.4), (5.8) and (5.11) to give

$$V_T(t) = (V_T)_i + B \left(\frac{N_{TT}}{2\sqrt{N_A}} \right) [1 - \exp(-t/\tau)] \quad (5.12)$$

or

$$V_T(t) \equiv A + (Q_B/C_{ox}) \left[1 - \left(\frac{N_{TT}}{2N_A} \right) \exp(-t/\tau) \right]. \quad (5.13)$$

We should note, that since the feedback circuit provides the threshold voltage and its changes directly, without ever measuring explicitly the drain-source current, then there is no need for the transistor size or surface mobility to be measured, which is a necessary part of the conductance or current DLTS methods. Furthermore, if the trap concentration and interface trap densities are the same, the voltage transient should be *independent* of the MOSFET dimensions. In other words, even deep submicron transistors should provide a DLTS signal which is large enough to obtain good signal-to-noise ratio. This is no surprise, given the fact that the small total amount of trapped charge beneath the gate of the minimum size transistor has to be balanced by a correction voltage applied across a relatively small gate-substrate capacitance.

5.4 EXPERIMENTAL RESULTS

We illustrate the new CR-DLTS technique with some results from measurements of n-channel MOSFETs with 0.8 μm channel length, the minimum dimension available for our test chip design. Here, it should be noted that the sample transistor gain is an effective part of the common feedback loop, and therefore it may be expected to affect the circuit sensitivity. However, to our observation, the large gain of the capacitance meter effectively compensates for the sample transistor's gain, and in practice, the transistor's size affects only the setting of the time constant of the feedback circuit integrator. At low temperatures, where the surface mobility increases, for samples with large W/L ratio, it was often better to reduce the capacitance meter gain, rather than to increase the integrator time constant, because the latter distorts the recorded transient for short delay times.

The CR-DLTS scan of the sample MOSFET presented in Fig. 5.1 shows a peak at ~ 70 K, which can be associated with an energy level at about 0.11 eV above the valence band and capture cross section $\sigma \sim 1 \times 10^{-15} \text{ cm}^2$. This peak arises from a signal with continuous energy distribution due to interface states. At this stage, the associated trap cannot be identified with confidence, but it may be related to (Fe - B) complex [13]. At higher temperatures, it appears that there are two other "peaks", but they cannot be related with confidence to discrete energy levels because they are wider than what is normally obtained. There were no intentional contaminations or damages of our samples, and the measured trap concentrations are very low. This in turn produces a very weak signal below the instrumentation noise level, and this weak signal can be detected only after advanced digital averaging [127]. However, the noise features can be identified easily and are distinguished from the peaks by varying the delay times and observing the changes in the scan. The increased magnitude of the signal at lower temperatures corresponds to the increased interface trap density toward the valence band edge. This result is in agreement with the well-known U-shape energy distribution of the interface traps, but contradicts other DLTS measurements on p-type MOS capacitors [102]. At present, there is no satisfactory explanation

Figure 5.1 CR-DLTS scan of an n-channel MOSFET. The peak at ~ 70 K appears for all possible combinations of t_1 and t_2 settings and from the Arrhenius plot, the corresponding energy level is ~ 0.11 eV above the valence band and the capture cross section is $\sigma \sim 1.2 \times 10^{-15} \text{ cm}^2$.

of this result.

In Fig. 5.2 is shown a CR-DLTS temperature scan of a minimum size MOSFET available from our test design. The device in Fig. 5.2 was selected in order to demonstrate a discrete trap energy level, and it was not on the same test chip as the device described in Fig. 5.1. The parameters of the hole trap causing the peak at ~ 100 K are: energy level at about 0.12 eV above the valence band and capture cross section about $6 \times 10^{-17} \text{ cm}^2$. It is possibly related to Mn impurity atoms [13]. Here we emphasize more on demonstrating the CR-DLTS method, rather than the results.

A similar deep level appears in the CR-DLTS scans shown in Fig. 5.3 at 0.13 eV

Figure 5.2 CR-DLTS scan of a minimum size n-channel MOSFET. The peak below 100 K is related to a discrete deep level at ~ 0.12 eV above the valence band with a capture cross section $\sigma \sim 6 \times 10^{-17} \text{ cm}^2$.

above the valence band and capture cross section $\sigma \sim 1 \times 10^{-15} \text{ cm}^2$. The measured device is a $2 \mu\text{m} \times 0.3 \mu\text{m}$ n-MOSFET which has an entirely different fabrication history from the devices in our test chips. In this figure, the interface trap density decreases toward the valence band edge, which result is in agreement with the previous DLTS measurements of p-MOS capacitors. Here, it is interesting to note, that both scans exhibit very similar features when the shift toward lower temperatures for slower rate window setups are taken into account. This supports the idea that we are measuring the actual variation in the interface trap density with different energy levels inside the bandgap. In Fig. 5.4 are presented results from measurements of the same device as in Fig. 5.3, but with variation of the source-substrate bias. The thermal scan with -1 V substrate bias has a lower magnitude compared to that obtained without substrate bias. The only exception is the peak associated with the hole trap at 0.13 eV above the valence band. At the same time the surrounding

Figure 5.3 Two CR-DLTS scans of an n-channel deep submicron MOSFET. The magnitude is comparable with that of the $0.8\mu\text{m} \times 22\mu\text{m}$ device shown in Fig. 5.1. The peak below 100 K corresponds to a deep level $\sim 0.13\text{ eV}$ above the valence band with $\sigma \sim 1 \times 10^{-15}\text{ cm}^2$.

peaks have significantly reduced magnitudes. Increasing the reverse substrate bias leads to a decreased gate control over the space-charge region near to the interface, and reduced number of interface traps which can participate in the charge capture and emission processes. At the same time, the width of the space charge region beneath the gate increases, and more bulk deep levels can respond to the filling pulse applied to the gate. This can explain the increased magnitude of the peak corresponding to the deep level in the scan with -1 V substrate bias. The differences in Fig. 5.4 between both DLTS scans demonstrate the possibility to distinguish the effect of the surface traps from the bulk traps by performing measurements with variations of the substrate bias.

It is useful to compare the new CR-DLTS method with some other DLTS technique. In our case, the constant capacitance DLTS method is very convenient. It uses almost the

Figure 5.4 Body effect in CR-DLTS. The substrate bias affects the surface and the bulk traps in different ways. The only part of the DLTS scan with -1 V substrate bias which is larger than the scan measured with zero bias is the peak corresponding to a bulk trap. At the same time, the signal related to the surface traps is decreased due to the reduced area of the channel which is still under gate control. This effect is more pronounced for short-channel devices.

same instrumentation, except that the reference structure is a variable air capacitor, the input of the feedback circuit is connected to the capacitance output, and the total bias is applied to the sample through an external bias circuit [262]. In [85] comparison of the proposed new technique to the standard capacitance DLTS was made by using a “fat” transistor, i. e. a transistor with relatively large gate area allowing for capacitance measurements. Since the constant capacitance DLTS signal is also area independent, one might expect that this is an unnecessary requirement in our case. However, the “gain” of the MOS capacitor structure in the feedback loop dC/dV is very low for small area devices, and the SNR is very poor, thus preventing sensitive measurements. For this reason, we compared the two

Figure 5.5 Comparison between CR-DLTS with different substrate bias and CC-DLTS by measuring 400 MOSFETs in parallel. Substrate bias was zero for CR-DLTS (1) and -2 V for CR-DLTS (2). Note the increased noise magnitude of CC-DLTS due to lower gain of the sample in the feedback loop.

DLTS modes by using 400 MOSFETs connected in parallel, each of $W/L = 22 \mu\text{m}/0.8 \mu\text{m}$. CR-DLTS measurements were done in the manner described above. For the CC-DLTS measurements, we used 1 MHz decoupling filter which connects the source and drain to the substrate at all the frequencies except 1 MHz. This filter has reduced the electromagnetic interference which affects the CC-DLTS more than CR-DLTS. In Fig. 5.5 are presented the results from the comparative measurements with variation of the substrate bias.

Comparing the two CR-DLTS scans, we see a substantial increase in the peak value at higher substrate bias, which indicates a bulk trap. A good agreement was found between the results obtained with CR-DLTS and CC-DLTS, despite some discrepancy above 200 K.

Figure 5.6 Arrhenius plots of the peaks in the previous figures. Bold circles refer to the trap in Fig. 5.1, bold triangles refer the trap in Fig. 5.2, and bold squares are for the trap in Fig. 5.3 and Fig. 5.4. The two overlapped leftmost plots correspond to the trap in Fig. 5.5. Data obtained from CR-DLTS (2) is denoted with crosses, and from CC-DLTS is denoted with open circles. The difference in the determined energy level position is about 7 meV and the difference in the capture cross section is $8 \times 10^{-16} \text{ cm}^2$.

We attribute the positive values in the CC-DLTS scan to possible problems with the biasing circuit and different averaging parameter settings of the DLTS processing and recording circuit. Since both measurements are performed using the same device, similar results should be expected. The hole trap is at 0.28 eV above the valence band and its capture cross section is $\sim 8 \times 10^{-16} \text{ cm}^2$. Differences between the parameters determined using CR-DLTS (2) and CC-DLTS are 7 meV and $\sim 2 \times 10^{-16} \text{ cm}^2$, and this difference can be attributed to the possible effect of field-enhanced emission, since the two types of measurements are performed with different reverse biases applied to the substrate.

In Fig. 5.6 are shown the Arrhenius plots of the traps from the previous figures.

Recording the whole transient for each degree change in temperature allows us to obtain large sets of data points for each trap. Note the good linearity and low dispersion of the data points. The traps in the Figs. 5.1 and 5.2 have similar energy levels, but their very different capture cross sections prevent us from attributing them to just one type of defect. A similar situation exists for the trap in the Fig. 5.2 compared to the trap in Figs. 5.3 and 5.4. They have approximately the same capture cross section, but the measured difference of 20 meV in the energy level position is well above the margin of error for our system, which we estimate to be just a few meV. The small difference in the parameters of the trap in Fig. 5.5 can be attributed to the effect of field-enhanced emission and is not necessarily due to inaccurate measurements.

5.5 CONCLUSIONS

In this chapter, we presented a new DLTS technique - constant resistance DLTS - suitable for submicron MOSFETs measurements. It does not require additional measurements of the sample transconductance g_m or the surface mobility μ , is very sensitive, and it can operate at very low channel current levels, thus it is unlikely to degrade the sample FET. Because the DLTS signal is independent of the device area, CR-DLTS allows measurements of minimum size transistors without loss of sensitivity.

CHAPTER 6

CONSTANT-RESISTANCE DLTS IN DEPLETION MODE

MOSFETS

6.1 INTRODUCTION

6.1.1 Charge Coupled Devices and Reading MOSFETs

Charge Coupled Device (CCD) image sensors are used widely in optical astronomical telescopes because of their high sensitivity, linearity, and low noise. CCDs are particularly attractive for space-based astronomy because of their low power consumption and high reliability. During operation in space, these CCD based imagers are subjected to various sources of radiation damage. Among these, proton induced damage is of particular interest to us because in the projected five-year mission of the Lyman Far-UV Spectrographic Explorer (FUSE), the imagers are expected to encounter a large number of energetic protons [82,83,124,125,169-171]. The charge signal induced in the CCD imaging array is converted to a voltage by a low-noise amplifier. The key device in these amplifiers is a buried-channel MOSFET, which has a significant effect on the overall performance and reliability of the CCD imager. Because of this, the radiation induced damage in these transistors is of particular importance to the reliability of the CCD imagers that are to be used in space.

The output MOSFETs are specially designed depletion mode lightly-doped drain (LDD) devices which operate as source followers with floating gates. The charge from the CCD array is dumped onto the gate of the transistor, and it produces a voltage inversely proportional to the capacitance of the floating node. Therefore, for the greatest sensitivity, it is desirable to reduce the capacitance of the gate as much as possible. This can be achieved by minimizing the gate area, and by using the LDD structure which reduces the overlap capacitance between the gate and the source and drain diffu-

sions. Typical CCD charge conversion transistors have channel dimensions $50\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ and the depths of the implanted channels are in the range of several microns. For our devices, using a C-V technique, the implanted channel effective doping concentration is measured to be $1.1 \times 10^{12}\text{ cm}^{-2}$, and this is in a good agreement with the value calculated from technology process modeling programs [110]. The deep channel design reduces the low frequency noise associated with surface and near-interfacial traps, but it makes it practically impossible to apply traditional capacitance transient DLTS [248].

6.1.2 CR-DLTS Method Applied for Measurement of Depletion Mode FETs

In this chapter we demonstrate the benefits of using the new CR-DLTS method for studying depletion mode MOSFETs. Although the DLTS setup used is technically the same as the setup described in Chap. 4, there is a major difference when it is applied for measurements of depletion mode transistors. If we consider enhancement and depletion-mode n-channel transistors, the gate-controlled space charge regions have different types of conductivity - p-type substrate in the enhancement mode transistor, and n-type implanted channel in the depletion mode device. Since DLTS is a majority carrier method, the enhancement device is well suited for investigation of the hole traps, while the depletion mode transistor is better used for measurement of the electron traps. In the case when the doping concentrations of the implanted channel and the substrate are comparable, it is possible to measure the trap distributions on both sides of the implanted channel-substrate p-n junction.

6.2 THEORETICAL BACKGROUND

The buried channel MOSFETs are more complicated for analysis than the corresponding enhancement mode surface channel devices [234]. Here we limit our discussion to an n-type buried channel MOSFET. For simplicity, we neglect the LDD regions and the depletion regions around the n^+ doped source and drain.

Figure 6.1 Part of a CCD n-MOSFET with the implanted channel fully depleted. For simplicity, the space charge region around the n^+ region and the LDD extensions are not shown.

Fig. 6.1 shows part of a buried n-channel MOSFET with the channel fully depleted. The vertical structure can be regarded as a combination of a MOS capacitor and an adjacent p-n junction diode. For front gate operation, the source-substrate (p-n diode) reverse bias voltage V_{SB} is held constant, and therefore the width of the two space charge regions of the channel-substrate p-n junction also remain constant. At the same time, the gate-source (MOS capacitor) bias is pulsed between a channel enhancement voltage (trap filling pulse) and a channel depletion voltage (emission pulse). During the filling pulse, when the gate-source voltage is constant, the gate-controlled part of the implanted channel is saturated with electrons flowing from the source and drain regions, and the electron traps are filled. During the emission pulse, a feedback circuit continuously adjusts the gate-source voltage

in order to maintain very weak conducting channel inside the buried channel. This conducting channel is maintained at the boundary between the gate-controlled and substrate-controlled parts of the channel, that is between the p-n diode and the MOS capacitor in Fig. 6.1, while the rest of the channel is fully depleted. This condition, when the two depleted regions inside the implanted channel meet, is defined as pinch-off, and it is shown in Fig. 6.1. The voltage to achieve channel pinch-off is denoted in Fig. 6.1 with $V_{GB}=V_{GBP}$ where the gate-substrate voltage V_{GB} includes the constant voltage V_{SB} . We use in our DLTS setup a memory feedback circuit (see Chap. 4), originally designed and used for a constant-capacitance DLTS mode of operation [101,102].

In general, V_{GBP} can be found by solving Poisson's equation. Tsividis [234] suggests an expression for V_{GBP} of the form

$$V_{GBP} = V_{SB} + V_P(V_{SB}) \quad (6.1)$$

where V_P is the "pinch-off voltage". For the case when the implanted channel has a substantially higher doping concentration N_I compared to that of the substrate N_{AB} , the pinch-off voltage is given by

$$V_P(V_{SB}) = V_{P0} + \gamma_I(\sqrt{\phi_o + V_{SB}} - \sqrt{\phi_o}) \quad \text{for } N_I \gg N_{AB} \quad (6.2)$$

where

$$V_{P0} = V_{FB} + \phi_o - \frac{q(N_I - N_{AB})y_I}{C_{ox}} \left(1 + \frac{y_I C_{ox}}{2\epsilon_s} \right) + \gamma_I \sqrt{\phi_o}. \quad (6.3)$$

In (6.3), the flat-band voltage $V_{FB} = \Phi_{MS} - Q_o/C_{ox}$ and

$$\gamma_I = \left(1 + \frac{y_I C_{ox}}{\epsilon_s} \right) \gamma \quad (6.4)$$

where γ is the body effect coefficient of an unimplanted device on the same substrate and y_I is the depth of the implanted channel. The remaining symbols have their usual meanings [234].

When there are charges trapped in deep impurities or defect centers, in addition to the shallow dopants ($N_I - N_{AB}$) in the implanted channel, their total charge has to be added to the ionized shallow impurity atoms in (6.3). If the total acceptor-like trap concentration is N_{TT} and all the traps are charged, then ($N_I - N_{AB}$) in (6.3) has to be replaced with ($N_I - N_{AB} - N_{TT}$). The time variation of the trapped charge is

$$N_T(t) = N_{TT} \exp(-t/\tau) \quad (6.5)$$

where τ is the emission time constant of the traps according to the Shockley-Read-Hall statistics. After a sufficiently long time, all the trapped charges will be emitted and then the space charge in the depleted implanted channel will consist only of donors and acceptors. With constant V_{SB} , if the interface trapped charge is neglected and the deep impurity concentration is much lower than the effective doping concentration in the implanted channel, then most of the terms in (6.3) are constant during the emission pulse, and only the third term is changing with time. The total change of V_{PO} will be

$$\Delta V_{PO} = V_{PO}(0) - V_{PO}(\infty) = \frac{qN_{TT}y_I}{C_{ox}} \left(1 + \frac{y_I C_{ox}}{2\epsilon_s} \right). \quad (6.6)$$

This reflects the fact that the volumes of all space charge regions and body coefficients remain constant during the trap emission, which is a good approximation for low trap concentrations. The time variation of V_{PO} using (6.5) will be

$$\Delta V_{PO}(t) = \frac{qN_{TT}(1 - \exp(-t/\tau))y_I}{C_{ox}} \left(1 + \frac{y_I C_{ox}}{2\epsilon_s} \right). \quad (6.7)$$

In our DLTS system, the feedback circuit compensates for the trapped charge loss and this compensation voltage balances the change in the pinch-off voltage $\Delta V_{PO}(t)$. We measure this change directly and without reference to the transistor width-to-length ratio W/L or free carrier mobility μ . The above expressions were derived for the case of $N_I \gg N_{AB}$, but it is possible to obtain corresponding expressions for the more common case with comparable concentrations N_I and N_{AB} , again without prior knowledge of W/L or μ . If the trap concentration is low enough, the volume of the space charge regions will remain essentially constant. This can greatly simplify the calculations and one can obtain expressions similar to (6.6) and (6.7), except that the effective width of the gate controlled part of the implanted channel y_I' should replace the total implanted channel thickness y_I . By adjusting the source-substrate bias we can vary this effective width y_I' and thus we can achieve depth profiling of the traps. Another commonly used DLTS profiling technique, that is selective trap filling, is also available [138,222].

6.3 EXPERIMENTAL RESULTS AND DISCUSSIONS

We have investigated three test chips, each containing a set of 15 buried n-channel MOSFETs. One set was subjected to 5.0×10^8 protons/cm² at 1.0 MeV, and another to 9.7×10^9 protons/cm² at 1.0 MeV. The third set of devices were undamaged. These are the same devices that were studied in [169,170]. Here we present first the CR-DLTS results from the measurement of the 20 μ m x 50 μ m device, since these results are typical. Fig. 6.2 shows CR-DLTS scans of these devices. As expected, the transistor with largest dose of radiation exhibits the largest DLTS signal. In this spectrum, five peaks are observed. In the spectrum of the device with moderate dose of radiation, one can distinguish only four peaks and the magnitude of the signal relates to that of the other damaged device in approximately the same ratio as the proton dose. The CR-DLTS scan of the undamaged device has a much lower magnitude and no peaks can be seen. The slight rise in ΔV_g at low temperatures that is visible in this scan is most likely due to the interface traps at the Si-SiO₂ interface, which can also be detected with this technique [102]. Our DLTS system records the

Figure 6.2 CR-DLTS spectra of two proton irradiated devices compared to the spectrum of an undamaged device. The source-substrate bias was -16 V and the filling pulse was 0.6 V.

transient at each degree of temperature as a set of data points [127]. Fig. 6.3 shows six DLTS spectra obtained from one temperature scan for six selected rate windows. The scans obtained for time constants 1, 2, and 5 ms become negative in the range 100-200 K. Reasons for this behavior could be the non-exponential transients or a high series resistance [249,199]. From the CR-DLTS data file, which was used to generate the spectra in Fig. 6.3, were obtained the data points for the Arrhenius plots shown in Fig. 6.4. Good linearity was obtained except for the data of the partly overlapped peak at 65 K. The electron trap energy levels were found to be 0.098, 0.138, 0.194, 0.256, and 0.392 eV below the conduction band. The corresponding capture cross sections were 4.6×10^{-15} , 6.3×10^{-15} , 1.2×10^{-16} , 8.5×10^{-16} , and $3.4 \times 10^{-15} \text{ cm}^2$. From these parameters, it is difficult to identify with confidence any of the traps with those listed in Ref. [13]. Our later analyses, described in this

Figure 6.3 Six CR-DLTS spectra obtained from one temperature scan of the heavily damaged device at different rate window settings of 1, 2, 5, 10, 20, and 37 ms.

work, have demonstrated that the values obtained for these traps are significantly affected by field-enhanced emission, and to indicate that, we present these values in parentheses.

Fig. 6.5 shows two DLTS spectra obtained with different setting of the source-substrate bias V_{SB} . Reducing V_{SB} causes a larger part of the implanted channel to be under gate control, and therefore, to an increased number of traps that participate in the filling and emission processes. This is reflected in Fig. 6.5 with an increased DLTS signal magnitude ΔV_g . Reducing V_{SB} also shifts the boundary between the substrate- and gate-controlled part of the channel deeper into the channel. In the common case where the traps have a non-uniform spatial distribution, then this can give a different change in the magnitude of ΔV_g for each deep level. In Fig. 6.5, the level denoted with E3 changes very slowly as compared to

Figure 6.4 Arrhenius plots using the CR-DLTS data file of the heavily damaged device which received the dose of 2.7×10^9 protons/cm².

E2, E4, and E5. This could indicate that traps at E3 are concentrated near the surface beneath the gate, so that increasing the depth of the gate controlled part of the channel does not include substantial new amount of the defects identified by E3.

In Fig. 6.6 we present again front-gate CR-DLTS spectra with variation of the source-substrate bias, but measuring another device on the same test chip. The increased relative magnitude, substantial variation of the temperature of the peak, and the shape of E4 can be indication that this peak might result from a combination of some other peaks and not necessarily be attributed to a separate deep level.

The profiling technique introduced with the DLTS method [138] is commonly

Figure 6.5 Transient magnitude dependence on the gate controlled volume of the buried channel. A decreased substrate bias allows a larger part of the channel to be controlled by the gate.

available in most of the DLTS experiments. The idea is to populate selectively the traps in the investigated space charge region by varying the magnitude of the filling pulse [138, 222]. In Fig. 6.7 we present several CR-DLTS scans with variation of the filling pulse magnitude. Since all the voltages are relative to the source, and the pinch-off voltage is about -8 V, increasing the filling pulse magnitude toward -7 V actually decreases the active volume in the channel and the amount of traps which can be populated, resulting in a proportional decrease of the DLTS signal. Furthermore, one can see a slight shift of all the peaks toward higher temperatures (for the same rate window setup), and this is equivalent to increasing the apparent time constant of the traps. In fact, at more negative filling pulse magnitude, only those traps which are close to the p-n diode/MOS capacitor boundary inside the implanted channel (see Fig. 6.1) can be populated.

Figure 6.6 Variations of the CR-DLTS spectra for different substrate biases using another device on the same test chip. Note differences with the device from the Fig. 6.5 and the strong variation of the peak at approximately 160 K.

During the emission pulse, these traps experience a weaker electric field compared to those close to the Si-SiO₂ interface and, the emission time constant of these traps will be less affected by the electric field. Therefore, for reduced field-enhanced emission and correct trap identification, one should use the data obtained with a filling pulse of magnitude close to the threshold voltage. Since the DLTS signal magnitude, and therefore sensitivity, is also reduced, then one has to determine some optimal filling pulse voltage for the transient analysis. This can be done by comparing the data from several scans with different filling pulse magnitudes. Alternatively, one can vary the filling pulse and monitor the time constant of the recorded transient at some fixed peak temperature.

We found that for our samples, setting the filling pulse at -3 V is a good compro-

Figure 6.7 Possibility for trap profiling using variation of the filling pulse magnitude. When the magnitude approaches the threshold voltage (from 0 to -7 V), then the filling pulse becomes more negative, less traps are populated, and the CR-DLTS signal magnitude proportionally decreases.

mise between reasonable sensitivity and lower electric field requirement during the emission pulse. In Fig. 6.8 are shown the Arrhenius plots and the activation energies of the traps. The results for E2, E3, and E5 are very close to these reported in Ref. [222,13,229] and more recent works [186,37,220,221,8]. There is an electron trap at 0.16 eV below the conduction band associated with the oxygen-vacancy complex [229,186,37] and our data for E2 is very close to this value. Others [222,13,220,221,8] have reported for this defect a level of 0.18 eV. More consensus exists for the defects giving levels at 0.23 eV and 0.43 eV [222,13,186,37] which corresponds to our results for E3 and E5. A double charged divacancy is considered to give the level at 0.23 eV and a singly-charged divacancy - at 0.43 eV. It was recently suggested that the level at 0.43 eV could also be a combination of

Figure 6.8 Arrhenius plots obtained from the data recorded with -3 V filling pulse magnitude. The source-substrate bias was -8 V. The capture cross sections obtained from the intercepts for the traps E1 through E5 are 10^{-16} cm^2 , $3 \times 10^{-15} \text{ cm}^2$, $4 \times 10^{-16} \text{ cm}^2$, $3 \times 10^{-16} \text{ cm}^2$, and 10^{-15} cm^2 respectively.

a singly-charged divacancy at 0.41 eV and a phosphorus- vacancy complex at 0.44 eV [186,37].

Unfortunately, most of the experiments in the literature are limited to liquid nitrogen temperatures and defect E1 giving a level at 0.11 eV could not be identified with confidence. The parameters are close to these listed for a Mn impurity [13], but the low relative concentration of this defect prevents reliable identification. The origin of E4 is also not well established. Similar results for a trap at 0.30 eV are reported as a minor level defect after 0.6 MeV ion implantation with Si [221] or 2 MeV electron irradiation [222,8]. However, the peculiar behavior of the peak associated with this trap demonstrated in Fig. 6.6 requires extra precaution in the trap identification. Similar peak

Figure 6.9 Substrate controlled CR-DLTS spectra and source-substrate (S-B) CC-DLTS spectrum. Filling pulse was -4 V for CR-DLTS(1) and -1 V for CR-DLTS (2) with gate bias -20 V and -17 V respectively.

broadening was observed in Ref. [222] and it was suggested that the peak at 0.30 eV may result from overlapping of two closely spaced peaks. In this work, we emphasize the various options for DLTS measurements which the new CR-DLTS technique offers rather than the trap identification. It should also be noted that, unlike the quoted references where the studies are carried out on specially prepared p^+-n and n^+-p samples, we use depletion-mode MOSFETs with dimensions and channel doping designed for other purposes.

By comparing the peak heights with the noise, the magnitude resolution in the spectrum at -7 V in Fig. 6.7 and in the spectrum of less exposed device in Fig. 6.2 can be estimated to be in the range of a few tens of microvolts. With the oxide thickness about 400 Å and y_I' estimated to be in the range of several microns, by using Eqn. (6.6) we estimate the

concentration resolution to be in the range of a few times 10^9 cm^{-3} . This sensitivity is about three orders of magnitude below the effective doping concentration in the channel, and it is about two decades worse than that obtained in our more recent results [128] which is typical for advanced DLTS systems [199]. However, when we take into account the size of the measured device ($50 \text{ } \mu\text{m} \times 20 \text{ } \mu\text{m}$), and consider the absolute number of traps into the active volume of the channel, to the depth of several microns, our estimate for the sensitivity correspond only to a few tens of traps. This high absolute sensitivity is not new in the DLTS [20], and we benefit from the special design of our devices which is aimed to highest possible sensitivity of the gate voltage versus gate charge changes [83].

While addressing the issue about the maximal absolute sensitivity of the DLTS and in particular of the variation presented here, one should remember that single traps were observed by analyzing the so called random telegraph signal (RTS). This high sensitivity was demonstrated for both MOSFETs [117] and JFETs [106]. Our best results are in the range of 20 to 30 detected traps. It may be possible for the sensitivity to be further enhanced by using specially designed devices and longer integration times and thus, only a few traps to be detected as demonstrated before for a scanning DLTS system [20], but still the RTS technique will be more sensitive and simpler. However, one should remember that this technique works well only when a few traps well separated in space and in energy are present, and if possible, it becomes very complex to perform RTS analysis in all other cases.

Because of the effective mechanism to maintain constant volume of the space charge regions employed by the new technique, the upper limits of trap concentrations which can still be measured with confidence can be very high, comparable to the doping concentration in the channel. This suggestion is based on estimates made for CC-DLTS [204], which setup has a similar effect on the space charge volume of the test capacitor. Similarly, the same limits should be valid for the new technique as well, if the variation of

source and gate-drain capacitors is small compared to the gate-channel capacitance.

An attempt was made to operate the CR-DLTS setup in back-gate mode. The gate bias was fixed at large negative values (-17 V and -20 V), and the filling pulse was varied. In Fig. 6.9, we see that a more negative filling pulse (-4 V) reduces the effect of hole trapping and emission and correspondingly, the magnitude of the large negative peak H1. The filling pulse magnitude also has a clear effect on the background level of E3, which we suggest is effect of magnitude variation of an overlapping negative peak denoted as H2. A constant-capacitance (CC-)DLTS scan was obtained from the measurement of a large implanted channel-substrate p-n junction formed by connecting in parallel all available transistors on the chip, and the results are also presented in Fig. 6.9. After scaling, this CC-DLTS scan coincides for the most part with the CR-DLTS (2) scan obtained with less negative filling pulse. The only large deviation is the large peak H1. These results demonstrate the simultaneous participation of electron and hole traps in capture and emission processes.

For CC-DLTS, this situation is identical to measurement of a dual-sided p-n junction, which is difficult to analyze. Although CR-DLTS appears to be similar to CC-DLTS, it has a major advantage. By varying the gate bias, one can control the active volume and total number of electron traps contributing to the DLTS signal. Also, one can vary the magnitude of the filling pulse applied to the substrate and thus control the trap filling on both sides of the junction. When these possibilities are combined with the front-gate operation, there are better opportunities for separation of the contribution of the hole and electron traps in the total DLTS signal. As an illustration, we found the activation energies for both the large and the small negative peaks suggested in Fig. 6.9. Our results for H1 and H2 are presented in Fig. 6.10 and they agree with those obtained for irradiation generated hole traps in p-Si at +0.22 eV and +0.36 eV above the valence band [13,229,37]. According to these references, H2 is associated with single positively charged divacancies, and H1 is

Figure 6.10 Arrhenius plots for the large negative peak and for suggested smaller peak using the same data as used for the CR-DLTS (2) spectra in Fig. 6.9.

considered to be due to carbon-oxygen complexes.

6.4 CONCLUSIONS

In conclusion, we have demonstrated how the new and improved DLTS technique can be applied to study defects in low gate capacitance MOSFETs which were used as charge conversion output transistors in CCD imagers. The technique is sensitive, independent of the transistor size, and does not require measurement of the transconductance or free carrier mobility. This DLTS technique offers extended opportunities to study the trap distribution in the depth of the implanted channel of output transistors in CCD imagers. When the front-gate mode of CR-DLTS operation is combined with the back-gate mode, there are additional opportunities for separating the contribution of electron and hole traps to the total DLTS signal.

CHAPTER 7

CONSTANT-RESISTANCE DLTS

IN JUNCTION FIELD-EFFECT TRANSISTORS

7.1 INTRODUCTION

7.1.1 Junction Field-Effect Transistors

Despite the early invention of the JFET by Shockley in 1952 [207] and its demonstration one year later [41], this type of FET has found limited applications when compared to the MOSFETs or bipolar transistors. JFETs are used for amplifiers, switches, voltage-controlled resistors, constant current sources, mixers and oscillators as discrete devices or in the input stage of operational amplifiers [60]. The attractive properties of JFETs are high input impedance, low noise and negative temperature coefficient at high current levels. These transistors are considered to be very prospective for application as front-end amplifiers in liquid krypton and liquid argon calorimeters for high energy physics experiments [36]. Large arrays containing many thousands of JFETs are expected to operate in a high radiation environment in some experiments. Therefore, radiation induced damage is of particular interest in determining the reliability of these transistors. Previously, the effect of neutron and gamma radiation on the dc and noise characteristics of JFETs produced by buried layer monolithic technology was reported [35,36]. In this chapter, we continue the investigation employing the new CR-DLTS technique. We also demonstrate the new technique with measurements of commercially available silicon and germanium JFETs which were tested “as received”.

7.2 THEORETICAL BACKGROUND

In Fig. 7.1 is shown a cross-section of a n-channel JFET build using buried layer monolithic technology. Details on this technology can be found elsewhere [36]. As indicated, the top and the bottom sides of the gate are connected internally. At zero or low gate

Figure 7.1 Cross-section of a silicon n-channel JFET built by buried layer monolithic technology. The channel thickness $2a$ was estimated from measurement of the pinch-off voltage to be about $1\mu\text{m}$. The epitaxial layer thickness was $5\mu\text{m}$. The dashed line indicates where a conductive channel appears, which connects source and drain and provides access to the gate-channel capacitors which are shown on both sides of the channel. Gate-source and gate-drain capacitors are also shown.

bias, the source and drain regions are connected together with the conductive channel and form a p-n junction with the top and bottom gate. When this p-n junction is biased in reverse direction, the depleted regions extend mostly in the channel area, since the doping concentrations in the gates are much higher than in the channel. The voltage, at which the depleted regions on both sides of the channel merge, is defined as a pinch-off voltage.

Let us consider an n-channel transistor. For a one-sided p-n junction between the gate and the conductive channel, and for uniform channel doping concentration N_D , the pinch-off voltage is given by [223]

$$V_P \equiv qN_D a^2 / 2\epsilon_s \quad (7.1)$$

where q is the electronic charge, ϵ_s is the semiconductor dielectric permittivity, and a is the channel depth (Fig. 7.1). When electron traps with concentration N_{TT} are present in the channel, then after sufficiently long positive filling pulse is applied to the gate all traps will be filled with electrons. The above expression then becomes

$$V_P(0) = q(N_D - N_{TT})a^2 / 2\epsilon_s, \quad (7.2)$$

where $V_P(0)$ denotes the pinch-off voltage at the beginning of a negative emission pulse, for example at moment $t=0$. During the emission pulse, the trapped electrons will be emitted, and the concentration of the occupied traps will vary as

$$N_T(t) = N_{TT} \exp(-t/\tau) \quad (7.3)$$

where τ is the emission time constant for electrons according to Shockley-Read-Hall statistics [206,78]. After sufficiently long time, all electrons will be emitted from the traps and the pinch-off voltage will be described by (7.1). Combining (7.1), (7.2), and (7.3) one can find the time variation of the pinch-off voltage

$$\Delta V_P(t) = V_P(\infty) - V_P(t) = q[N_D - (N_D - N_T(t))]a^2 / 2\epsilon_s = qN_{TT} \exp(-t/\tau)a^2 / 2\epsilon_s, \quad (7.4)$$

which shows a direct relation between the charge emitted from the traps and the change of the pinch-off voltage. As usual, it is assumed [32,85,154,155] that in the vicinity of a

DLTS peak the concentration of the ionized donors N_D will remain constant.

We have designed a system which maintains the above condition and at the same time measures $\Delta V_p(t)$ directly. It is important to note that $\Delta V_p(t)$ is independent of the transistor dimensions, and only the channel depth a is important for measurements of the trap concentration. Also, the carrier mobility, which may vary with the temperature, does not have to be taken into account since there is no explicit current measurement in this system.

7.3 EXPERIMENTAL RESULTS AND DISCUSSION

7.3.1 Silicon JFETs

Two types of Si JFETs were measured. The first type are devices fabricated using buried layer monolithic technology [35,36]. Several devices are incorporated on the same die with 5 and 7 μm channel lengths and widths ranging from 350 to 11400 μm . One set of devices was irradiated with 1MeV neutrons at a fluence of 4×10^{14} neutrons/cm². A second set of devices was left intact for comparison. Only the irradiated devices produced measurable DLTS transients.

Fig. 7.2 shows selected CR-DLTS spectra with different rate window settings. As explained in Chap. 3, the rate window is set by subtracting two data points with different time delays [127]. Three peaks which indicate electron traps denoted with E1, E2, and E3 are observed. The variation of the peaks is discussed later in this section when we compare the new CR-DLTS technique with constant-capacitance and standard capacitance-transient DLTS.

Since we record the whole transient, there are many points available to obtain Arrhenius plot data. With a large trap concentration, the signal is strong and no additional

Figure 7.2 CR-DLTS spectra of JFET J4 - $480 \times 7 \mu\text{m}^2$ with various time constant windows. The magnitude of the defect denoted with E3 is approximately twice that of defect E2.

time averaging is needed. This allows the measurement of long transients, limited only by our DLTS system hardware to a maximum of 1.3 sec. [127]. Arrhenius plots obtained from a single thermal scan are shown in Fig. 7.3. It is clear that the magnitude variation is relatively weak and does not affect the accuracy of measurement of the activation energy - the data points are fitted well with straight lines in the Arrhenius plots with a maximal standard error of 1.3 meV. However, this accuracy in finding the activation energy does not indicate the same accuracy of determination of the energy level because of the large error contributed by the field-enhanced emission [138,125,127,252,237,39] or by the inherent limitation of the rate window technique to separate defects with similar emission rates [174].

Figure 7.3 Arrhenius plots obtained from a data file containing 1.3 s long transients obtained using the new digital signal processing techniques. 50% of the data points obtained for E3 were removed for clarity. In weak electric field when field-enhanced emission is reduced, then the corresponding values are E1~0.164 eV, E2~0.225 eV, and E3~445 eV.

The traps observed in these Si JFETs are consistent with previous observations [5, 11,12,13,19,29,31,37,54,61,112,114,125,145,186,209,217,218,230,240,244,252]. Trap E1 in our notation has the characteristics of an interstitial (i) oxygen-vacancy complex O_i-V often referred to as an A-center [31,145,186,217,218,230,244]. It is an electron trap situated at approximately 0.17 eV [5,29,61,145,209,217,240,244] below the conduction band edge E_c , but also has been reported at 0.18 eV [11,12,112,114,252] and at 0.16 eV [31,230]. In our devices, E1 appears at 0.161 ± 0.003 eV which agrees with some recent results [19,37,186]. Another defect at the same energy level as the A-center is attributed to a substitutional (s) carbon related to interstitial carbon C_s-C_i [5]. No lowering of the acti-

vation energy caused by field-enhanced emission was observed. Several devices were tested from the same set under various bias conditions and employing different DLTS techniques. Indeed, when only the traps close to the edge of the depletion region are populated during the filling pulse, we observed a slight increase of the activation energy to about 0.164 eV. However, the value of 0.17 eV frequently reported in the literature remained outside the 2 meV margin of the experimental error. Our data processing techniques have been carefully tested [127] and do not produce any significant distortion of the recorded transient or error in defining the rate window which can explain this deviation. Also, we performed detailed analysis of data obtained for both directions of the thermal scan which also gives less than a 2 meV difference. This value is also consistent with the previously reported results from noise measurements [36] of the same samples. Earlier [125], we measured the A-center level at 0.166 eV in lightly doped ($\sim 10^{12} \text{ cm}^{-3}$) n-Si of buried-channel MOSFETs after 1 MeV proton bombardment to a fluence of $\sim 10^{10} \text{ protons/cm}^2$.

Defect E2 at 0.221 eV is consistent with the double-charged divacancy (V-V) [5, 11, 12, 13, 19, 29, 31, 37, 54, 61, 114, 125, 209, 217, 218, 230, 252]. In Ref. [54], it was suggested that this defect results from the combination of two defects at 0.205 eV and 0.249 eV. Our system allowed to record 1.3 s long transients, similar to the the system described in [54], but unlike the results there, our data shows no coexistence of two separate levels around 0.23 eV, even when the rate window was set to 930 ms. This value of 0.222 eV is also close to our earlier results [36, 125]. Defect E3, consistent with the characteristics of a phosphorous-vacancy pair $P_s\text{-V}$, is also known as an E-center [30, 61, 209, 230]. The measured energy position at 0.433 eV below the conduction band is close to the value of 0.44 eV referenced in the literature [5, 11, 13, 29, 31, 145, 186, 209, 217, 230, 252]. Although the accuracy in determination of the activation energy is better at high temperatures, we observed a much larger data spread in the range 0.415 to 0.451 eV, depending on the sample or biasing. This variation probably results from the different relative contributions of

two defects with close energy levels - P_s -V pair at 0.44 eV [5,13,29,145,186,209,217,218, 230], and single charged divacancy (+V-V) at 0.41 eV [12,19,61,112,114]. In Fig. 7.3 are shown the capture cross sections determined from the intercept with the vertical axis [180, 199]. We include these values in order to complement the signature data of the traps. Also, in Appendix H are shown the activation energies and capture cross sections (where available) of the defects in radiation damaged n-Si obtained by other researchers.

The trap concentration in Fig. 7.3 was calculated using (7.4). Since the accuracy of the concentration measurement strongly depends on the channel depth $2a$ (Fig. 7.1), we verified the technology information with additional I-V and C-V measurements. Taking into account the total fluence of 4.10^{14} neutrons/cm² [36] and possible defect annealing, it is obvious that each accelerated neutron creates more than one trap. The trap concentrations obtained demonstrate a high efficiency of the neutron radiation in creating electrically active centers which is attributed to the low-temperature at which the samples were irradiated [36].

In Figs. 7.4 and 7.4 are shown the CR-DLTS spectra and the Arrhenius plot of another, larger device from the same set - J1 with 11400 μ m channel width and 5 μ m channel length. Comparing Figs. 7.2 and 7.4, the independence of the signal from the device size is obvious.

The second type of silicon JFETs that we use to demonstrate the new CR-DLTS technique are commercially available devices 2N5459 and 2N5457 produced by Siliconix Inc. [265] These are discrete transistors encapsulated in TO-92 plastic packages which we attached with an epoxy compound to a ceramic 24-pin carrier in order to improve the thermal contact with the sample holder in our closed-cycle helium refrigerator. This was the only manipulation prior the DLTS measurement - the devices were not subjected to any kind of defect-generating procedure and they have not been used in an electronic circuit. We detected deep levels in only two of a set of several devices, both 2N5459. In Fig. 7.6

Figure 7.4 CR-DLTS spectra of JFET J1 - 11400 $\times$ 5 μm with various time constant windows. note the similarity with the spectra in Fig. 7.2.

Figure 7.4 Arrhenius plots obtained from the same data file which was used to extract the spectra in Fig. 7.4.

the CR-DLTS spectra of these devices are shown displaying two deep levels with low concentrations. Since the transconductance of the samples is in the range of several milliamperes per volt which contributes to the total feedback gain, we were able to perform very sensitive measurements. The Arrhenius plots of the deep levels are shown in Fig. 7.7. Notice the overlapping of the data for defect E1 in both samples. The difference in the slope of the plots for E1 is less than 1 meV. Since these devices are from the same distribution set and, most likely they have the same production history, the coincidence of the fitting lines is not surprising. However, the overlapping of the Arrhenius plot demonstrates the high precision of our DLTS system [127], since the data is for two different devices measured at identical conditions. When the source for defect generation is not known, obtaining accurate activation energy and capture cross section is important, but this is only part of the process of trap identification, as outlined in Ref. [12]. Without technological

Figure 7.6 CR DLTS spectra of general purpose silicon JFETs 2N5459. These devices were tested “as received” without any intentional damages. Note the y-axis scale and the sensitivity of the measurement.

Figure 7.7 Arrhenius plots of the traps in the CC DLTS spectra on Fig. 7.6. Note the minor difference in the energy level and capture cross section of E1 in both samples.

data, we limit our comments only to the demonstration of the new CR-DLTS technique as a potential tool for routine defect analysis and possible control in industrial environment. With a combination of current-voltage (I-V) and capacitance-voltage (C-V) measurements, and with the aid of the design catalog of Siliconix Inc., the doping level was estimated to be around $5 \cdot 10^{15} \text{ cm}^{-3}$. Then, the trap concentrations were calculated using (7.4).

One possible application of CR-DLTS is to study the defect distribution in the bulk of the channel, for example, by varying the filling pulse level in order to selectively populate only fractions of the traps [138]. In Fig. 7.8, we demonstrate several CR-DLTS scans of sample 2N5459 #1 with variation of the magnitude of the filling pulse relatively to the pinch-off voltage V_p (about -5.2 V in this case). There is an obvious change in the peak magnitudes versus filling pulse level, particularly around -3 V. Again,

Figure 7.8 CR-DLTS scans with variable filling pulse level. The signal magnitude change with the filling pulse level can be used for defect profiling.

we emphasize more the aspects of possible applications of the new technique rather than the final result of the defect profiling.

7.3.2 Germanium JFETs

We demonstrate the new technique also with p-channel germanium JFETs TIXM12 produced by Texas Instrument. As in the previous case, these samples were neither used in an electronic circuit nor damaged with radiation. In Fig. 7.9 are shown CR-DLTS spectra in one device. Unlike the spectra of the previous devices, the spectra in Fig. 7.9 show bipolar signals resulting from the measurement of two-sided p-n junctions. We obtained fairly good Arrhenius plots shown in Fig. 7.10 and from these, the energy levels were found to be 0.12 eV, 0.173 eV, and 0.283 eV above the valence

Figure 7.9 CR DLTS spectra of germanium p-channel JFET TIXM12 #3. The sign reversal is probably caused by emission from electron trap inside the gate material.

band edge for H1, H2, and H3 respectively, and -0.268 eV for E1 below the conduction band. The capture cross sections determined from the intercept with the y-axis were $7.4 \cdot 10^{-15} \text{ cm}^2$, $4 \cdot 10^{-14} \text{ cm}^2$, $8 \cdot 10^{-13} \text{ cm}^2$, and $7 \cdot 10^{-16} \text{ cm}^2$ respectively. However, this data should be treated with caution because the results for the hole traps H1, H2 and H3 could be affected by the electron trap E1, or by field enhanced emission. This may explain the difference in our results with these obtained in high purity germanium by other researchers (see [15,79] and the References therein). Therefore, we limit our discussion only to illustration of the CR-DLTS in general purpose commercially available transistors. From the magnitude of the signal, it can be estimated that the sensitivity of the concentration measurement should be comparable to that of the silicon devices in the 10^{11} cm^{-3} range.

Figure 7.10 Arrhenius plots of the germanium transistor in Fig. 7.9. Note the fairly good linearity and small data spread despite the low signal level shown in Fig. 7.9.

7.3.3 Comparison of CR with CC and CT-DLTS.

To explain of the similarities and differences between constant-capacitance (CC-) and CR-DLTS, we need to review some specifics of the C-V curves of a JFET. From , we note that there are three capacitors connected in parallel: gate-source, gate-drain and gate-channel capacitors. This model is further complicated from the internal connection of the top and bottom gates. In Fig. 7.11 are shown typical C-V curves of a monolithic silicon JFET. Let us consider the possible configurations for C-V measurements.

If the p-n junction capacitance of the gate versus source or drain is measured, then we obtain curve similar to curve a). One can repeat this measurement with source and

Figure 7.11 Capacitance-voltage curves of JFET J1: a) gate to source or gate to drain capacitance; b) gate to source and drain, which are connected in parallel. The aspect ratio is $11400\ \mu\text{m}$ to $5\ \mu\text{m}$.

drain connected externally together, in order to eliminate the isolation of the two areas around and below the pinch-off voltage. Curve b) was obtained from this configuration. The source-drain symmetry of the device can be verified by multiplying the part of curve a) around and below the pinch-off voltage by a factor of two, and then comparing the result with the corresponding part of curve b). As seen in Fig. 7.11, the measured device is fairly symmetrical. In Ref. [223], the expression for the pinch-off voltage (7.1) was derived using the assumption of abrupt edges of the depleted regions extending into the channel from the top and bottom gate (see Fig. 7.1). When these regions merge, the contact between source and drain no longer exists, and this should lead to a sudden drop in the gate capacitance. However, in Fig. 7.11 shows that this sharp drop in the capacitance

extends from -0.8 to -1.2 V, and this reflects a gradual merging of the ends of the depleted regions (Debye tails). In this region of the gate voltage, the channel is depleted from free current carriers. In Fig. 7.11, this region can be defined from the bias point where curve a) and curve b) split to the bias point where curve a) multiplied by 2 deviates sharply from curve b). Above this region, the voltage variation corresponds to variation of the depletion width (and thus, capacitance) of the p-n junctions extending from source to drain along top and bottom gates. Below this “channel depletion” region, in the pinch-off region, there are just two separate capacitors of the source and drain versus (mainly) the bottom gate. The relative contribution of the gate-channel capacitance can be estimated from the smooth step in the curve b) during the transition from linear to the pinch-off region. From Fig. 7.11 it is clear, that this capacitance is dominated from the capacitance of the gate-source and gate-drain p-n junctions and the associated edge capacitances.

In constant-capacitance mode of operation, the volume of the depleted region is fixed by selecting the value of the reference capacitor. In order to compare this mode with CR-DLTS, one has to select an appropriate value of the reference capacitor, so the base line in CC-DLTS (see Fig. 4.3) during the emission pulse equals that in the CR mode. This will ensure complete depletion of the channel and emission from all charged traps in the channel. However, in CR-DLTS, the base line drives the transistor in the subthreshold region. Therefore, matching this requirement in CC-DLTS mode effectively eliminates the reaction of the traps inside the channel region - the channel will be completely depleted. As a result, the gate-channel capacitance will be independent of the gate voltage. Since the gate-channel capacitance is connected in parallel with the gate-source and gate-drain capacitors, the observed voltage transient in CC-DLTS mode will compensate for the variations in these two capacitors. This means, that the CC-DLTS signal will originate from the traps located inside the source and drain depleted regions.

In contrast, in CR-DLTS mode, the voltage transient compensates only the

charge emitted from the traps localized inside the channel, since the charge trapped in the source and drain depletion regions cannot affect the pinch-off voltage and the channel conductance. Of course, one can select a value of the reference capacitor convenient to bias the transistor in the linear region (Fig. 7.11), so the traps inside the channel can be measured. However, the existence of a conductive layer in the middle of the channel during the emission pulse will reduce the total number of the responding traps. Even if this biasing is matched in CR mode by reducing the value of the reference resistor, and the expression (7.4) is appropriately changed, there will still be a difference in the area and volume tested by the two techniques. Thus, an accurate comparison of CR- with CC-DLTS is not possible in this case. Although the two techniques use very similar instrumentation, they rely on entirely different physical mechanisms for compensation of the charges emitted from the traps. Fortunately, both techniques are area independent and, for uniform defect distribution, should ideally produce identical voltage transients. In practice, there will be some difference in the magnitude because of edge capacitance effects - the effective defect concentration will appear different even for a completely uniform defect distribution.

More significant differences will appear for small area devices. In CC-DLTS, the differential capacitance versus voltage (dC/dV) plays a critical role in the total gain of the feedback loop as an “internal gain” of the test structure, and it strongly affects the signal-to-noise ratio. Obviously, small *area* devices will have low dC/dV and, if possible at all, the CC-DLTS measurements will have a severely limited sensitivity. In CR-DLTS however, the parameter corresponding to the “internal gain” of the test structure is the transconductance of the transistor which depends on the *aspect ratio* W/L , and not on the active device area. Thus, unlike the constant-capacitance technique, the constant-resistance technique is *completely* area independent and allows for very sensitive DLTS measurement of deep-submicron devices. This is demonstrated by sensitive DLTS measurements made on $2\text{ }\mu\text{m} \times 0.2\text{ }\mu\text{m}$ MOSFETs [123].

Figure 7.12 Profiling curves of J1 ($11400\ \mu\text{m} \times 5\ \mu\text{m}$) and J5 ($400\ \mu\text{m} \times 7\ \mu\text{m}$). Circles denote CR-DLTS data, triangles denote CC-DLTS, and crosses show the data obtained from capacitance-transient DLTS after appropriate magnitude adjustment.

In Fig. 7.12 are shown several curves demonstrating the magnitude dependence of the DLTS magnitude on the filling pulse level. This is a classical method for obtaining the trap distribution in the depleted region by partially filling and monitoring the emission from only a fraction of the defects [138,2,47]. As seen in Fig. 7.12, to the first order, the trap E3 is uniformly distributed [138]. For our illustration of the potential for defect profiling using CR-DLTS, more important is the precise overlapping and smooth nature of the curves. For non-uniform trap distribution, the analysis would be complicated by the internal, non-removable interconnection between the top and the bottom gates. Thus, for low-level filling pulses (in our case around $-1\ \text{V}$), the traps in the middle of the channel will be first populated (Fig. 7.1). As the filling pulse levels goes to zero, more traps will be

charged and the signal magnitude will increase. We see this behavior in Fig. 7.11 down to zero bias, and slightly in the forward bias direction where the signal saturates.

The major difference between CR and CC-DLTS is in forward direction. Also, the difference between the two modes of DLTS is more pronounced for J1 ($11400 \mu\text{m} \times 5 \mu\text{m}^2$), a device with very large periphery as compared to that of J5 ($400 \mu\text{m} \times 7 \mu\text{m}^2$). At about -1.3 V , when the filling pulse magnitude and the DLTS signal are close to zero, the extrapolated curves cross the x-axis at different points. This corresponds to a difference in the pinch-off voltages of the devices. After appropriate scaling, the magnitude dependence of the standard capacitance-transient DLTS signal completely coincides with the curves obtained with CR- or CC-DLTS.

Figure 7.13 CC-DLTS scans of JFET J1. Below 200 K a weak peak E4 appears, but it is dominated by E3 which is tentatively assigned to a $\text{P}_s\text{-C}_i$ complex at -0.29 eV . Note the wide range of rate windows used.

In Fig. 7.13 are shown CC-DLTS spectra of device J1. The main difference between the results in Figs. 7.13 and 7.2 is in the appearance of a partly resolved peak below 200 K. We attribute this peak to a local fluctuation of P_s-C_i defect E4 located at 0.29 eV [5]. In view of the difference in the two modes of operation, we believe that this peak is related to defects mainly concentrated in the source and drain regions. Since the CR-DLTS signal originates entirely from the channel region, it may have a reduced influence of this type of defect. The activation energy and capture cross sections of the traps are shown in Fig. 7.14 and are similar to the those obtained by CR-DLTS. Also, it was possible to perform sensitive CC-DLTS measurements using three other transistors in parallel -J3, J4, and J7. The spectra are shown in Fig. 7.15 and the Arrhenius plots in Fig. 7.16. Comparing with the results from measurement of a single device J1, the area independence of CC-DLTS mode of operation is demonstrated. The minor differences can

Figure 7.14 Arrhenius plots from CC-DLTS data. The device measured is J1.

be attributed to the different area-to-periphery ratio in the two cases.

The thermal dependence of the base line voltage for one CR-DLTS and two CC-DLTS spectra is shown in Fig. 7.17. The darker line corresponds to constant-resistance mode. Around 200 K, this darker line displays a step which is related to E3 - for a given pulse period and below certain temperature, the time constant of E3 is slow and the traps remain charged all the time. This explain the similarity of the curve with thermally-stimulated capacitance curves [240]. The remaining two lines are recordings of the base line voltage during operation in constant-capacitance mode. Line #1 was obtained after the reference capacitor was adjusted at room temperature so the base line was the same as in CR mode. Note the different effect which the carriers freezing has on the CR and CC base line curves at low temperatures. This effect is more pronounced in the CC

Figure 7.15 CC-DLTS spectra obtained from measurement of three JFETs connected in parallel. Note the similarity with the spectra in Fig. 7.13.

Figure 7.16 Arrhenius plots of the defects in Fig. 7.15.

curve #2 which was recorded after the adjustment was performed at 50 K. One should note that CC curve #1 actually follows the temperature variation of the Fermi level in the source and drain depletion regions, while the CR curve is related to the Fermi level variation in the channel region. Both CC curves have slope changes around 80 K which correspond to defect E1, but curve #1 has the change associated with E3 at significantly lower temperatures. This may be related to the specific balance between carrier freezing and the shift of the Fermi level inside the source and drain depleted regions with the temperature.

In Fig. 7.18 are compared several CR-DLTS spectra of devices with different aspect ratios. Also included is a CC-DLTS spectrum of three of the devices connected in parallel. The fluctuations in the magnitude are insignificant and can be attributed to variation of the defect concentration. This suggestion is supported by the appearance of a defect E4 which we have assigned to P_s-C_i complex [5]. Notice the complete indepen-

Figure 7.17 Thermal dependence of the base line voltage is very similar to the thermal dependence of the pinch-off voltage. The darker line was recorded from a CR-DLTS run, CC-DLTS #1 was recorded after adjustment at the room temperature, and CC-DLTS #2 was recorded after adjustment at 50 K, the low-temperature end of the thermal scan.

dence of the magnitude of the DLTS signal from the size of the device. This is also true for the constant-capacitance spectrum which is influenced by the trap E4 in the same way, as it appears in the spectrum of J7, one of the devices which was connected for the CC-DLTS measurement. The largest available device in the set J1 displays the strongest signal for defect E3, and in the same spectrum, the magnitude of E2 appears almost at 60% as compared to the other CR spectra. This can be regarded as evidence for the independence of the DLTS signal magnitude from the device size or the mode chosen for the experiment - CR or CC.

The advanced digital signal processing implemented in our system [127] allows us

Figure 7.18 Comparison of CR-DLTS spectra of transistors with different size and with a CC-DLTS spectrum. The small difference in the magnitude can be attributed to variations in the trap concentrations and to edge capacitance effects. CC-DLTS spectra was obtained from JFETs J3, J4, and J7 connected in parallel.

to record 1.3 sec. long transients with just 208 data points and with 10 μ s-resolution at the beginning of the transient. In Fig. 7.19 are shown several recorded transients at a temperatures where the time constant is roughly equal to 1/5 of the duration of the emission pulse. In this way, we could record most of the decaying curve. Next, we display the traces on a semilogarithmic scale and this allows for immediate checking for non-exponential behavior. As we see in Fig. 7.19, all the traces deviate from pure exponents during the first 25% of the time. This is the reason for magnitude variation in Figs. 7.2, 7.4, 7.13, and 7.15. Less deviation is present in the transient of E1, and this corresponds to reduced variation of the peak magnitude. This non-exponential behavior is frequently attributed to field enhanced emission, distortion caused by large trap concentration, or presence of multiple

traps. However, more plausible is the cause suggested in Ref. [189] - variation of the Debye tail both with the temperature and the bias. In our case this effect is enhanced by the overlapping of the Debye tails from both top and bottom gates. Also, the bias is fixed to relatively low values near the pinch-off voltage. The difference in the magnitude between CR and CC mode of operation is attributed to the edge capacitance. We find evidence to support this suggestion in the differences between the two modes for J1 and J5 - the device J5 with smaller periphery has the CC trace closer to CR trace as compared to the much larger device J1.

Figure 7.19 CR and CC traces of JFETs J1 and J5 recorded at appropriate peak temperatures. The deviation from pure exponential decay is the reason for magnitude variation in Figs. 7.2, 7.4, 7.13, and 7.15. CT-DLTS denotes a capacitance transient trace after appropriate scaling and shifting in order to be distinguished from the CR-DLTS trace. CR-DLTS J5 - low was recorded with small magnitude of the filling pulse referred to the base line and scaled until the tail coincides with the capacitance transient trace of the same transistor.

For sensitive capacitance-transient DLTS measurements, the capacitance meter should be operated in its most sensitive range. This requires the quiescent sample capacitance to be balanced by a reference capacitor all the time during the thermal scan [54]. Because we did not have a computer controlled reference capacitor [54], we were unable to perform sensitive capacitance-transient DLTS measurements. However, our reference capacitor for CC-DLTS measurements could be temporarily used for balancing the sample capacitance at a fixed temperature. This allowed us to record the capacitance transient CT DLTS J5 in Fig. 7.19. After appropriate scaling, it coincided completely with the other transients and this proves that the non-exponential behavior is not related to a particular DLTS mode of operation - they produce identical results. In order to verify the reason for non-exponential behavior, we also recorded a transient denoted as CR-DLTS J5 - low (a. u.). It was recorded after a low-level filling pulse, just 180 mV above the base line maintained by the feedback circuit. With this low magnitude of the filling pulse only the traps localized near the edge of the depletion regions of the top and bottom gates - in the Debye tails were populated. According to the bias dependence demonstrated in Ref. [189], this should increase the non-exponential behavior. Next, we adjusted the tail of the recorded transient by scaling it to coincide with the tail of the capacitance transient, the uppermost trace in Fig. 7.19. The difference between the two curves during the first 200 ms gives strong support to the idea for the cause for non-exponential behavior suggested in Ref. [189], that the reason for non-exponential behavior is charge capture in the Debye tail region.

In Fig. 7.20 are shown CR- and CC-DLTS spectra of the germanium JFET. The area of transistor 2N5459 was too small to perform the constant-capacitance measurement with the required sensitivity. Again, there is a remarkable overlapping of the both spectra in Fig. 7.20, particularly below 120 K. Also, the CR curve demonstrates much better signal-to-noise ratio when compared to the CC curve. Obviously, for small devices, CR-DLTS is superior to CC-DLTS.

Figure 7.20 Comparison of CR-DLTS and CC-DLTS spectra of a germanium JFET. Note the increased signal-to-noise ratio of the CR versus CC spectrum.

We have observed an interesting difference between CR- and CC-DLTS spectra at high temperatures when the gates of several monolithic JFETs were connected in parallel. In Fig. 7.21 and Fig. 7.22, CR- and CC-DLTS spectra are shown at high temperatures. Not only the magnitude is substantially different, but the signal sign is also reversed. Since the devices were isolated on common, floating substrate, the minority carriers generated at high temperatures could accumulate on the external gate, and this affects the measurement in a similar way to the situation in CC-DLTS of MOS-capacitor [102]. In this case, the ratio of the external gate area to that of the measured device was important. While this is obviously a system effect, it still clearly demonstrates the different physical nature of CR- and CC-DLTS methods despite the apparent similarity of their principle of operation. When the external gate was disconnected, the strong CC-DLTS signal disappeared. Arrhe-

Figure 7.21 Effect of minority carriers generation on CR- and CC-DLTS spectra of several devices with gates connected in parallel. CC-DLTS magnitude difference depends on the size of the external device connected to the measured.

nus plots of these peaks produced almost the same activation energy of the E-center (in our notation E3), about 0.66 eV above the valence band.

7.4 CONCLUSIONS

We have applied the new constant-resistance DLTS technique to both custom made and commercially available silicon and germanium JFETs. We have demonstrated that CR-DLTS is a reliable and very sensitive tool for investigation of electrically active point defects located in the channel of the JFET. The trap concentration

Figure 7.22 Same experiment as in Fig. 7.21 but measuring only the largest available device from the set. Compare the magnitudes with these in Fig. 7.21.

was calculated without knowledge of the transconductance g_m or the mobility μ of the test device. The new technique was compared in detail to constant-capacitance DLTS. The CR-DLTS signal magnitude was demonstrated to be independent of the device size and it was shown, that for small size devices, CR-DLTS is more sensitive than CC-DLTS. Comparisons have also been made with the standard, capacitance-transient DLTS. The observed non-exponential behavior was attributed to the complex generation-recombination processes at the edge of the depletion regions in the Debye tail. In addition, the possibility for defect profiling using CR-DLTS was illustrated.

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 CONCLUSIONS

In this thesis, we introduced a new approach to signal processing in digital DLTS systems. The problems of signal recovery from noise and efficient data storage are addressed separately from the transient signal analysis. As a result of this approach, an improved digital averaging scheme for DLTS signal recovery from noise and transient data storage is proposed. We have shown that the combined action of two complementary digital averaging techniques can improve the DLTS digital signal processing. Pseudo-logarithmic time averaging is efficient in reducing the number of processed data points and improving the signal-to-noise ratio for the high frequency noise components and long delay times. We demonstrate that the normalized errors in the magnitude measurements introduced by this type of averaging remain below 1% for pure logarithmic, and below 0.1% for the case when the logarithmic averaging intervals are further divided into five or more equal parts. Continuous time averaging is well suited for improving the overall signal-to-noise ratio, for continuous display and processing of data, and for more efficient use of the computer resources. The described combination of hardware and software tools for the implementation of these techniques, supplies continuously fresh data and does not require any synchronization with the main computer program.

Compared to other digital DLTS systems, this new approach offers an improved short delay time resolution, improved signal-to-noise ratio, and more efficient data storage. At the same time it offers real-time observation of essentially noise-free transients and, like analog systems, a real-time display of the DLTS scan. The real-time display means that the displayed transient and DLTS scan can be updated on the computer screen after each pulse even for a very large number of averaged pulses and the result can be predicted well before the acquisition process reaches this number. The proposed techniques allow one to combine the powerful transient analysis of the digital DLTS methods with the sensitivity and the convenience of the analog methods. The described averaging and data reduction techniques

are intended primarily for DLTS data processing but the same principles can be useful for many other physical experiments involving transient data analysis.

In this thesis, we describe setup configurations for CC- and CR-DLTS. Also, details of the novel feedback circuit which solves the most critical technical problems for implementation of CC-DLTS are given. After a slight modification, the same circuit makes possible CR-DLTS. We comment the most important technical parameters which this feedback circuit should have in order to allow for fast and sensitive DLTS measurements. When these requirements are met, the speed and sensitivity of CC-DLTS are almost the same as in the conventional constant-voltage capacitance-transient DLTS. Also, guidelines for using the feedback circuit are presented in order to provide a practical guidance for running CC- and CR-DLTS experiments. The application of the feedback circuit is demonstrated with recorded traces and experimental results of interface trap density measurements.

We present a new variation of a DLTS technique convenient for measurement of submicron field-effect transistors, where standard capacitance DLTS cannot be used. Constant-resistance DLTS is similar to the conductance DLTS, but it is more sensitive and it does not require simultaneous measurement of the transconductance or surface mobility for calculation of the trap concentrations. In addition, the DLTS signal is largely independent from the transistor size, thus allowing measurements of very small-size transistors. The proposed technique is not restricted to metal-oxide-semiconductor field-effect transistors, but can be used also to study other field-effect transistors.

In another application, CR-DLTS is demonstrated with measurements of radiation-induced traps in buried channel MOSFETs which are used as CCD output amplifiers. The unique structure of these devices offers extended opportunities for studying the space distribution of the radiation induced defects. Still, most of the results are also valid for ordinary depletion mode MOSFETs. In addition, we show a variation of the CR-DLTS technique using back-gate driving; a technique which is applicable for studying the channel-substrate p-n junction, and the results are compared with those obtained from

constant-capacitance (CC-)DLTS measurements. Complementary measurement using front-gate and back-gate operation of CR-DLTS can help to resolve the ambiguities usually associated with DLTS measurements of symmetrical p-n diodes.

CR-DLTS have been successfully applied to study virgin and radiation-damaged junction field-effect transistors (JFETs). We have studied three groups of devices: commercially available discrete silicon JFETs, virgin and exposed to high level neutron radiation silicon JFETs custom-made by using a monolithic technology, and commercially available discrete germanium p-channel JFETs. CR-DLTS was found to be a simple, very sensitive, and area independent technique which is well suited for measurement of a wide range of deep level concentrations. Comparisons have been made with the CC-DLTS and standard capacitance DLTS. In addition, possibilities for defect profiling in the channel have been demonstrated.

8.2 RECOMMENDATIONS

8.2.1 Development of the System

Hardware development. There are several areas for improvement. First, it is useful to replace the low-noise amplifier with a programmable-gain amplifier. This would allow for the program to select convenient gain according to the signal and to avoid overload and loss of data. Another, simpler improvement is to connect a second reference resistor and to alternate between the two resistors. Thus, when measuring transistors with high conductance during the filling pulse, it would be possible to avoid overloading of the capacitance meter. As a result, the recovery time would be decreased several times and the fast portion of the transient would not be distorted. Other important improvements would be the possibility to control the values of the reference resistor and capacitor from the computer. This would offer opportunities for automated spatial profiling of the defects. Also, it would be convenient to build a small, automated relay matrix in order to change automatically the configuration from CC-DLTS to CR-DLTS or to change the measured device. A fixture to apply short filling pulses is useful for implementation of alternative

techniques for determination of the capture cross section as explained in Chapter 2.

Software development. Hardware development can be efficient only when is complemented with the corresponding software development. This is especially true when the goal is to make available gain adjustments during thermal scans, or setup, bias and test device changes between the scans. This includes routines for estimating the prevailing magnitude and for gain adjustments based on these estimates. These changes would require a new format of recorded data files which would allow for automated recognition of gain changes. Major improvements can be done in the transient data analysis. With superior raw data, all known digital techniques for transient analysis should work better. Many of them could be implemented to operate in real time and to display the trap parameters during the measurement. The references in Chapter 3 provide a good starting point.

8.2.2 Applications

The new CR-DLTS method can be tested with new types of FETs such as Silicon-on-insulator (SOI), Silicon-on-sapphire (SOS), III-V MESFETs, or high-electron mobility transistors (HEMT). Hot-carrier degradation in submicron MOSFETs can be also studied. By an independent variation of the source-substrate and drain-substrate biases, the spatial distribution of the interface and bulk traps can be investigated. Unlike the capacitance measurements, CR-DLTS uses the channel conductance as a probe. It is also very tolerant to the changes in the gain of the test structure and allows measurement of very small devices. Therefore, it makes possible to re-route the CR-DLTS test signal to a single device in a large set of devices connected together, provided that the channel conductance of each device can be tested independently. Combined with other functional tests, this would possibly allow us to identify the type of defect causing malfunction of a particular device out of many similar devices.

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Appendix A

Magnitude Errors

The following pages contain printout of a MathCAD 5.0 file which was used to transform the expressions for the magnitude errors. Below, first we set the values for example calculation, n is the group number (logarithmic index), m is the number of averaged intervals inside the group (linear index), Δt is the sampling interval, D is the programmed delay, i is the sampling index, C is the magnitude at $t=0$, $ts_{n,m}$, $tm_{n,m}$, and $te_{n,m}$ are beginning, middle and end of the averaging interval correspondingly, $Tc_{n,m}$ and τ are initial guess values of the time constant. Then, we define the error function $Er(\tau)$ in percents as a difference between the exact magnitude $Ex(\tau)$ and the averaged magnitude $Ea(\tau)$ at the mid-point of the averaging interval, and τ_{max} is the time constant at which this error occurs.

$$\begin{aligned}
 n &:= 3 \quad m := 10 \quad \Delta t := 0.01 \quad D := 0.0 \quad ts_{n,m} := \Delta t \cdot m(2^n - 1) + D \quad te_{n,m} := \Delta t \cdot m(2^n - 1) + \Delta t \cdot 2^n + D \quad Tc_{n,m} := \frac{te_{n,m} - ts_{n,m}}{\ln\left(\frac{te_{n,m}}{ts_{n,m}}\right)} \\
 i &:= 1..2^n \quad j := 0 \quad C := 100 \quad tm_{n,m} := \Delta t \cdot m(2^n - 1) + \Delta t \cdot 2^{n-1} + D \quad tm_{n,m} = 0.74 \quad \tau := Tc_{n,m} \\
 tc_{i,n,m} &:= \Delta t \cdot m(2^n - 1) + \Delta t \cdot i + D \quad ts_{n,m} = 0.7 \quad te_{n,m} = 0.78 \quad Tc_{n,m} = 0.739279 \quad \frac{te_{n,m} - ts_{n,m}}{\Delta t} = 8 \\
 Ex(\tau) &:= C \exp\left(\frac{-tm_{n,m}}{\tau}\right) \quad Ea(\tau) := \frac{C}{2^n} \sum_{i=1}^{2^n} \exp\left(\frac{-tc_{i,n,m}}{\tau}\right) \quad Er(\tau) := C \exp\left(\frac{-tm_{n,m}}{\tau}\right) - \frac{C}{2^n} \exp\left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1)\right] \cdot \sum_{i=1}^{2^n} \exp\left(-\Delta t \cdot \frac{i}{\tau}\right) \\
 Ex(\tau) &= 36.752069 \quad Ea(\tau) = 36.521876 \quad Er(\tau) = 0.230193 \\
 \text{given} \quad \frac{d}{d\tau} Er(\tau) &= 0 \quad \tau_{max} := \text{find}(\tau) \quad \tau_{max} = 0.79835 \quad Er(\tau_{max}) = 0.230895 \quad \tau := \tau_{max} \\
 \frac{d}{d\tau} \frac{C}{2^n} \exp\left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1)\right] \cdot \sum_{i=1}^{2^n} \exp\left(-\Delta t \cdot \frac{i}{\tau}\right) &+ C \exp\left(\frac{-tm_{n,m}}{\tau}\right) \cdot \frac{d}{d\tau} C \exp\left[\frac{-\Delta t}{\tau} \cdot (m(2^n - 1) + 2^{n-1})\right] \\
 C \frac{\Delta t}{\tau^2} \cdot (m(2^n - 1) + 2^{(n-1)}) \cdot \exp\left[\frac{-\Delta t}{\tau} \cdot (m(2^n - 1) + 2^{(n-1)})\right] &
 \end{aligned}$$

$$\begin{aligned}
& \frac{C}{(2^n)^2} \frac{\Delta t}{\tau^2} \cdot m(2^n - 1) \cdot \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \left[\exp \left(\frac{\Delta t}{\tau} \right) - 1 + \exp \left(\frac{\Delta t}{\tau} \right) \cdot \exp \left[\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] \right] + \dots \\
& + \frac{C}{(2^n)} \frac{\Delta t}{\tau} \cdot \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \left[\exp \left(\frac{\Delta t}{\tau} \right) - 1 + \exp \left(\frac{\Delta t}{\tau} \right) \cdot \exp \left[\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] \right] + \dots \\
& + \frac{C}{(2^n)} \frac{\Delta t}{\tau} \cdot \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \left[\exp \left(\frac{\Delta t}{\tau} \right) - 1 + \exp \left(\frac{\Delta t}{\tau} \right) \cdot \exp \left[\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] \right] + \dots \\
& + \frac{C}{(2^n)} \frac{\Delta t}{\tau} \cdot \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \left[\exp \left(\frac{\Delta t}{\tau} \right) - 1 + \exp \left(\frac{\Delta t}{\tau} \right) \cdot \exp \left[\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] \right] + \dots
\end{aligned}$$

$$\begin{aligned}
& \frac{-C \Delta t m}{\tau^2 \left(\exp \left(\frac{\Delta t}{\tau} \right) - 1 \right)^2} \cdot \left[\exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^n) \right] + \exp \left[\frac{\Delta t}{\tau} \cdot (m + 1) \cdot (2^n - 1) \right] + \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] \dots \right. \\
& + 2^{-n} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^n) \right] - 2^{-n} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m + 1) \cdot (2^n - 1) \right] - 2^{-n} \cdot \exp \left[\frac{-\Delta t}{\tau} \cdot m(2^n - 1) \right] \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] \dots \\
& + 2^{-n} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] + \frac{2^{-n}}{m} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m + 1) \cdot (2^n - 1) \right] - \frac{1}{m} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^n) \right] \dots \\
& + \frac{1}{m} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m + 1) \cdot (2^n - 1) \right] - \frac{2^{-n}}{m} \cdot \exp \left[\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] \dots
\end{aligned}$$

$$\begin{aligned}
& \frac{-C \Delta t \cdot m}{\tau^2 \cdot \left(\exp\left(\frac{\Delta t}{\tau}\right) - 1 \right)^2} \left[\left(2^{-n} - \frac{1}{m} - 1 \right) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^n) \right] \dots \right. \\
& \quad + \exp\left[-\frac{\Delta t}{\tau} \cdot (m+1) \cdot (2^n - 1) \right] - 2^{-n} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m+1) \cdot (2^n - 1) \right] + \frac{2^{-n}}{m} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m+1) \cdot (2^n - 1) \right] \dots \\
& \quad + \exp\left[-\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] - 2^{-n} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] - \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] \dots \\
& \quad \left. + 2^{-n} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] + \frac{1}{m} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m+1) \cdot (2^n - 1) \right] - \frac{2^{-n}}{m} \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] \right] \\
& \frac{-C \Delta t}{\tau^2 \cdot \left(\exp\left(\frac{\Delta t}{\tau}\right) - 1 \right)^2} \left[(m(2^n - 1) - 1) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^n) \right] - (m(2^n - 1) - (2^{-n} + 1)) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m+1) \cdot (2^n - 1) \right] \dots = 0 \right. \\
& \quad + (m(2^n - 1) - 2^{-n}) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) - 1) \right] - m(2^n - 1) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot m(2^n - 1) \right] \dots \\
& \quad \left. + \left(\exp\left(\frac{\Delta t}{\tau}\right) - 1 \right)^2 \cdot (m(2^n - 1) + 2^{n-1}) \cdot \exp\left[-\frac{\Delta t}{\tau} \cdot (m(2^n - 1) + 2^{n-1}) \right] \right]
\end{aligned}$$

$$\tau_{\max} := \text{find}(\tau) \quad \tau_{\max} = 0.79835 \quad \text{Er}(\tau_{\max}) = 0.230895$$

The error was calculated directly by setting the derivative obtained by MathCAD to zero (above), and by first finding the expression for the derivative and then setting the obtained expression equal to zero (below). This was repeated for each transformation in order to verify it's correctness. For the choosen parameters, obtaining same numerical result (0.230895%) means that the simplified expression for the derivative is correct. Here we demonstrate the correctness of the last transformation which gives the expression for the derivative shown in Chapt. 3, Eqn. (3.4).

Appendix B

Time Constant Errors

This listing is similar to Appendix A, but here the time constant error is directly calculated without finding an exact expression for the derivative. The exact time constant is calculated numerically by setting the derivative to zero and then it is compared to the time constant found by mid-point approximation. This procedure is repeated for all possible values of the group index n and linear index m .

group index is $n := 5$ with $m := 10$ averaging intervals inside containing

$i := 1 .. 2^n$ samples each $\Delta t := 0.01$ ms long with magnitude $C := 100$

The mid-point of the first delay time is $t1_{n,m} := \Delta t \cdot m \cdot (2^n - 1) + \Delta t \cdot 2^{n-1}$ or $t1_{n,m} = 3.26$ ms

The mid-point of the second delay time is $t2_{n,m} := \Delta t \cdot m \cdot (2^{n+1} - 1) + \Delta t \cdot 2^n$ or $t2_{n,m} = 6.62$ ms

The time constant calculated using mid-point approximation is $Tc_{n,m} := \frac{t2_{n,m} - t1_{n,m}}{\ln\left(\frac{t2_{n,m}}{t1_{n,m}}\right)}$ or $Tc_{n,m} = 4.743296$ ms

we define $\tau a_{\max} := Tc_{n,m}$ we set the initial guess value to $\tau := Tc_{n,m}$

Using current time delay for each sample $tc_{i,n,m} := \Delta t \cdot m \cdot (2^n - 1) + \Delta t \cdot i$ we calculate the exact time constant:

$$Tx(\tau) := \frac{C}{2^n} \cdot \exp\left[\frac{-\Delta t}{\tau} \cdot m \cdot (2^n - 1)\right] \cdot \sum_{i=1}^{2^n} \exp\left(-\Delta t \cdot \frac{i}{\tau}\right) - \frac{C}{2^{n+1}} \cdot \exp\left[\frac{-\Delta t}{\tau} \cdot [m \cdot (2^{n+1} - 1)]\right] \cdot \sum_{i=1}^{2^{n+1}} \exp\left(-\Delta t \cdot \frac{i}{\tau}\right)$$

given $\frac{d}{d\tau} Tx(\tau) = 0$ $\tau x_{\max} := \text{find}(\tau)$ $\tau x_{\max} = 4.74829$ ms

Next, we find the error in percents $Er := 100 \cdot \left(\frac{\tau x_{\max} - \tau a_{\max}}{\tau x_{\max}}\right)$ or $Er = 0.105173$ %

Appendix C

Noise Sources and Signal-to-Noise Ratio in the DLTS Transients

As mentioned in Chapt. 2, the noise component in the DLTS transient is directly related to the ability of the system to separate deep levels with similar emission rates. Therefore, a short discussion on the noise sources and their contribution to the noise components of the recorded DLTS transients is presented in this appendix.

C.3. Noise sources

Thermal (or Johnson) noise is inherent to all electrically conductive devices with limited active conductivity. It can be shown, that the reactance component does not introduce thermal noise. The thermal noise current average in frequency interval Δf [236] is defined as

$$\overline{i_{th}^2} = 4kTg\Delta f \quad (C.5)$$

where g is the small signal active conductance component. Usually this noise is orders of magnitude below the noise associated with other sources and in most cases it can be neglected.

Another noise source usually associated with the discrete nature of the current flowing through a potential barrier is the shot noise. It is considered to appear due to carriers crossing potential barriers independently and at random. For a p-n junction and Schottky-barrier, this noise [236] is defined as

$$\overline{i_{sh}^2} = 2qI(\Delta f). \quad (C.6)$$

The deep levels themselves are another source of noise – generation-recombination (G-R) noise. The physical source of that noise is the fluctuation in the total number of charge carriers exited from or trapped back into the traps. In equilibrium, at any given temperature, the deep levels at a few kT below the Fermi level are mostly filled, and those at a few kT above the Fermi level are mostly empty. Therefore, the associated G-R noise is significant only when the Fermi level is close to the trap energy level. The noise current in the case of m centers with m time constants is given by [236]

$$\overline{i_{GR}^2} = \sum_{i=1}^m \frac{A_i \tau_i}{1 + \omega^2 \tau_i^2} (\Delta f) \quad (C.7)$$

where A_i and τ_i are the amplitude and the time constant associated with the i -th center.

At low frequencies there is another source of noise, flicker noise, whose spectral density frequency dependence of about $1/f^\alpha$ and, with $\alpha \sim 1$, it is called $1/f$ noise. One pos-

sible model for this noise source involves G-R sources with continuous distribution of time constants. Two mechanisms are considered for generation of $1/f$ noise: number-fluctuation, when the number of the free charge carriers vary and mobility-fluctuation, when mobility of the charge carriers vary. Often the mobility-fluctuation is related to the surface mobility, which is in general less than the bulk mobility and may fluctuate due to interaction of the free carriers with the surface, regarded as a large defect. This can explain why the $1/f$ noise in enhancement mode MOSFETs is much larger as compared to this type of noise in depletion mode MOSFETs or in JFETs. As postulated by Hooge, the $1/f$ noise current is [236]

$$\overline{i_f^2} = \frac{\alpha_H I^2}{Nf} (\Delta f) \quad (\text{C.8})$$

where α_H is a constant (Hooge constant) of about 2×10^{-3} which vary slowly with the temperature, N is the carriers number and I is the bias current. At present, it is accepted that α_H can be several orders of magnitude smaller for small devices. For non-uniform devices, instead of N , the effective number of carriers N_{eff} is used. For practical purposes, the expression (C.8) is modified by combining α_H and N_{eff} to give a new constant K , and the powers of I and f may be set different from two and one respectively, so that by substitution in Eqn. (C.8) we get I^β and f^α .

C.4. Noise Sources in CT-, CC-, and CR-DLTS Transients

As noted by Lang in his fundamental work [138], a major advantage of the DLTS over previously used TSCAP and TSC methods is that it allows us to avoid or to significantly reduce the $1/f$ noise component in the measured signal. However, for long transients the repetition rate can be as low as 0.6 Hz and, in some cases, the $1/f$ noise component can be significant in the raw DLTS transient. The PSD technique employed in the capacitance meter strongly reduces the drift, offset and the $1/f$ noise component of the high-gain 1 MHz amplifier that is part of the instrument [251], but there remain other, frequency independent noise sources. A white noise is present at both capacitance and conductance outputs of the instrument, even without a device connected to the test terminals, particularly at high sensitive ranges. Good noise analyses of CT-DLTS systems can be found in Refs. [17,20,164,187] and they will not be repeated here.

In the case of closed loop system as CC-DLTS and CR-DLTS, quantitative noise analysis can be much more complicated, and it depends strongly on the properties of the measured device and less on the used instrumentation. The test device can be considered as a first stage in an amplifier consisting of the test device, the 1 MHz amplifier of the capacitance meter, and the feedback integrator. The output signal of this complex amplifier is a stimulus for the measured device which is at the input of the complex amplifier. Therefore, as mentioned earlier, the effective gain of the test device can significantly affect the total noise in the loop. The base line provided by the memory circuit is added to the output signal, and this can further complicate the analysis. Fortunately, a well-designed memory circuit produces a baseline with noise components well below 1 Hz and

it may be considered noiseless. The bandwidth of the loop is limited at high frequencies from the integration time constant of the feedback integrator. Since the recovery time of the capacitance meter is at best about 40 μs , there is no reason for the time constant of the integrator to be less than 8 μs . At low frequencies, the bandwidth is limited by the duration of the emission pulses.

In the case of CC-DLTS, the effective gain is the differential capacitance of the test device dC/dV . Obviously, large area devices with large total capacitance will have larger effective gain and this will reduce the noise in the system, since most of the needed total loop gain will be accomplished by the 1 MHz amplifier inside the capacitance meter, while the feedback integrator will need to contribute less gain. In contrast, small test devices with poor dC/dV will require much more gain from the feedback integrator to be added to the total gain. Since there is no PSD noise rejection in this part of the loop, the total noise may increase dramatically, particularly the $1/f$ noise component.

Similar situation exists for the case of CR-DLTS. Because the transistor is near to cut-off, there is essentially no channel current to contribute to the thermal, shot or $1/f$ noise components. The G-R noise component is also not important, since a large G-R component will also generate a very large DLTS signal. However, the above discussion about the role of the effective gain of the test device for the redistribution of the gain in the loop requires a small modification. Here, the effective gain is actually the transconductance of the FET, therefore, the ratio of the channel width to the channel length will be important and not the area of the device.

Since the MOSFETs and the JFETs used for measurements reported in this thesis have substantially different channel width-to-length ratios, direct comparisons of the noise were not possible. To our observation, the differences in the noise could be attributed more to the gain of the FET than to the type of the transistor. In practice, the role of redistribution of the gain in the loop between the 1 MHz amplifier inside the capacitance meter and the feedback amplifier could be easily demonstrated by selecting a less sensitive range of the capacitance meter, or by varying the 1 MHz test signal level.

C.5. The role of the averaging techniques for SNR improvement

Quantitative analyses of the SNR improvement resulting from the averaging technique are also complicated. The main reason is that the SNR improvement due to pseudo-logarithmic time averaging varies along the decaying transient and depends on the specific setup. As a rule of the thumb, noisy signal with a significant $1/f$ noise component is better processed with higher digital time constants selected for continuous time averaging, and this require higher repetition rates of the filling pulses to keep the acquisition time reasonably long. Still, it is possible to obtain 30-40 times SNR improvement by continuous time averaging and about 20-25 times SNR improvement (in the transient tail) by pseudo-logarithmic time averaging. Then the total SNR improvement can reach several hundred, but in this case there is also need to account for the limited resolution of the digitized signal, which in turn can also be effectively enhanced by the averaging process [251], again with variation along the time axis.

Appendix D Electrical Circuit of the Pseudo-Logarithmic Generator.

Appendix E

Electrical Circuits of the Feedback Circuit.

Appendix F

Listing of a Template for a DLTS Measurement Program

```

#include <conio.h>
#include <iostream.h>
#include <dos.h>

.... include some libraries.

#include <graphics.h>
#include "svga16.h"
#include <ieeio.h>
#define      out617(chars)      ieeewt("output 09;"chars"\n")
#define      in617()            ieeewt("enter 09\n")
#define ON    1                 /* Define some handy constants */
#define OFF   0                 /* Define some handy constants */
#define uch   unsigned char
#define      P300 0x300         //hardware communication ports/
#define      P304 0x304
#define      P307 0x307
#define      P308 0x308

...graphics definitions

void  interrupt  (*oldisr)(...);           // save old interrupt
void  interrupt far  int_resp(...);        // declare the new interrupt
routine
void      setGEN(uch &dly, uch &linnmbr, uch &octv);
                                         //setup pseudo-logarithmic generator
void      setGAIN(uch &gn);               //setup gain, if available
void      writedata(FILE *f);             //record time intervals
void      writetrace(FILE *f1,float Temp); //record trace magnitude
void      cleanup(int cod);
int      changesettings(int);
void      settemp( double stemp1, double stemp2, float rramp);
                                         //two routines for temperature control
float      meastemp( void );
extern "C" {                             //declaration of Assembler functions)
    unsigned Chtest( void );             //extended character check
    int runDMA( void );                  //DMA initialization and control rou-
tines
    int stopDMA( void );
    void startDMA(void);
    void statusDMA(void);

```

```

    unsigned initDMA(void);
    int huge ReadBuffer(unsigned Segmnt,unsigned Offst,uch Weight);
                                //read and clean memory buffer
    void ClearBuffer( unsigned Segmn,unsigned Offs );
    }
extern unsigned BUFSEG,BUFLEN, BUFBEg ,BUFEND, MODE ;
int huge      cnt[400][210];      //magnitude array
long          tm[210];            //delay array

...more global declarations

void main( int _argc, char **_argv)
{
    ...local definitions

    ...check the name and open a data file

        out617("F0R0D1B4T4C0Z1X");
        setGEN(dely,lnmbr,octvs);
        setGAIN(gain);
....   open graphics windows
        oldisr = getvect(0x72);      //save old HW interrupt vector
        setvect(0x72,( void interrupt far (*) (...))int_resp);
                                           //set new interrupt vector

        bt = inportb(0xA1) & 0xFB;
                                           //check if it is safe to initialize the DMA controller
        outportb(0xA1,bt);
            do
            {
                ...do measurements or observations until ESC is pressed
            }
    }while (chtst != 27);
    do    {    bt = inportb(P308) & 1;}while (bt==0);
    init_err = stopDMA();
    setvect(0x72,( void interrupt far (*) (...))oldisr);
    bt = inportb(0xA1) | 0x04;
    outportb(0xA1,bt);
    closegraph();                      // Return the system to text mode
    ieeewt("output 17;RAMP 0\n");
    temp = meastemp();
    sprintf(ieeestr,"output 17;SETP %5.1f\n",temp);
    ieeewt( ieeestr );
    ieeewt("local 17\n");
    ieeewt("local 18\n");

```



```

        ieeewt("local 09\n");
        if (ieeeclose()==-1) cleanup(5);
        if (fclose(fp)!=0) printf("Error closing text data file.\n");  */
    }
    /*******
void    interrupt int_resp(...)
    {
        unsigned i;
        outportb(0xA0,0x20);
        BUFO = 0;
        for (i=0 ; i<m ; i++ )
        {
            cnt[k][i] = ReadBuffer(BUFSEG,BUFO,Wgt);
            BUFO += 2;
        }
        count = initDMA();
        startDMA();
        alarm = 1;
        oldisr(...);
    }
    /*******
void    setGEN(uch &dly, uch &linnmbr, uch &octv)
    {
        int i,j;
        uch com_byte,nmbr;
        com_byte = ((dly - 1)<<4) + linnmbr - 1;
        nmbr = (linnmbr * octv) -1;
        outportb(P300, com_byte);
        outportb(P307, 0x3A); outportb(P304, nmbr);
        outportb(P304, 0 );
        m = (int)linnmbr * (int)octv;  // m-1 is the number of time data points
        BUFLen = 2 * linnmbr * octv;
        for (i=0 ; i<(int)octv ; i++ ) {
            for (j=0 ; j<(int)linnmbr ; j++ ){
                if ((i*linnmbr+j)<m)
                    if (i>0)
                        tm[i*linnmbr+j] = dly+linnmbr*(((long)1<<i)-
1)+((long)1<<i)*j+((long)1<<(i-1));
                    else
                        tm[i*linnmbr+j] = dly+linnmbr*(((long)1<<i)-1)+(j*(long)1<<i);
            }
        }
        t1 = (int)(3*(m>>2));
        if (lg==1)scaleX = MaxX/(float)(tm[m-1]);
        else     scaleX = MaxX/(float)log10(tm[m-1]);

```

```

        scaleY = (MaxY-height-25)/4096.0;
    }
//*****
void    setGAIN(uch &gn)
{
    outportb(P308, gn);
}

... graphics routines
// *****
float    meastemp( void )
{
    float tmp;
    ieeewt("output 17;SDAT ?\n");
    ieeewt("enter 17\n");
    ieeescnf("%f",&tmp);
    if (tmp<10.0) ieeewt("output 17;rang 1\n");
    else
    {
        if (tmp<25.0) ieeewt("output 17;rang 2\n");
        else ieeewt("output 17;rang 3\n");
    }
    return tmp;
}
// *****/
void settemp( double stemp1, double stemp2 , float rrate)
{
    char  ieeestr[40];
    ieeewt("output 17;RAMP 0\n");
    sprintf(ieeestr,"output 17;SETP %5.1lf\n",stemp1);
    ieeewt( ieeestr );
    delay(300);
    ieeewt("output 17;RAMP 1\n");
    sprintf(ieeestr,"output 17;RAMPR %5.1lf\n",rrate);
    ieeewt( ieeestr );
    sprintf(ieeestr,"output 17;SETP %5.1lf\n",stemp2);
    ieeewt( ieeestr );
}
// *****/

```

Appendix G

Listing of a Template for a DLTS Analysis Program.

```

...include standard libraries
#include <graphics.h>
...declare graphics routines

void      WriteTrace(char *filename);
void      WriteScan(char *filename);
void      WriteArrhenius(char *filename);
unsigned  Arrhenius(unsigned ch,int N);
void      readdata(FILE *f);
void      readtrace(FILE *f1,double &Temp,int ko);
extern "C" unsigned Chtest( void );
unsigned  chtst;
int huge  cnt[400][210];                //magnitude data array
long      tm[210];                      //time data array
float      fgain,scmag[10][400];
double     T[400],temp,T1,T2,Tdif,deltaT,scaleX, scaleY,zoomk=1.0;
                                                //temperature array and other declarations

double     intgrl[400],dcnt[210];
double l000_T[10][200],T2xtau[10][200];    //Arrhenius data points array

..other global declarations

void main( int _argc, char **_argv)
{
....    local declarations

...    selecting and handling data file name
        strcat(filename,".dat");
        if (( fp = fopen( filename,"rt" )) == NULL) {           //open and read data file
            printf("Error opening %s file.\n",filename);
            exit(1); }
        readdata(fp);
        while (!feof(fp))
        {
            readtrace(fp,T[k],k);
            k +=1;
        }
        if (fclose(fp)!=0) printf("Error closing text data file.\n");

.... graphics routines sush as....    DrawScan(t1);

```

```

    }
    wrt = 0;
    while ( kbhit()!=0)
    { wrt = 1;
      chtst = Chtest();
      if ((chtst>0x40) && (chtst<0x5B))chtst += 0x20; //convert to lower case
      switch( chtst )
      {
        case 0x4D00:      // -->
                          if (t1<m-10)  t1 +=1;      break;
        case 0x4B00:      // <--
                          if (t1>10)      t1 -=1;      break;
        case 0x9:          // tab
                          if (t1<m-10)      t1 +=10;    break;
        case 0xF00:        // shift + tab
                          if (t1>10)      t1 -=10;    break;
        case 0x5000:      // down arrow

```

... different actions on the chart depending on the key pressed

```

    }while (chtst != 27);
    closegraph();          /* Return the system to text mode*/
  }
  /*******

```

... graphics routines

```

void      readdata(FILE *f)
{
  int      ij;
  char     delys[4],octvss[43],lnmbrs[4],gainstr[5],Wgts[4],tms[8];
          fscanf(f,"%s %s %s %s %s\n",&delys,&octvss,&lnmbrs,\
&gainstr,&Wgts);
          dely = atoi(delys);
          octvs = atoi(octvss);
          lnمبر = atoi(lnmbrs);
          gain = atoi(gainstr);
          fgain = (10000.0/gain)/4096.0;
          Wgt = atoi(Wgts);
          m = lnمبر * octvs;          // m-1 is the number of time data points
  for (i=0;i<octvs;i++) {
    for (j=0; j<lnمبر; j++)
      if ((i*lnمبر+j)<m){
        fscanf(f,"%s ",tms);
        tm[i*lnمبر+j] = atol(tms);  }

```

```

        fscanf(f, "\n");
    }
    for (i=0; i<octvs; i++) {
        for (j=0; j<lnmbr; j++)
            if ((i*lnmbr+j)<m) {
                if (i>0)
                    tm[i*lnmbr+j] = dely+lnmbr*(((long)1<<i)-1)+((long)1<<i)*j+((long)1<<(i-1));
                else
                    tm[i*lnmbr+j] = dely+lnmbr*(((long)1<<i)-1)+(j*(long)1<<i);
            }
        // cout<<tm[i*lnmbr+j]<<" "; }
        // cout<<endl;
    }
    // exit(1);
}
// *****
void readtrace(FILE *f1, double &Temp, int ko)
{
    int i, j;
    char cnts[6], Temps[6], *endptr;
    fscanf(f1, "%s\n", &Temps);
    Temp = strtod(Temps, &endptr);
    for (i=0; i<octvs; i++) {
        for (j=0; j<lnmbr; j++)
            if ((i*lnmbr+j)<m){
                fscanf(f1, "%s ", cnts);
                cnt[ko][i*lnmbr+j] = atoi(cnts); }
            fscanf(f1, "\n");
        }
    }
// *****
void DrawScan(int No) // display spectrum for time(2*No)-time(No)
{ .... }
// *****
unsigned Arrhenius(unsigned ch, int N)
{ char msg[80];
    int i, j;
    double tau, Xscale, Yscale;
    struct PTS pt, z;
    tau = (double)(tm[N+lnmbr]-tm[N])/
        (100000.01*log(((double)tm[N+lnmbr]/(double)tm[N])));
    switch( ch )
    {
        case 0x3B00: // F1 //select an Arrhe-
nious data point

```

```

1000_T[0][f[0]] = 1/T[i_peak]; if (k2<1) k2 = 1;
T2xtau[0][f[0]] = (T[i_peak]*T[i_peak]*tau);f[0] += 1;break;
...more data points
    } //display and store in the global array the Arrhenius data points
    return ch;
}
// *****
routines to writethe Arrhenius data points or the spectrumpoints to a file
//*****
void boxcar(int N,double Xsc,double Ysc,struct PTS zr)
{

... calculate spectrum points, (called from the graphics routine)

    }
}

... routines to write data to files

```

Appendix H

Radiation Induced Defects in Silicon

E1 [eV] σ [cm ²]	E2 [eV] σ [cm ²]	E3 [eV] σ [cm ²]	Reference
0.184±0.004 (1.4÷2.3)×10 ⁻¹⁵	0.196±0.003 (1.7÷2.9)×10 ⁻¹⁶	0.445±0.004 (1.8÷2.4)×10 ⁻¹⁴	²⁵² Yamasaki <i>et al.</i>
0.1742±0.0014	0.2355±0.0006	0.4706±0.0015	²⁴⁰ Walker and Sah
0.17	0.23	0.42	²⁴⁴ Wang <i>et al.</i>
4.4×10 ⁻¹⁵	4.8×10 ⁻¹⁵	7.9×10 ⁻¹⁶	
0.18	0.23	0.39	¹¹² Kimerling
10 ⁻¹⁴	2×10 ⁻¹⁶	4×10 ⁻¹⁵	
0.16	0.19	0.44	²³⁰ Tokuda <i>et al.</i>
3.9×10 ⁻¹⁴	1.6×10 ⁻¹⁶	2.3×10 ⁻¹⁴	
0.17	0.23	0.41	⁶¹ Evwaraye
-	0.6×10 ⁻¹⁶	1.62×10 ⁻¹⁶	and Baliga
0.18	0.28	0.41÷0.43	¹¹⁴ Kimerling <i>et al.</i>
0.18	0.20	0.46	¹¹ Barnes
0.15÷0.18	0.20÷0.25	0.39÷0.46	³¹ Chen and Milnes
~10 ⁻¹⁴	~10 ⁻¹⁶	~10 ⁻¹⁵	
0.18	0.23	0.44	¹³ Benton and
10 ⁻¹⁴	2×10 ⁻¹⁶	>10 ⁻¹⁶	Kimerling
0.17	0.23	0.44	²⁰⁹ Song <i>et al.</i>
0.17	0.21÷0.23	0.44	²⁹ Chantre and
-	(2÷4)4×10 ⁻¹⁶	1.2×10 ⁻¹⁷	Kimerling
0.17	0.23	0.44	⁵ Asom <i>et al.</i>
0.17	0.23	0.44	²¹⁷ Su <i>et al.</i>
-	0.24÷0.26	-	²¹⁸ Su <i>et al.</i>
-	1.5×10 ⁻¹⁴ ÷2.7×10 ⁻¹⁵	-	
0.18	0.23	0.39	¹² Benton
0.164÷0.172	0.202÷0.258	0.409÷0.419	⁵⁴ Doolittle
(1.8÷7.5)×10 ⁻¹⁵	7×10 ⁻¹⁶ ÷2.2×10 ⁻¹⁴	(1.1÷1.6)×10 ⁻¹⁵	and Rohatgi
0.17	-	0.44	¹⁴⁵ Li and Li
0.16±0.01	0.25±0.02	0.40±0.02	¹⁹ Bosetti <i>et al.</i>
(1.4±0.2)×10 ⁻¹⁴	10 ⁻¹⁶	4×10 ⁻¹⁵	
0.16	0.23	0.44	¹⁸⁶ Privitera <i>et al.</i>
0.16	0.23	0.41	³⁷ Coffa <i>et al.</i>
0.1665±0.0025	0.225±0.005	0.425±0.005	¹²⁵ Kolev <i>et al.</i>
1.7×10 ⁻¹⁴	2×10 ⁻¹⁶	4×10 ⁻¹⁵	
0.1608±0.0016	0.2215±0.0016	0.4335±0.0016	¹²⁸ Kolev <i>et al.</i>
1.7×10 ⁻¹⁴	2×10 ⁻¹⁶	4×10 ⁻¹⁵	

IMAGE EVALUATION TEST TARGET (QA-3)

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