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High Voltage Circuits for Short Loop SLICs in a Low Voltage Submicron BiCMOS Technology

by

Mehran Aliahmad

A thesis submitted in conformity with the requirements
for the degree of Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
University of Toronto

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High Voltage Circuits for Short Loop SLICs in a Low Voltage Submicron BiCMOS Technology

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Doctor of Philosophy, 1998

Department of Electrical and Computer Engineering
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Abstract

This thesis deals with the integration of short loop subscriber line interface circuits (SLIC) using a low voltage submicron BiCMOS technology. The high voltage front-end of the short loop SLIC was implemented in a 5V, 0.8μm BiCMOS process. The use of a low voltage process allows the implementation of the SLIC's high voltage functions on the same chip with the rest of the high-density low-voltage circuits at much lower cost while achieving higher performance.

The short loop SLIC front-end presented includes all the required high voltage building blocks such as differential preamplifier, line drivers and power switch. Using a novel high voltage common-mode feedback circuit, the fully differential 30V preamplifier provides a wide bandwidth (more than 30MHz) with a power dissipation of only 10mW and an area of 0.1 mm^2. Three different line drivers were also presented in this thesis, all capable of driving more than 30mA loop current while operating at supply voltages as high as 30V. The first line driver uses a pure CMOS process based on a quasi-current-mirror (QCM) class AB output stage and provides a bandwidth of 2 MHz with a power of only 25mW and an area of 0.3 mm^2. A BiCMOS process is used in the second line driver resulting in improved performance and lower sensitivity to process variations. This line driver exhibits a bandwidth larger than 3MHz with 30mW power and 0.24 mm^2 area. A floating-current-mirror (FCM) PMOS output stage is used in the third line driver. This design is robust with respect to hot-carrier problems in NMOS devices and provides a very well controlled quiescent current. A bandwidth of 3.8 MHz is achieved with only 18 mW of power and 0.34 mm^2 of area.

Acknowledgments

I would like to express my sincere gratitude to Professor C.A.T. Salama for his insightful guidance and invaluable assistance throughout the course of this work.

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A special word of thanks to my parents and my brothers who have been a constant source of support and encouragement.

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CHAPTER 1

Introduction

The expanding demand for advanced subscriber services such as interactive internet access, multimedia and video-on-demand, is driving the current trend in the telecommunication industry towards providing efficient, broadband and low-cost local access networks. Currently, the widespread plain old telephone service (POTS), is the most cost-effective telecommunication infrastructure for providing multi-service access to residential and small business users. Over the past two decades, broadband technologies have been widely used in long distance and inter office transmission systems, increasing the capacity of the network as well as its quality and reliability. The old analog transmission system has evolved into a totally digital pulse-code-modulation (PCM) system with optical fibre and satellite links as the high capacity media. However, still after almost 100 years, the final connection from the central office to the subscriber has remained an analog twisted-pair copper loop, limiting the data transmission rate.

The long survival of POTS is not due to the lack of a modern alternative technology. In fact, optical fibers have traditionally been used in the network core for many years because of their high capacity and long range capabilities. Rather, it is because the local exchange network involves a unique combination of cost and engineering barriers. With more than 600 million telephone subscriber worldwide, the investment required to replace the existing infrastructure is immense, while the investment return from domestic customers is limited.

Therefore broadband media such as optical fibers, although economical for long-distance high-volume transmission, are still far from replacing the copper lines.

In order to reduce the cost per customer in the new emerging technologies such as fiber-in-the-loop (FITL) or hybrid-fiber-coax (HFC), the broadband media are shared by a number of subscribers. In these techniques, broadband links extend beyond the central telephone office to a service access point close to the subscriber premises and short copper lines connect the subscriber to the service access point. The main advantages offered by these systems include:

- dividing the installation cost of the broadband system among many users, thus reducing the access cost per customer,
- reducing loop lengths to increase the maximum data transfer rate of the copper loops, and
- maintaining POTS compatibility (which is the main concern of the telephone companies).

In order to provide a variety of different services including voice, video and data, these new systems will require a large amount of VLSI circuitry. One of the most challenging blocks required is the subscriber loop interface circuit (SLIC) which provides the appropriate signaling for POTS. Conventional SLICs have long been used in telephone central offices to drive twisted pair copper loops. Traditionally, SLICs are implemented using a number of separate chips and discrete components to perform the various high voltage and low voltage functions required. Due to the high voltage requirements and functional complexity involved, the integration of SLICs has been an enduring challenge. Although dedicated high voltage integrated circuit processes have been used in implementing central office SLICs, the next generation of SLICs for shorter loops, will

require a higher level of integration at much lower cost. This can best be achieved by using an advanced VLSI process with enhanced high voltage capabilities.

In the following sections, the conventional SLIC is introduced and its high voltage functions are discussed. The evolution of short loops and their application in future local access networks are then discussed followed by a review of the characteristics of short loop SLICs. The choice of an appropriate technology for short loop SLIC implementation is addressed next by considering the current state of high voltage integrated circuit processes and discussing new techniques used to increase the high voltage capabilities of a low voltage VLSI process. Finally, previous related work is reviewed and the objectives and outline of the thesis are presented.

1.1 Subscriber Loop Interface Circuits (SLIC)

The subscriber loop refers to the circuit formed by twisted-pair copper lines (named Tip and Ring) connected to the central office or a private branch exchange (PBX) at one end and the terminal equipment (such as the telephone, fax machine,...) at the other end as illustrated in Fig. 1.1. Generally, the loop performs the following functions:

- provides power for the terminal equipment from the central office,
- transmits bidirectional voice or data signals between the calling and called parties,
- carries bidirectional control signals (supervision) between the subscriber and the central office, and
- passes ring signals to the called party.

The subscriber loop can be considered as the exchange access portion of a telecommunication channel as illustrated in Fig. 1.2. The core of the transmission network between the central offices, referred to as the inter-exchange access, uses broadband communication channels such as optical fiber, microwave radio systems and satellite links

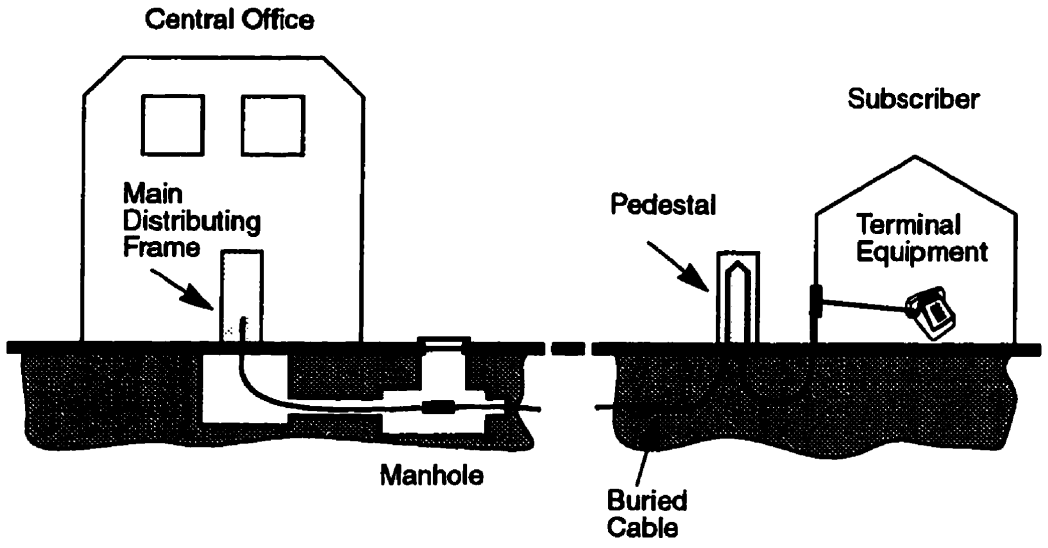


Fig. 1.1: Subscriber loop connecting the subscriber to the central office

incorporating digital PCM systems. The copper loops, as the end links of the communication channel, have remained completely analog as originally introduced.

The copper lines are connected to the line cards at the central office. For each subscriber, there is a subscriber loop interface circuit (SLIC) on the line card handling all the signaling through the loop. SLICs act as the interface between the digital PCM network and the analog loops.

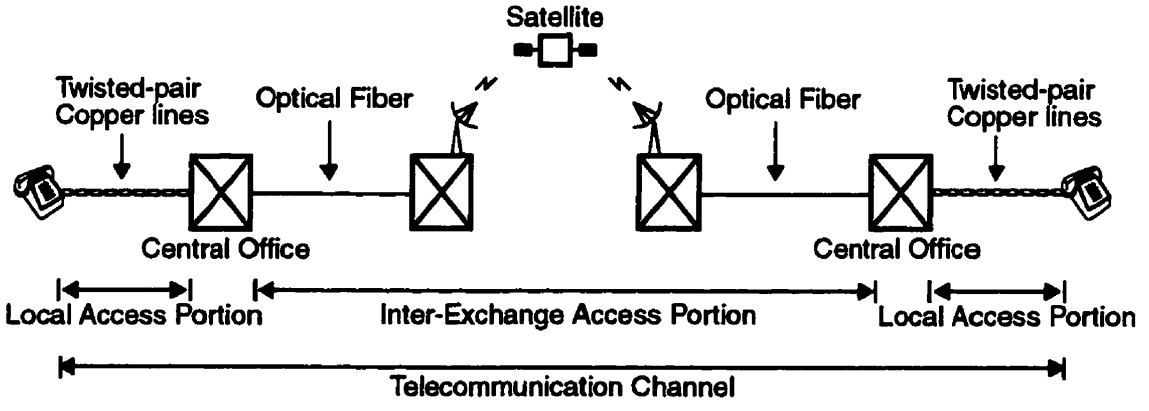


Fig. 1.2: A typical telecommunication channel

A SLIC must support a wide variety of functions referred to as BORSCHT functions [1-2]. BORSCHT stands for Battery feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid and Test. Fig. 1.3 shows a simplified diagram for a conventional SLIC, performing all of the above mentioned functions.

One of the main functions of the SLIC is to supply direct current from the central office battery to the loop. This is the only source of power for passive terminal equipment such as a telephone set. As shown in Fig. 1.3, the 48V DC source is connected to the loop through two 200Ω feed resistors. The reason for the high battery voltage and the feed resistors is that the loop resistance changes over a wide range from almost zero for short loops, to 1500Ω for long loops. While minimum power must be delivered to the telephone set in a long loop, the line current must be limited in a short loop with small resistance.

The SLIC is responsible for transmitting and receiving voice signals on the loop. The transmission on the loop is a full-duplex two-wire transmission while there are separate

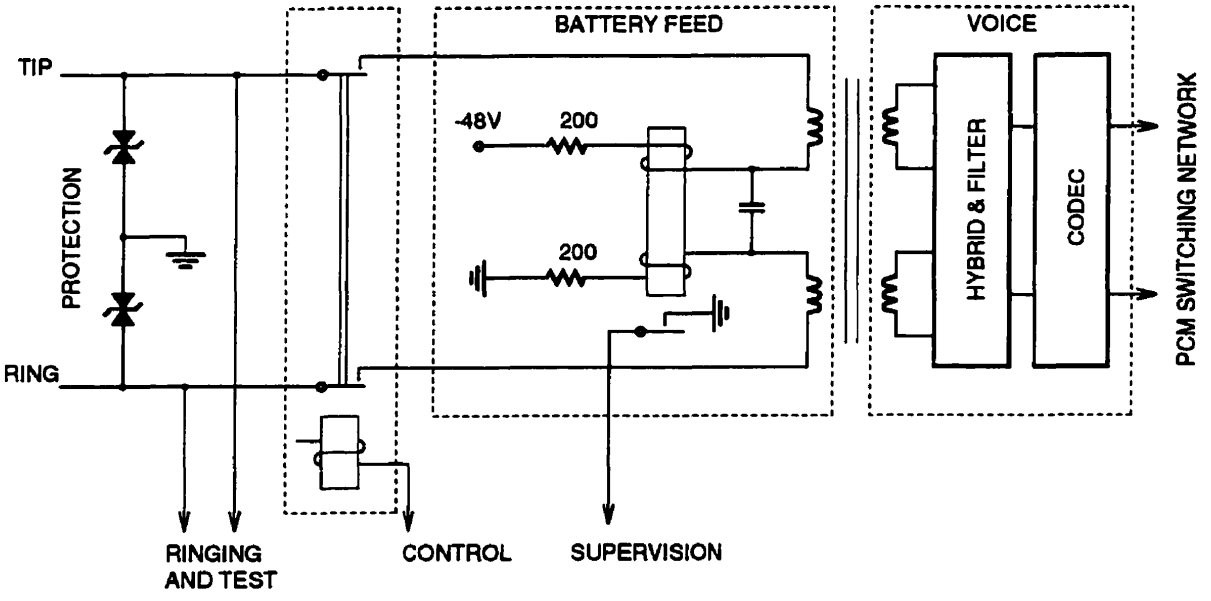


Fig. 1.3: Schematic of a central office SLIC

channels for receiving and transmitting signals (four-wire) in the switching network. The hybrid circuit in the SLIC performs the two-wire to four-wire conversion. This circuit is connected to the PCM highway through a codec block including A/D and D/A converters. The SLIC must also provide a suitable ac impedance (ranging from 135Ω to 1200Ω for different standards) for a matched loop termination.

The loop current is monitored by the SLIC to determine the on-hook and off-hook conditions. Furthermore, all other signaling such as dialing, call processing tones and test signals are provided by the SLIC.

In order to ring the telephone set, a high voltage (90Vrms) ring signal is applied to the loop. The ringing signal frequency is in the range of 16 to 66 Hz. A ring signal generator on the line card provides the required signal which is switched to the loop by the SLIC.

Buried or aerial loop wires are exposed to hazardous electrical interference that may cause high potential surges in the loop. High voltage spikes caused by lightning, power lines contacts or power line induction can damage the circuits connected to the loop. Therefore, protection devices must be provided at both ends of the loop (at the central office and subscriber's premises) to prevent destructive damage.

1.2 Short Loops and Their Applications

The current trend in the telecommunication industry is towards providing advanced subscriber services such as interactive internet access, video-on-demand and HDTV by deploying broadband communication systems into the existing telephone networks. However, the small bandwidth and poor noise and interference characteristics of twisted-pair copper loops severely limit their use for high-speed digital services.

The ideal solution is to replace the copper lines with a wideband media such as coaxial cables, optical fibers or radio links. This has led to a number of new proposed network

architectures such as fiber-in-the-loop(FITL)[3], hybrid-fiber-coax(HFC) [4] or wireless-local-loops (WLL) [5]. These systems are briefly described in the following sections.

1.2.1 Fiber-In-The-Loop (FITL)

FITL refers to the use of fiber optic transmission beyond the central office and close to the subscriber. The ultimate goal of the telecommunication industry is to extend the fiber all the way from the central office to the terminal equipment at the subscriber's premises. This technology, referred to as fiber-to-the-home (FTTH), provides the full fiber bandwidth which offers enormous capacity to the user. However, replacing the whole copper infrastructure with a completely new system will not be economically feasible for the telephone industry for at least another decade [3].

A loop survey compiled by Bellcore [6], shows that the average existing loop length is 3.5 km with more than 75% of the loops shorter than 4.5 km. Fig. 1.4 shows the loop length distribution in residential areas [6]. While fiber connections are more economical for loops longer than 4 km (which mostly use digital loop carriers such as T1), they are too costly for a majority of loops with lengths shorter than 4 km [6].

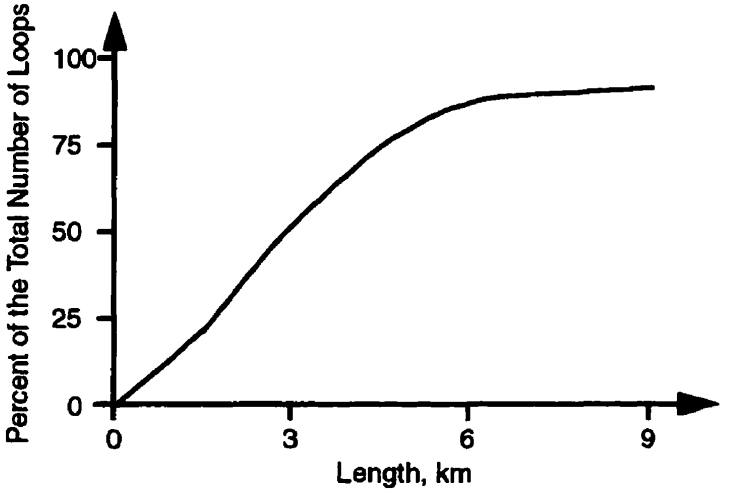


Fig. 1.4: Cumulative distribution of existing loops in terms of length [6]

A rough estimate for the first installation cost of a FTTH system is about $1500 per customer [3]. Therefore, replacing the entire copper network would require a huge investment in the range of trillions of dollars. Any payoff from such a large investment must come from the customer who is not expected to require the extremely wide bandwidth of the whole fiber in near future.

Furthermore, replacing the existing infrastructure would take no less than two decades. The fastest estimated rate of installing new cables is 7% per year [7]. Since the number of telephone lines is growing at about 3% annually, the net replacement rate would only be 4%.

Studies [7] conclude that the transition from copper to fiber is not likely to happen in one step. Therefore, the telephone companies are looking for interim solutions towards the broadband network of the future. One of the most popular solutions is fiber-to-the curb (FTTC) which is capable of supporting POTS and can eventually be upgraded to FTTH [8].

In FTTC systems, fiber is brought to within 150-300m of the subscriber to an optical network unit (ONU) located on a pedestal[1]. Copper drops then carry the POTS signals from the ONU to the subscriber. Fig. 1.5 illustrates a FTTC architecture. In the ONU, there is an optical interface for transmitting and receiving signals over the fiber. The ONU also includes circuitry for multiplexing and demultiplexing different signals onto the optical channel. Both time division multiplexing (TDM) and wavelength division multiplexing (WDM) are used in the proposed systems. SLICs are also included in the ONU to drive the short copper loops.

The intent of the FTTC system is to share the cost of the optical network among many subscribers. The level of sharing represents a trade-off between cost and bandwidth. If a

1. FTTC systems are also called Fiber-To-The-Pedestal (FTTP)

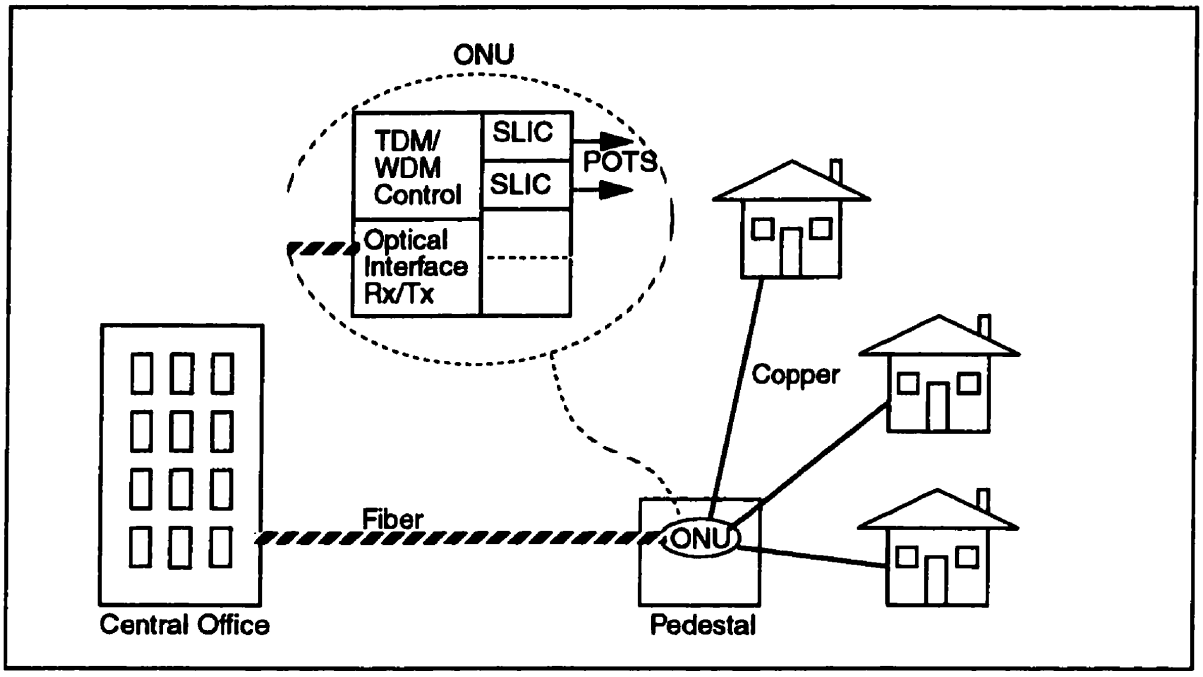


Fig. 1.5: Schematic of a fiber-to-the-curb system

large number of customers are served by the ONU, the cost of common functions on a per-line basis can be reduced. On the other hand, moving the fiber further away from the customer increases the copper length reducing the data transfer rate. Fig. 1.6 shows an estimate for the cost per subscriber versus the number of customers sharing the same fiber [9].

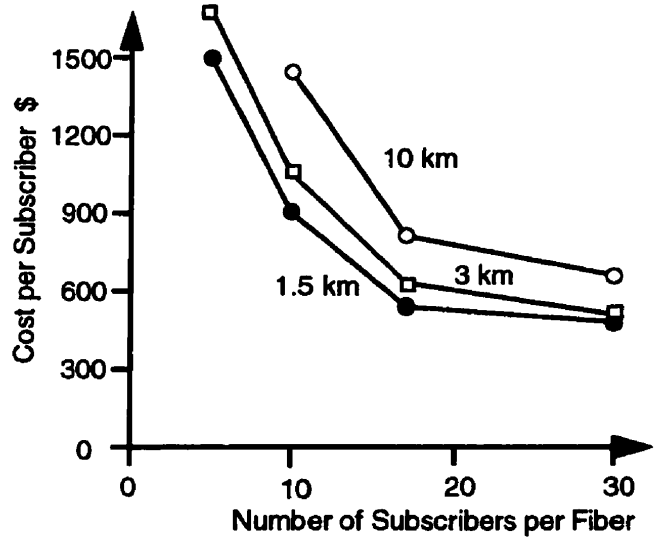


Fig. 1.6: Estimated initial cost of the installation of FTTC systems per customer

1.2.2 Hybrid-Fiber-Coax (HFC)

Although the fiber bandwidth is shared by a number of customers, the capacity of FTTC is expected to be sufficient for the near future. Short loops in the range of 100 meters are capable of transmitting in excess of 10Mbit/s, while placing shielded pairs in the loop could provide transmission rates of up to 100 Mbit/s. A coaxial cable could broadcast as many as 150 NTSC video channels or multiple DS-3 (45 Mbit/s) signals. Such bandwidths can be achieved with hybrid-fiber-coax (HFC) systems [6].

The HFC mostly supported by cable TV companies, is mainly designed for providing interactive multimedia services such as video-on-demand [4]. However, they are also capable of supporting POTS and data. Fig. 1.7 illustrates the structure of a HFC system. The central office transmits optical signals over the fiber to an optical node installed in the serving area. Optical signals are then converted to electrical ones at the optical node and are transmitted to the subscribers through a coaxial cable network typically serving a couple hundred users. A network interface unit (NIU) installed in a wall-mounted box at the

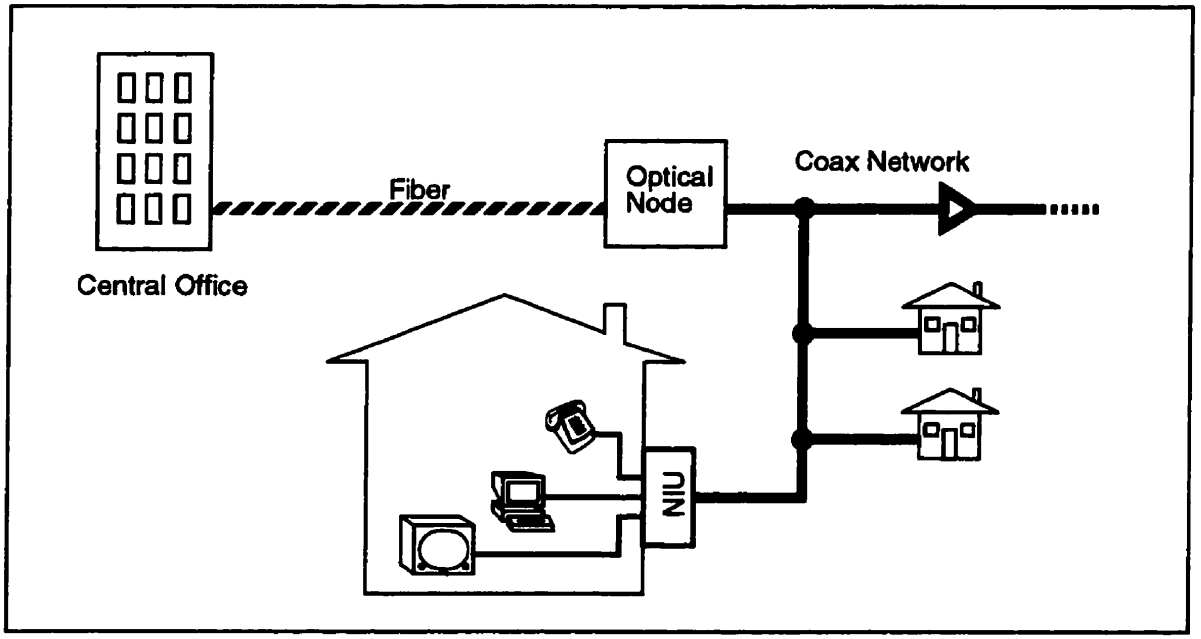


Fig. 1.7: Schematic of a hybrid-fiber-coax system

subscriber's home, separates different services for computers, TVs and telephone sets. To drive telephone lines inside the house there will be a SLIC in the wall box as well as other interface circuits for other services.

1.2.3 Wireless Local Loops (WLL)

Wireless Local Loop (WLL) is a generic term for a local access system in which a wireless link instead of conventional copper lines, is used to connect subscribers to the local exchange office. Originally, WLL systems were proposed as a cost effective solution to provide voice service for developing nations without a widespread wired telecommunication network. A large portion of the total investment and the development time in providing telephone access in rural areas is spent on installing subscriber loops. By using a wireless link, the telephone network can penetrate far into the unwired areas in a short period of time because of the small amount of construction involved in installing a WLL system. A typical WLL architecture is illustrated in Fig. 1.8. The central office is connected through a fiber or coax cable to a radio link which can be installed on a building

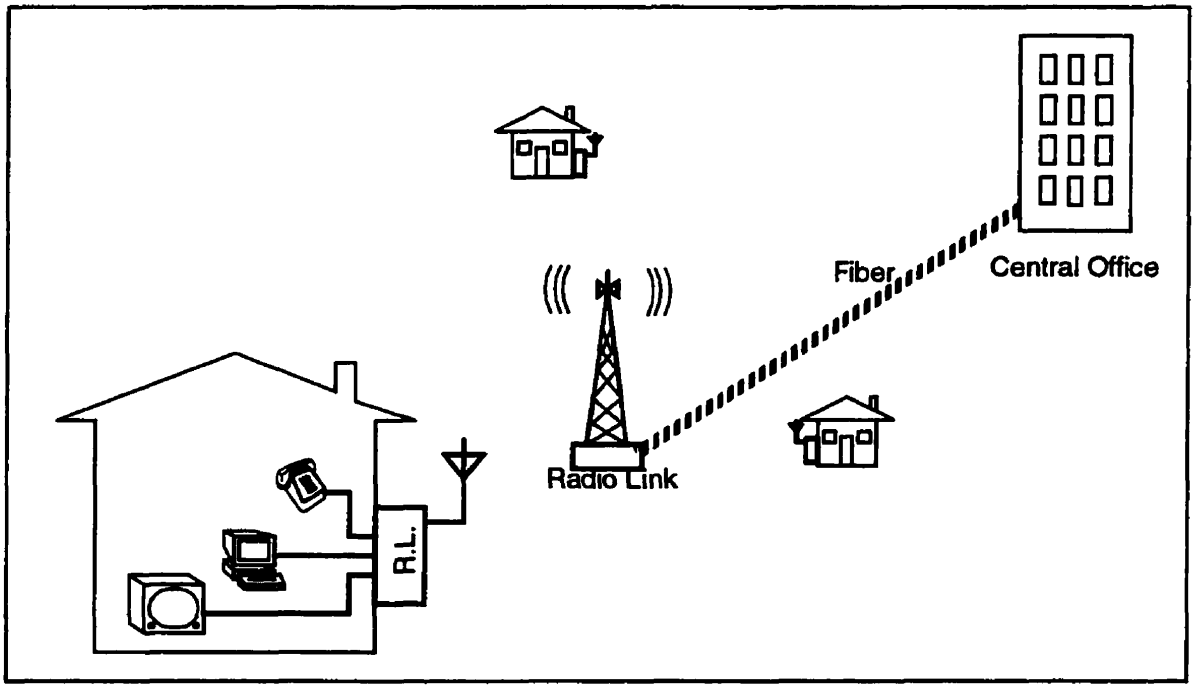


Fig. 1.8: Schematic of a wireless local loop system

or a utility pole in a residential area. A wall-mounted box at the subscriber's house includes a radio transceiver as well as short loop SLICs and other interfaces for telephone sets and data terminals.

Recently, WLL has gained increased attention in the developed and underdeveloped countries as a potential rival to other broadband access architectures. Using existing cellular and PCS infrastructures, WLL can deliver voice and data services at higher rates and lower cost [5].

1.3 High Voltage Integrated Circuits Processes

The implementation of SLICs requires the use of high voltage integrated circuits (HVIC) which are defined as integrated circuits that combine high voltage devices with low voltage components on a single chip. Using mostly lateral devices, HVICs are able to sustain high voltages with limited current handling capability.

High voltage integrated circuits are usually classified in terms of the type of isolation technique employed [10]. The three types of isolation schemes encountered are: junction isolation (as in bipolar processes), self isolation (as in CMOS) and dielectric isolation including silicon-on-insulator (SOI) processes. Although SOI technologies provide superior performance, they are not attractive due to their high complexity and cost. Therefore, most practical HVIC solutions are based on junction or self isolated processes.

There are two major approaches to developing junction isolated or self isolated technologies for HVICs. In one approach, an optimized high voltage device structure is designed and the low voltage control components are built around it. This results in high performance high voltage devices but poor-quality low voltage components. The other approach involves starting with a low voltage CMOS or BiCMOS process and incorporating high voltage devices within it. Since these processes are not optimized for high voltage operation, the performance of the high voltage components is usually limited.

A dedicated HVIC process, based on the former approach, usually uses a thick epitaxial layer (10 to 25μm) to provide high breakdown voltages. However, the controllability of such processes is more complicated as a result of deep diffusions required. Also, a larger isolation area, larger feature sizes and increased parasitics, severely degrade the performance of the low voltage devices. Therefore, compared to a low voltage VLSI process, dedicated HVIC technologies provide less integration density at a much higher cost.

Prior to the mid-eighties, most high voltage ICs were realized using pure bipolar processes. With the growing request to incorporate more control logic functions on the chip, CMOS replaced I^2L logic in the control sections of high voltage ICs. Meanwhile, the advent of power MOS devices which unlike bipolars, do not need DC driving current and provide fast switching speed, greatly influenced the development of high voltage ICs. Advanced high voltage IC processes merge different device structures onto the same chip. Junction isolated BCD (Bipolar, CMOS DMOS) smart power technology[11] is an example of such a process, a cross section of which is illustrated in Fig. 1.9. BCD processes were first introduced in the late eighties. The main high voltage devices are vertical n-channel DMOS transistors and extended drain PMOS devices. The process also provides low voltage CMOS and bipolar transistors. The first generation of BCD processes offered 4μm minimum gate length DMOS devices in three different versions with voltage ratings of 60 V, 100 V and 250 V, respectively. The main difference between these three versions is the thickness of the epitaxial layer (10-23μm). In the second and third generations [12], the minimum feature size was reduced to 2.5μm and 1.2μm respectively, with the latest submicron version providing 0.6μm DMOS transistors with 0.8μm, low voltage CMOS devices. However, the breakdown voltage has drastically dropped from 250V to 16 to 40V for lateral devices and 60 to 80 for DMOS transistors. Also with more than 20 masks, the complexity and cost of this process is much higher than a low voltage BiCMOS technology.

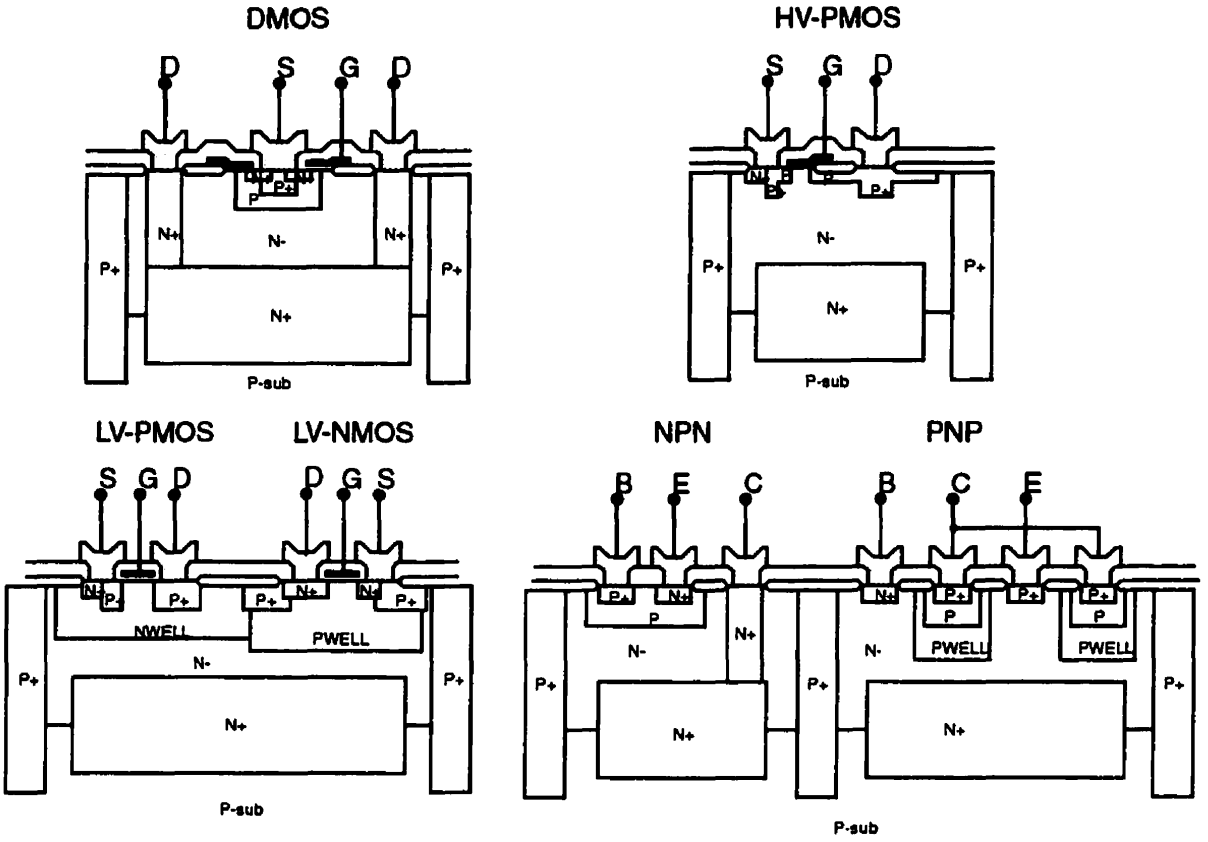


Fig. 1.9: Cross-section of BCD process and compatible devices

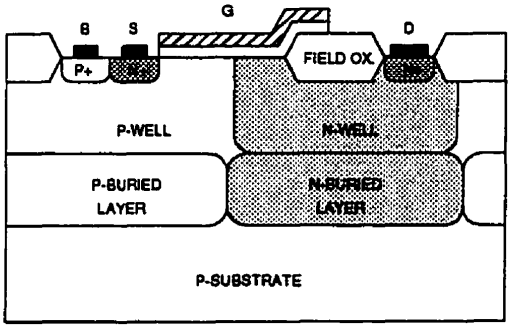
On the other hand, adding high voltage capabilities to a low voltage process can be advantageous in applications where low voltage circuits form a large proportion of the system. This approach is more economical as the cost of an advanced low voltage CMOS or BiCMOS process is much lower than that of a BCD type technology. Moreover, because of the higher levels of integration, this approach results in further area and cost reduction for complex systems. The ability of using existing low voltage circuit libraries also helps reduce the development time and cost.

Fig. 1.10 shows the cross section of high voltage NMOS and PMOS devices compatible with a submicron BiCMOS process [13-14]. These structures are based on a lateral extended drift region at the drain of the transistor to withstand high voltages. In order to keep the compatibility with the low voltage process and avoid additional processing steps, the low doped well regions are used as the drain drift region. These devices are

implemented by appropriate layout without any modification to the low voltage process. Further improvements to the lateral devices can be achieved by utilizing the reduced surface field (RESURF) concept in the design [15].

1.4 Previous work on SLICs

The challenge of integrating SLICs stems from the variety of different functions and the wide range of operating voltages and power required. There have been various attempts at developing central office SLICs using dedicated HVIC processes. Due to limited density and flexibility of these processes, these chips can only include a small number of the SLIC functions. As a result, today's line cards include a chip set along with a number of off-chip components such as transformers, relays and other discrete devices. Although this thesis is the first work that specifically targets the integration of a short loop SLIC in a low voltage process, it is useful to review reported solutions for conventional SLICs.



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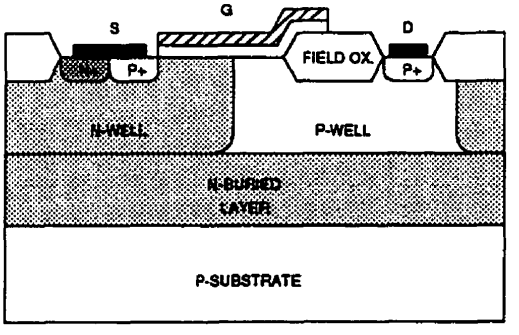

(b)

Fig. 1.10: High voltage MOS devices in low voltage BiCMOS process

Several attempts at integrating SLICs in a dielectrically-isolated bipolar process have been reported [16,17]. However, they have remained at the experimental stage without offering a real practical solution as a result of their high cost.

Until recently, when the BCD (Bipolar-CMOS-DMOS) technologies became popular [18,19], most of the proposed SLICs were implemented in high voltage bipolar processes [20]. As a result, they included only a limited amount of control circuitry, usually implemented in I^2L logic. Consequently, a multi-chip approach was used to separate the low voltage and high voltage functions [21-22]. Currently, there exist a number of commercial ICs for SLIC applications implemented using high voltage bipolar processes. The latest line of products in this category allows the use two different power supplies to compensate for the loop length variations [23].

Recent attempts at implementing monolithic SLICs, include the implementation of high voltage amplifiers for line driving functions, fabricated in a 100V version of the BCD process[24]. These amplifiers, designed for conventional SLICs use a combination of class AB and class B output stages to control the quiescent current and provide high output current. These circuits mostly use vertical DMOS and high voltage PMOS devices to withstand the high operating voltages. Although these circuits can be useful for conventional SLICs, they are not suitable for short loop applications due to their large area (4 mm^2 for each line driver) and limited bandwidth (less than 1MHz).

Another multi-chip solution for a SLIC has been reported recently [25]. This chip was implemented in a 170V BCD process [18]. It occupies 30 mm^2 of area and dissipates 1.3 W. Similar to other HVIC SLICs presently available, this SLIC also suffers from limited density and high cost.

Because all the available SLICs use a dedicated HVIC process, they are economically unattractive for short loop applications where a compact and low cost solution is desirable.

Therefore, it would be quite advantageous to consider a cost effective low voltage process for implementing a short loop SLIC. There has been no previous report of such an approach to solving the problem prior to the work presented in this thesis.

1.5 Objectives and Outline of the Thesis

Several architectures are presently competing to become the dominant local access network of the future. Although their characteristics and cost differ over a wide range, the need for short loop copper access is ubiquitous. The escalating capacity and complexity of the new systems require better performance and a higher level of integration at minimum cost. Yet, to maintain the compatibility with POTS, the high voltage requirements of the short loops must be satisfied. Thus, the objective of this thesis is to investigate the feasibility of integrating the high voltage building blocks of a short loop SLIC in an advanced low voltage submicron BiCMOS process. By enhancing the voltage handling capabilities of the BiCMOS process, the high voltage building blocks are designed and implemented with minimum area and power in order to efficiently integrate a large amount of low voltage circuitry on a single chip. Achieving this goal results in a highly economical solution for the cost-driven local access networks of the future.

In Chapter 2, the requirements for short loop system are discussed. An architecture for the SLIC's high voltage front-end is proposed and the high voltage building blocks are introduced. Chapter 3 deals with device and process issues. The high voltage capabilities of the BiCMOS process used in this thesis are examined in this chapter. The structures, layouts and mask layers used for implementing different high voltage devices are described and a set of electrical circuit models are developed.

Chapter 4 contains a detailed description of the SLIC components. The design of the high voltage building blocks are presented along with the implementation and experimental results. Conclusions and guidelines for future work are presented in Chapter 5.

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CHAPTER 2

Short Loop SLIC System

2.1 Introduction

The challenge in integrating SLICs stems from the variety of different functions and the wide range of operating voltages and power which must be implemented on chip. While a large number of codec and control functions are required in the low voltage back-end of the system, line feed functions are the bottleneck at the high voltage front-end. A successful approach to such integration must include careful system design as well as suitable choice of technology. This chapter deals with the system aspects and the proposed architecture for the short loop SLIC. Technology issues and the characteristics of the process used to implement the system is the subject of the next chapter.

The main objective of the system design is to reduce the area and the power dissipation of the high voltage portion of the chip. This objective can be achieved by minimizing the complexity of the high voltage parts and transferring as many functions as possible to the low voltage back-end. This has resulted in a suitable architecture that satisfies all the short loop requirements.

This chapter starts with the general specifications of the short loops. The architecture of the high voltage front-end of a short-loop SLIC is then presented and a functional explanation of each high voltage building block is provided.

2.2 Short Loop SLIC Requirements

The requirements for short-loop SLICs differ from those of conventional ones currently employed in central offices. Traditionally, high driving voltages are used to compensate for the large voltage drops in the long loops due to their high resistances. The DC voltage of the loop is provided by a standard 48V battery located at the central office. The loop voltage can rise even higher during ringing, when an AC ring signal in the range of 90V is injected in the loop. However, the loop resistance is much smaller in short loops resulting in less stringent voltage requirements on the interface circuits. Table 2.1 presents the Bellcore recommendations on the maximum loop resistance for three different systems [1]. Due to the small loop resistance in the FITL and other short loop systems, the battery voltage can be reduced to the recommended 24V [2]. Similarly, the ring signal can be decreased to 40V or less for short loop applications.

There is no specific requirement on the loop current and therefore it is allowed to vary over a wide range. However, most low power systems limit the loop current to below 30 to 50 mA [2]. Meanwhile, the internal current of the SLIC must be kept to a minimum in order to keep the on-chip power dissipation as low as possible.

Unlike Conventional SLICs which are mainly designed for voice transmission with limited bandwidths, short loop SLICs are expected to support high speed modems and

Table 2.1: Maximum loop resistance for different systems

	Max. Loop Resistance (Ω)
Central Office (LSSGR[3])	1500
Digital Loop Carrier (TR57[4])	900
Fiber In The Loop FITL (TR909[5])	17[1]

1. Specified as 150 feet of no. 22 American Wire Gauge (AWG) wire at 65 C.

digital subscriber loop (DSL) systems as well. Therefore, a higher bandwidth (more than 1MHz) is expected from short loop systems.

2.3 Proposed Architecture for a Short-Loop SLIC

A conceptual architecture of the high voltage front-end of the short loop SLIC is illustrated in Fig. 2.1 [6-7]. A voltage-drive, current-sense approach is used in this architecture. In this configuration, the lines are driven by voltage sources while the loop current is controlled. The other alternative is to drive the loop with current sources to control the loop current. The former approach is more power efficient especially for short loops where the loop resistance is small and lower driving voltages are required. As a result, the power supply voltage of the SLIC can be reduced to decrease the overall power consumption.

The main signal path consists of a differential preamplifier and two high voltage line drivers for the Tip and Ring lines. The voice (or data) information is processed in the low voltage section of the SLIC (including codec, hybrid and control circuitry) and is provided as a low-swing (in 5V range) AC signal V_{in}. This signal is then amplified and converted to two differential signals V_r and V_t by the preamplifier stage. The preamplifier also shifts the DC levels of V_r and V_t to provide the required DC line-feed voltage. The DC level is controlled by a low voltage control signal V_{dc}, injected at the input of the preamplifier. This signal is generated by the low-voltage control circuitry based on the loop current.

Since the preamplifier is a fully-differential stage, its output common-mode voltage is independent from the input signal. Therefore, common-mode feedback circuitry is required to adjust the common-mode level of the two differential outputs of the preamplifier as illustrated in Fig. 2.1.

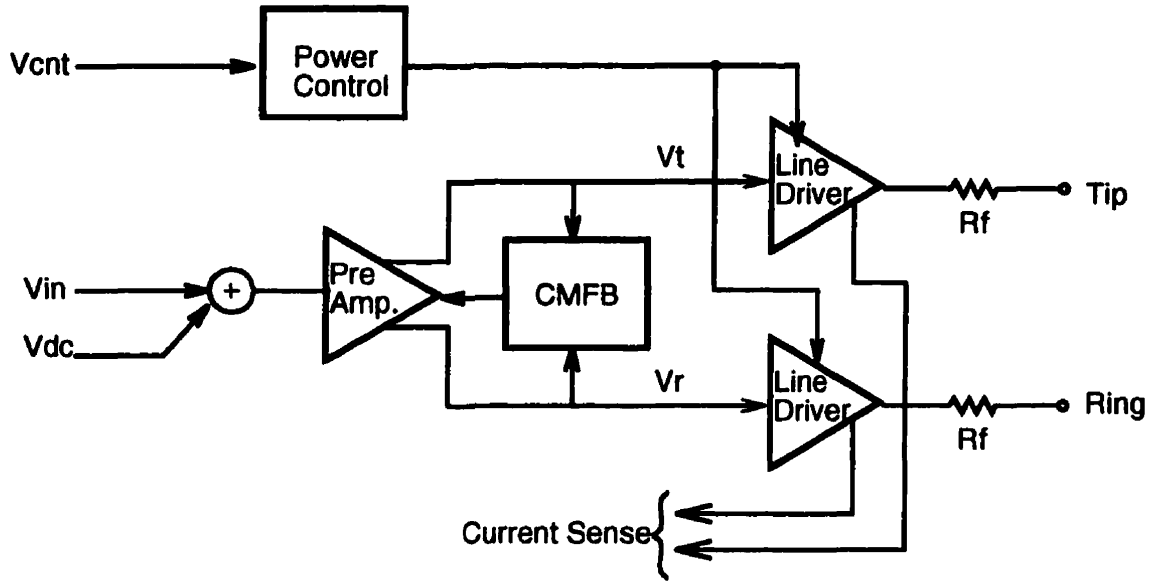

Fig. 2.1: Architecture of the high voltage front-end of the short-loop SLIC

The two line drivers are the most important components of the system. They must provide large currents to the loop while handling high supply voltages. Also a high bandwidth, low output impedance and high power supply rejection ratio is expected from the line driver in the presence of heavy capacitive and resistive loads. The output current of the line drivers is sensed and used in the low-voltage section of the system to perform the hybrid and loop supervision functions [8].

In a conventional SLIC, the power supply of the line drivers is usually controlled by a switching power modulator to adapt the line feed voltage according to the variable loop resistance. This method is less efficient in short loops where the loop resistance is insignificant. Instead, a simple power switch to select a high or low supply voltage can be used (in on-hook or off-hook conditions) for short-loop applications. A high supply voltage is usually used in on-hook condition when the loop has a high impedance and very small current. In off-hook mode the loop is terminated by the telephone set's impedance (600Ω

typical) and its voltage is dropped to limit the loop current. As a result, the supply voltage can be decreased by the power switch to reduce the power dissipation.

Historically, series feed resistors R_f were used in conventional SLICs to passively control the loop current as well as provide a suitable driving impedance for the loop [8]. Up to 300Ω feed resistors are typical for conventional loops, however, smaller resistances (20Ω to 100Ω) are required for short loops because of the lower line feed voltage and loop resistance.

2.3.1 Preamplifier Design

The main two functions of the preamplifier are

- adjusting the DC level of the loop signals and
- converting the single-ended low voltage transmit signal to a pair of amplified differential signals.

To clarify these functions, the loop signals are conceptually illustrated in Fig. 2.2. The voice information is provided by the codec and PCM interface circuits[8] in the form of a low voltage AC signal, shown as V_{ac} in Fig. 2.2 a. V_{ac} swings within the power supply range V_{dd} (typically a 5V supply) of the low voltage portion of the system. The signals on the loop consist of a DC and an AC component, illustrated in Fig. 2.2 b. The DC component V_{DC}, is used to feed power into the loop while the AC component carries the voice information. As a result, the voltage on each line (V_{TIP} and V_{RING}) includes a small AC signal V_{AC}, superimposed on a large DC level. Typical values are in the 1 to 2 V range for V_{AC} and 10 to 20 V for V_{DC} [9].

Since all signals are transmitted differentially over the loop, the AC components of V_{TIP} and V_{RING} must be 180° out of phase to inject a true differential signal into the loop. A fully-differential amplifier stage, similar to the one shown in Fig. 2.3 can be used to

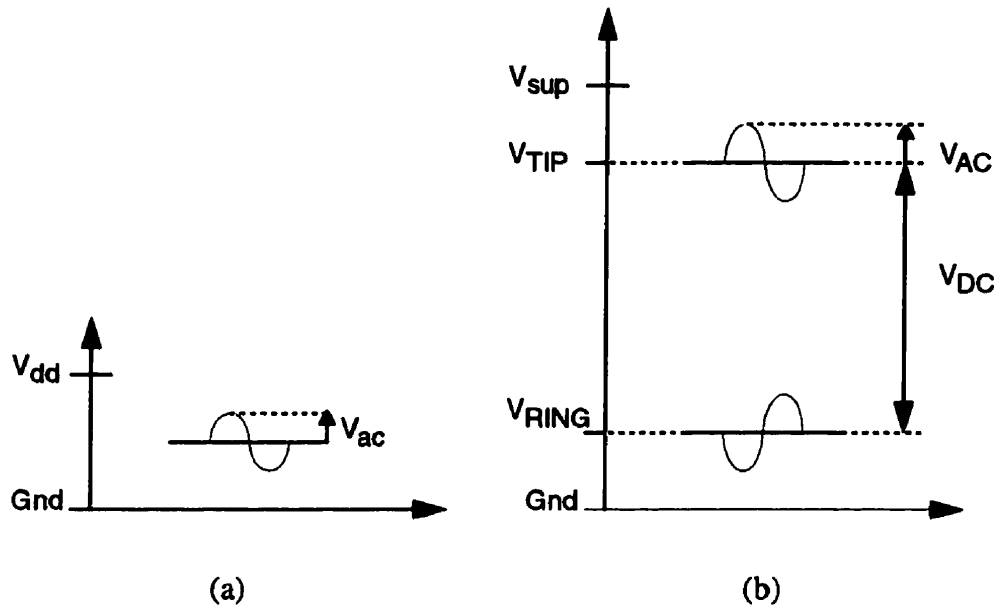

Fig. 2.2: Transmitting signal levels: a) low voltage signal from Codec b) loop signal

generate such signals. Using a differential opamp, the two inputs V_{ac} and V_{dc}, can be combined to generate the appropriate signal levels.

The differential output voltage V_{od} can be expressed as

$$V_{od} = \frac{R_f}{R_a} V_{ac} + \frac{R_f}{R_d} V_{dc} \tag{2.1}$$

where R_f, R_a and R_d are the feedback resistors around the differential amplifier shown in Fig. 2.3. This equation implies that the gain of the amplifier for each input source can be fixed separately using R_a and R_d. Therefore, the DC level and the AC amplitude of the output voltage can be adjusted independent from each other.

In order to realize the circuit of Fig. 2.3 , a high voltage differential opamp is needed. Major requirements of this opamp are minimum power dissipation and a bandwidth larger than that of the line drivers to avoid degrading the bandwidth of the whole SLIC system. A

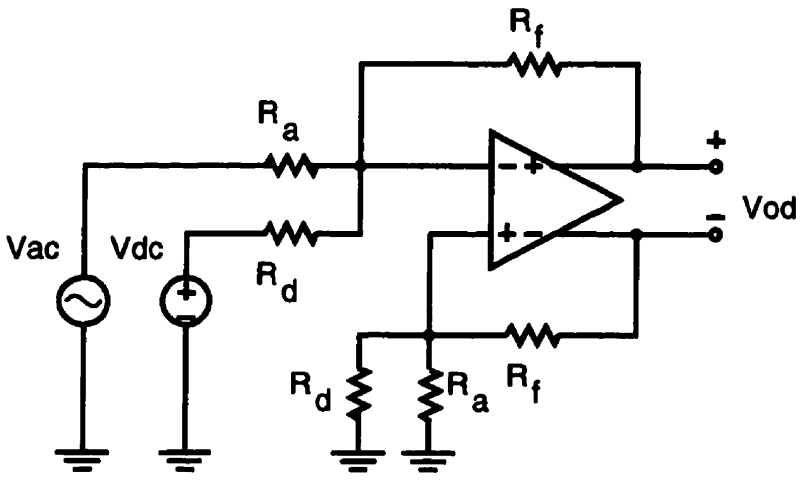

Fig. 2.3: A differential preamplifier structure

high current driving capability is not expected from the opamp as it must only drive the input stage of the line drivers.

Equation 2.1 deals with the differential part of the output voltage. The average or common-mode component of the output voltage is independent of the input voltages and must be fixed separately. Usually, a common-mode feedback circuit is used to control the common-mode level of the output.

2.3.2 Common-Mode Feedback Circuit

The common-mode output voltage of a differential amplifier may vary independently of the input signals over the whole supply voltage range, causing the output voltages to saturate at one of the supply rails. Therefore, it is necessary to control the common-mode level in a feedback loop.

The function of the CMFB loop is illustrated in Fig. 2.4. The CMFB circuit monitors the two output voltages of the differential amplifier and adds them up to measure their

average. The result is compared with a reference level V_{ref}, amplified and fed back to the differential amplifier (V_{ctrl}) to adjust the common-mode level of its outputs. When the loop is closed, the common-mode voltage of the differential amplifier outputs is equal to the reference voltage V_{ref}.

Traditionally, two types of CMFB circuits are used in low voltage applications: switched-capacitor and continuous types [10]. The switched-capacitor CMFB circuits[11], specifically designed for switched-mode applications, are not suitable for the SLIC application. Conventional continuous CMFB circuits, either use a source-coupled voltage comparators [12] or a resistive voltage adder [13] at the input. While the first approach has a limited input range, the second one requires impractically large resistors to be able to operate with high input voltages. Therefore, none of the available designs can be used for high voltage applications. A new high voltage CMFB circuit with wide input range is required for this system. The design and implementation of this circuit is discussed in Chapter 4.

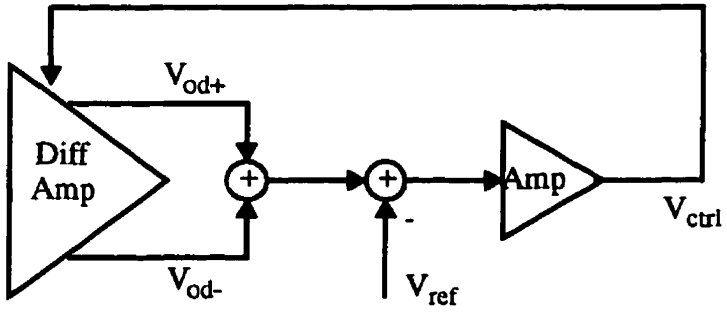

Fig. 2.4: Model of the CMFB loop

2.3.3 Line Drivers

Line drivers are the most important high voltage building blocks of a SLIC system. As the actual interface to the telephone lines, they play a key role in providing large loop currents and handling high voltage signals.

Line driver specifications are mainly dictated by the requirements for the short-loop SLIC. The nominal supply voltage for short-loop SLIC is 24V [9]. In addition to the high operating voltage, a large driving current (up to 30 mA) capability is also expected from the line drivers. Meanwhile, their idle power must be kept as low as possible, preferably less than 30mW. As a result, the sum of all the internal bias currents must not exceed 1mA assuming a maximum supply voltage of 30V [9].

Another important issue in line driver design is the stability of the circuit which must be guaranteed over a wide range of load impedances. Resistive loads down to 500Ω and capacitive loads up to 1nF may be expected at the output. In spite of such heavy loads, a unity-gain-bandwidth of more than 1MHz is required to increase the power supply rejection ratio at high frequencies and to satisfy digital subscriber line (ADSL) applications [14].

The line drivers must also have a very small output impedance. This feature is mainly required for longitudinal signal suppression [1]. Spurious noise and interference appear as longitudinal (or common-mode) signals on telephone lines. If the line driving circuits of the two lines are asymmetrical, common-mode signals can be converted to differential ones degrading the quality of transmission. This effect is characterized by longitudinal balance which is the ratio of the longitudinal to differential voltages at the output of the SLIC. This factor is a function of the matching between the driving impedances of the tip and ring terminals including the feed resistors and the output impedance of the line drivers as illustrated in Fig. 2.5. The induced noise on the twisted-pair wires is shown as a longitudinal signal source V_l. R_F is the feed resistance and r_o is the output impedance of the line driver.

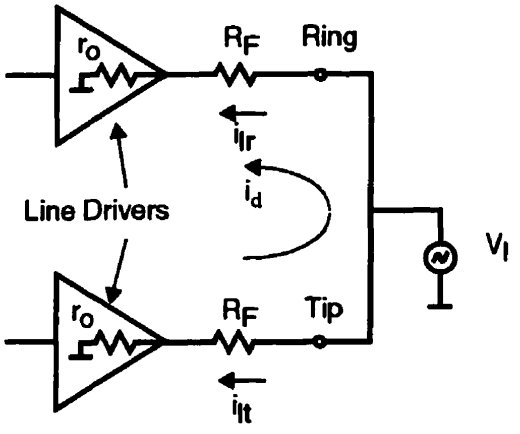

Fig. 2.5: Longitudinal balance model

In the ideal case when R_F and r_o on both lines are equal, the noise currents in the ring and tip lines are the same: $i_{lr} = i_{lt}$, hence canceling each other. However, if there is a mismatch $(\Delta R_F + \Delta r_o)$ between the total resistances of the tip and ring lines , then $i_{lr} \neq i_{lt}$ and a differential current $i_d = i_{lr} - i_{lt}$ will flow in the loop mixing with the actual voice signals. The longitudinal balance can be expressed as:

$$\frac{i_d}{i_{lr}} \cong \frac{\Delta R_F + \Delta r_o}{R_F + r_o} \tag{2.2}$$

The mismatch of the feed resistors ΔR_F , can be controlled by choosing accurate off-chip components. However, the output impedance of the line drivers may vary with operating currents, voltages and frequency. Therefore, it is not possible to maintain accurate matching for all the possible operating conditions. In order to eliminate the effect of line drivers mismatch Δr_o , their output impedance r_o must be less than the maximum allowable mismatch of the feed resistors ΔR_F . For example, a longitudinal balance of 60 dB translates into a maximum allowable mismatch of 0.1% between the feed resistors. As a result, with a typical 200Ω feed resistor, the output impedance of the line drivers must not exceed 0.2Ω .

Table 2.2: Major line driver specifications

Max. Supply Voltage	30V
Max. Line Current	30mA
Idle Power	< 30mW
Unity Gain Bandwidth	> 1MHz
Output resistance (@ DC)	< 0.2Ω
Load[15]	500Ω, 1nF

Due to lower noise and interference in a short subscriber loop, a 40 dB balance is sufficient for short loop applications [9]. However, because of lower driving voltage, the feed resistors are also smaller. With a minimum feed resistance of 20Ω, an output resistance of less than 0.2Ω is still desirable. Finally, the line driver must occupy minimum area to be easily integrable with a large amount of low voltage circuitry required for other short loop services. The main design specifications for the line driver are summarized in Table 2.2. These specification dictate the use of an efficient circuit topology for the output stage.

2.4 Summary

The specifications and characteristics of the short-loop SLIC system were discussed in this chapter. Based on the general requirements of the short-loop systems, an architecture for the high voltage front-end of the SLIC was presented. A minimum number of high voltage building blocks was used in this configuration to save both area and power. The resulting architecture is quite suitable for a single-chip implementation of a short-loop SLIC. The function and characteristics of each block were also described in this chapter. A detailed description of the implemented circuits will be presented in Chapter 4.

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CHAPTER 3

BiCMOS Compatible High Voltage Device Design

3.1 Introduction

The choice of a suitable technology is the key issue in the integration of a short-loop SLIC. Traditionally, high voltage bipolar processes were used to implement central office SLIC circuits[1-2]. Recent advances in power MOS devices has led to the development of BCD technologies which can implement Bipolar, CMOS and DMOS devices on the same chip [3-6]. However, being specifically designed for high voltage applications, such processes generally involve more complexity, less density and much higher costs as compared to VLSI CMOS or BiCMOS processes.

As mentioned in Chapter 1, the implementation of short-loop SLICs in future local access systems will require a high level of integration at minimum cost. Since the high voltage blocks only comprise a small part of the system (which includes a significant amount of high-performance, high-speed, low voltage circuitry), an advanced low voltage VLSI process with enhanced high voltage capabilities is more suitable for this application than a dedicated high voltage IC technology.

This thesis is the first attempt at implementing a short-loop SLIC using a submicron low voltage BiCMOS process. The high voltage capabilities of this process are provided by lateral extended-drain NMOS and PMOS transistors [7-9]. In this chapter, after a brief review of the two versions of the BiCMOS process (i.e. BATMOS-5 and BATMOS-10), the

structure and characteristics of the high voltage devices, implemented in this process, are discussed. Fabricated devices are characterized and a set of SPICE models are developed to facilitate the design of high voltage circuits.

3.2 BATMOS-5 Process

The BATMOS process used to implement the high voltage circuits in this thesis is a 0.8μm BiCMOS process available through Nortel [10]. The original BATMOS-5 is a 5 V process. By adding a few more masks and processing steps, another version of the process called BATMOS-10 was developed at Nortel [11]. This version of process was designed to provide 10V NMOS devices as well as PNP bipolar transistors. The features of BATMOS-10 process will be discussed in the next section.

The submicron CMOS devices in the BATMOS process are very attractive for high-density, low-power logic and control circuits, while the bipolar transistors are more suitable for high-gain, high-speed analog stages because of their high transconductance. In addition, the bipolar devices offer the best performance in high precision linear blocks such as current mirrors as a result of their superior matching.

Fig. 3.1 illustrates the flow of the BATMOS-5 process [13]. Starting with a p-type substrate, the thin buried layers are defined followed by the growth of a very lightly doped 1.3μm epi-layer. The buried layers are used to reduce the collector resistance of the bipolar devices as well as improve the latch-up immunity of CMOS circuits. Self-aligned n and p wells are formed next following by the growth of a thick field oxide for isolation. A n+ sinker implantation is performed at this stage to reduce the collector resistance of the bipolar transistors.

In the next step, a 175Å gate oxide is grown and a blanket threshold voltage adjustment implantation is carried out afterwards. The poly-silicon gates and poly-poly capacitors are

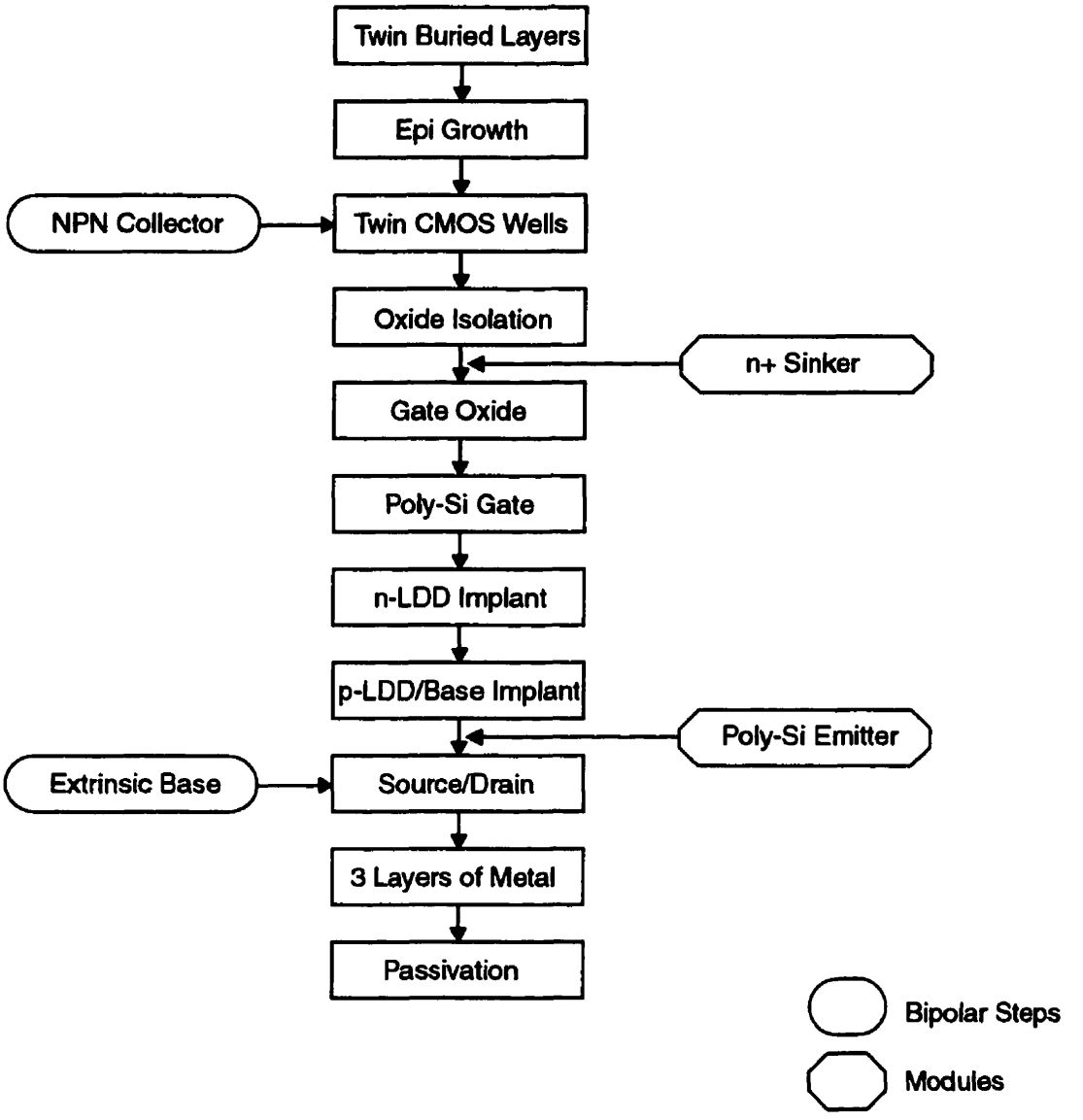


Fig. 3.1: BATMOS-5 process flow

then formed followed by the low doped drain (LDD) implantations. The LDD regions are used in the CMOS devices to suppress the hot carrier effects. The poly-silicon emitter of the bipolar devices is created in the next step. The source and drain regions of CMOS components are formed along with the extrinsic base of the bipolar devices. The process is completed with three levels of metallization and passivation.

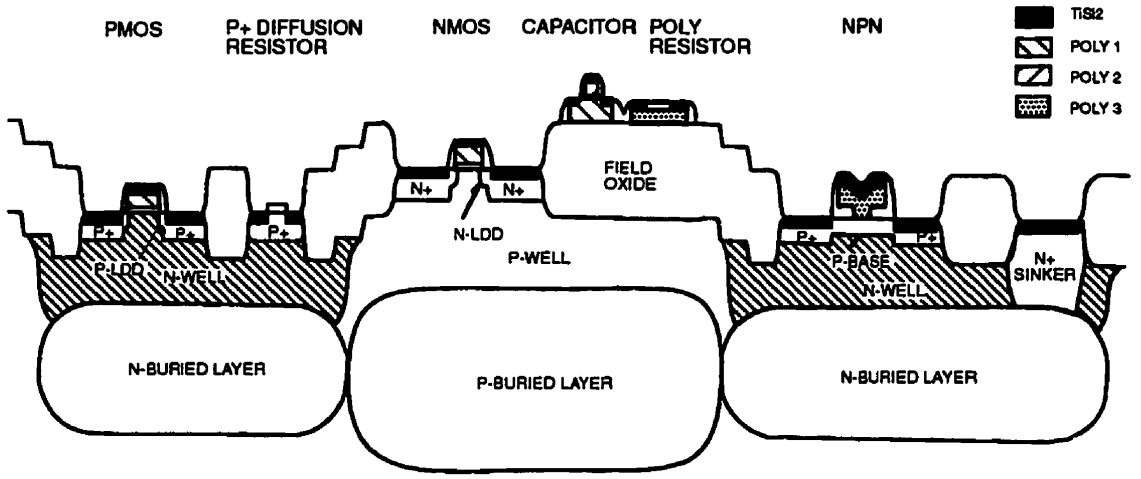


Fig. 3.2: Cross section of the BiCMOS process [10]

A cross section of the BATMOS-5 process is illustrated in Fig. 3.2. The thin epi-layer is used to obtain a high speed vertical NPN transistor. However, it severely limits the ability to implement high voltage structures in this process. The breakdown voltage of the CMOS devices is limited to 7V and that of the bipolar transistors to 8V. The bipolar transistors have a peak cutoff frequency of 12 GHz with a minimum emitter area of 0.8x4 μm^2. The 0.8μm CMOS components have good immunity to hot carrier injection effects and latch-up through the use of low-doped drain (LDD) structures and buried layers respectively.

This process also provides poly-silicon resistors with sheet resistances of 30 and 750 Ω/sq and high power 120Ω/sq diffusion resistors useful for high current densities. The high quality poly-poly capacitors offer a large capacitance per unit area (1.15 $fF/\mu m^2$). However, the voltage across them must not exceed the 5 V limit. Therefore they cannot be used in high voltage applications. Table 3.1 summarizes the available devices in this process.

Table 3.1: Available devices in the 0.8μm BiCMOS

Device	Parameter	
CMOS	L_{eff}	0.66 μm
	V_t	0.8 V
	BV	7 V
Bipolar	Emitter Area	4x0.8 μ^2
	f_t	12 GHz
	BV_{ceo}	8 V
Capacitor	C_{p-p}	1.15 fF/μm^2
	BV	5 V
Resistors	Rpoly	750 Ω/sq
	LRpoly	30 Ω/sq
	Rdiff	120 Ω/sq

3.3 BATMOS-10 Process

Modularity is one of the key features of the BATMOS process which allows the selection of optional modules without any impact on the remainder of the process. The BATMOS-10 version is a result of adding such modules to the original BATMOS-5 process. The extra modules have been developed by Nortel [11] with design support from the University of Toronto to provide two additional layers namely n-subwell and high voltage (HV) n-well.

The useful feature of BATMOS-10 process is the implementation of a n-subwell layer. The n-subwell is an extra n-type layer, located underneath the buried layers. This is implemented by using an additional mask and a diffusion step at the very beginning of the process (i.e., before the definition of the buried layers) as shown in Fig. 3.3 . Therefore, it

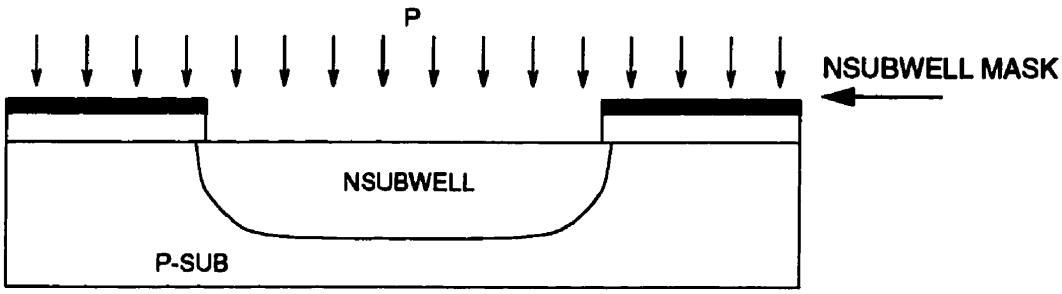


Fig. 3.3: NSUBWELL processing step

has no effect on the buried layers or well regions leaving the performance of the low voltage components intact.

The main use of the n-subwell is to isolate the p-well region from the p-substrate. This allows the body of the NMOS devices to be disconnected from ground, eliminating the body effect in high-side configurations. An isolated p-well can also be used as the collector of a vertical PNP transistor. In fact, using additional n-base and p-emitter processing modules, a high quality vertical PNP device has been developed at Nortel with its cross section illustrated in Fig. 3.4. The availability of complementary bipolar devices offers great advantages in designing analog circuits with this process.

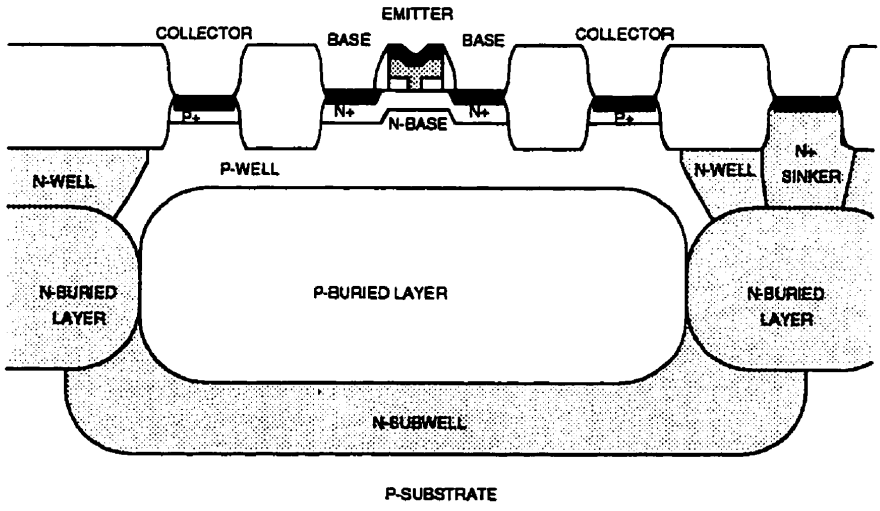


Fig. 3.4: Structure of PNP transistor in the 10V BiCMOS process

The HV n-well is similar to the n-well with a much lower doping concentration. It has been designed for implementing NMOS devices with a breakdown voltage of 10 V. While the HV n-well must be implemented together with the n-well, it must not affect the characteristics of other layers including the n-well itself. Therefore, an extra mask (M_HVNWELL) and ion-implantation step is used with a much lower implant dose as shown in Fig. 3.5.

The n-well regions are implemented using two separate implantation steps. After opening windows in the oxide for both the n-well and HV n-well using the n-well mask (M_NWELL), a low dose ion-implantation is performed. In the second step, a high dose implant is used to create the n-well. However, this implant is blocked over the HV n-well areas by the HV n-well mask (M_HVNWELL). In this way, a very low doped HV n-well can be implemented together with the n-well without affecting it's characteristics.

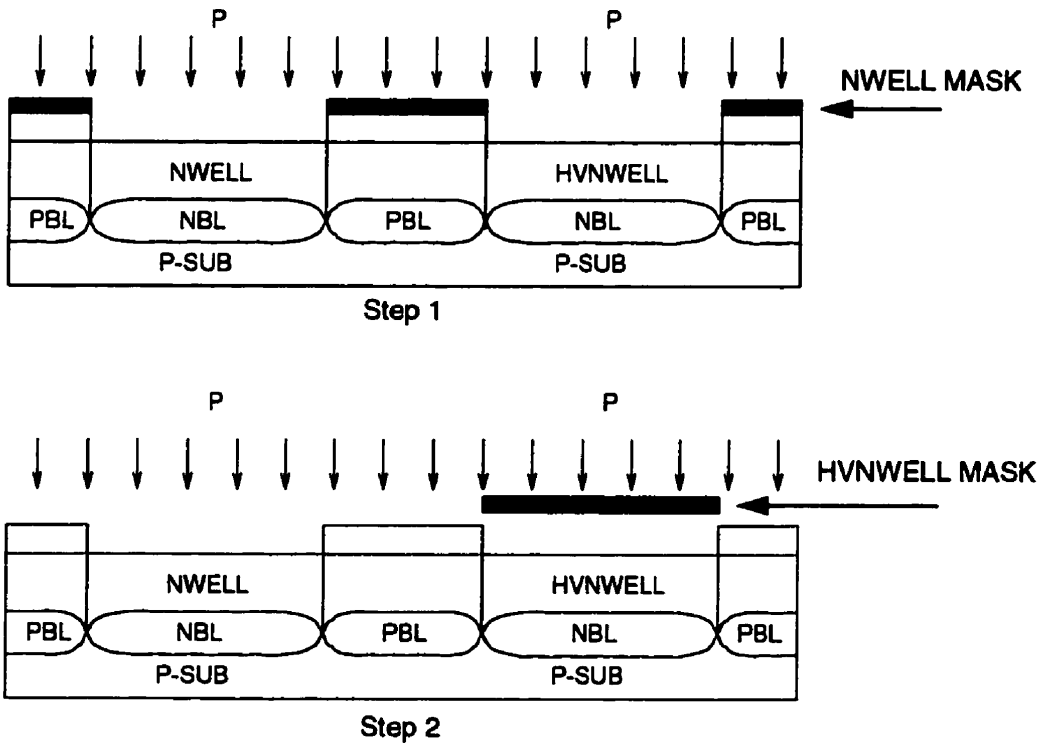


Fig. 3.5: Processing steps for implementing both n-well and HVn-well

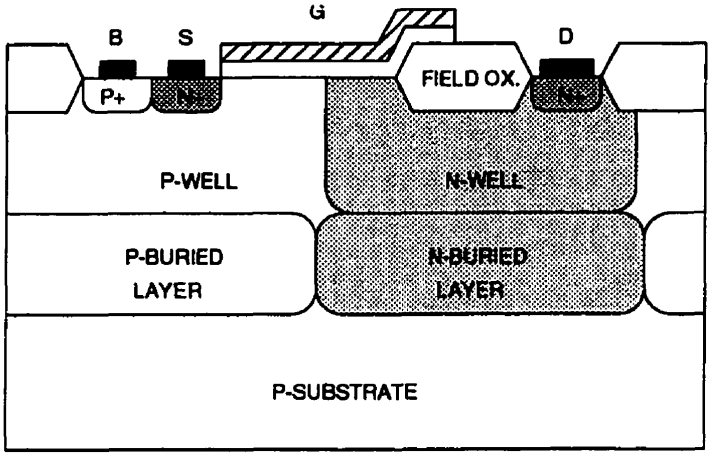
3.4 High Voltage Device Structures

To integrate high voltage circuits into a low-voltage submicron process, suitable high voltage device structures are required. These structures must be completely compatible with the process such that their implementation does not degrade the performance of the low voltage components or increase the complexity of the process.

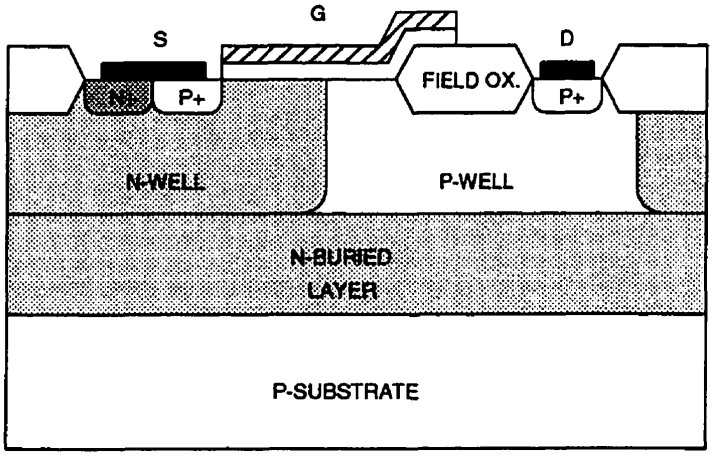
Due to the thin epitaxial layer, lateral high voltage structures are more suitable for a VLSI process. Among such structures, lateral high voltage MOSFETs are very common because of their simple structure and high performance. The main difference between a low voltage and a high voltage MOS transistor is the existence of a large low-doped drift region at the drain side of the high voltage device. This region serves to reduce the electric field at the drain-gate interface by allowing the depletion layer to extend into it, resulting in higher breakdown voltages.

Fig. 3.6 shows the high voltage NMOS and PMOS devices developed for the BATMOS-5 process [7]. For both transistors, the highly doped drain contact regions are separated from the channel by a lightly doped drift region. In this process, the n-well serves as the drift region for the NMOS device, while the p-well acts as the drift region for the PMOS transistor. The structure of these devices is similar to that of low voltage transistors at the source side. Therefore, their gates are self-aligned with respect to their sources. However, at the drain side, the gate overlaps the drift region to spread the depletion layer at the silicon surface, reducing the electric field.

In this process, the n-buried layer mask is usually generated from the n-well mask resulting in self-aligned buried layers underneath the well regions as shown in Fig. 3.6 a. However, for the PMOS transistor (Fig. 3.6 b), only the n-buried layer is used all underneath the device to isolate the p-well drain region from the substrate. This can be accomplished by modifying the n-buried layer mask layout manually.



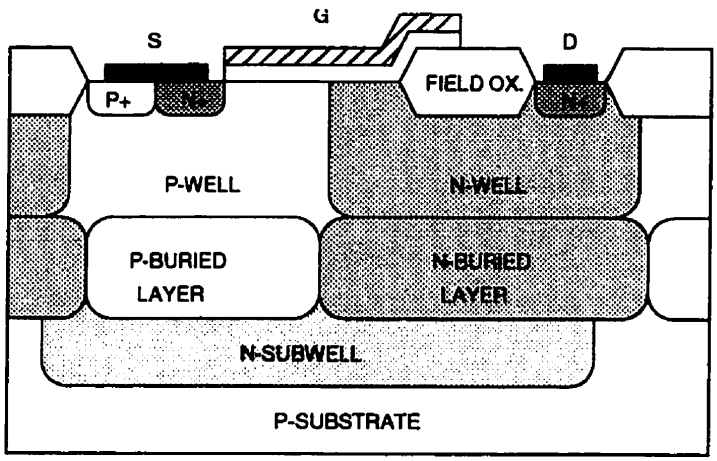
(a)



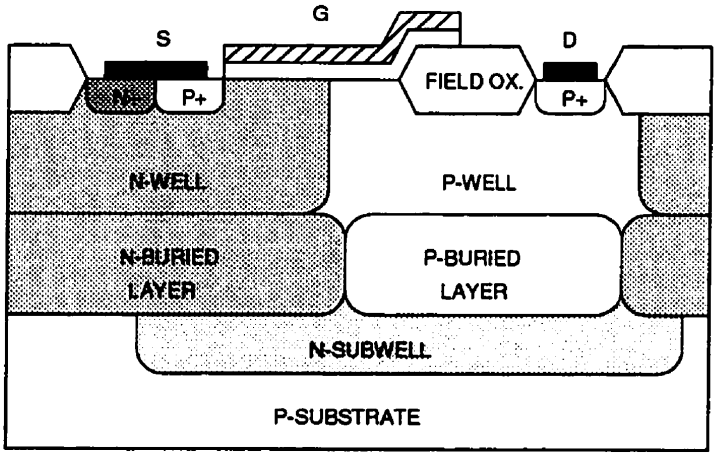
(b)

Fig. 3.6: Cross-section of: a) a high voltage NMOS and b) a high voltage PMOS in BATMOS-5

Because the high voltage PMOS device is implemented in an n-well region, its body is isolated from the substrate. As a result, it can be used at high-side configurations with the source and bulk terminals connected together and hence, no body effect. However, the p-well body of the high voltage NMOS device is connected to the p-substrate. Since, the source structure of the high voltage NMOS is similar to that of the low voltage device, the breakdown voltage on the source terminal is no larger than 7 V. This limits the use of the device as a source-follower or high-side driver where large source voltages are applied.



(a)



(b)

Fig. 3.7: Cross-section of: a) a high voltage NMOS and b) a high voltage PMOS in BATMOS-10

The existence of the n-subwell layer in BATMOS-10, facilitates the isolation of the high voltage devices. This layer can be used instead of the n-buried layer to isolate a p-well region which can serve as the drain of a PMOS or the body of a NMOS device. A cross-section of the high voltage devices in BATMOS-10 process is shown in Fig. 3.7. Both NMOS and PMOS devices in this process are isolated from the substrate allowing them to operate in high-side configurations.

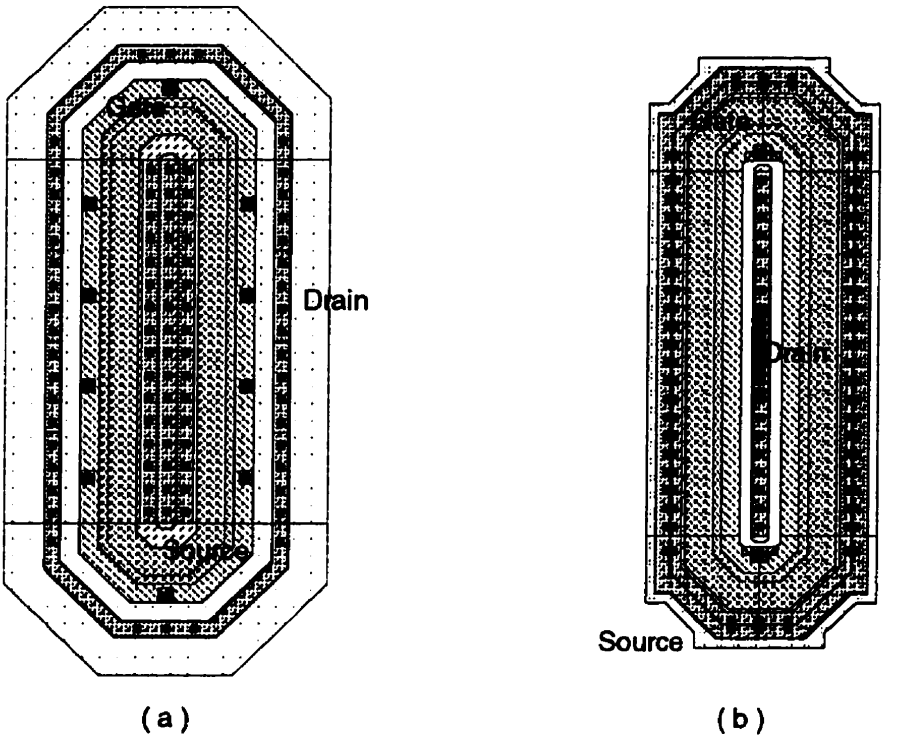


Fig. 3.8: Layouts of the high voltage transistors in BATMOS-5: a) NMOS and b) PMOS

3.5 Experimental Device Characterization and Modeling

Fig. 3.8 and Fig. 3.9 illustrate layouts and micrographs of the high voltage devices fabricated in BATMOS-5 technology. Similar devices were also fabricated in BATMOS-10 process with identical layouts. The devices are implemented with octagonal shapes to avoid possible breakdown voltage degradation due to the sharp corners. A channel length of 3μm was chosen for all the high voltage devices to prevent channel punch-through effect [12]. Using long channel lengths also minimizes the effects of process variations on device parameters which may be caused by a non-self-aligned channel at the drain side. Other device dimensions, generally follow the optimized structure proposed by Li [12].

In order to design high voltage circuits, the development of a set of electrical models which fully characterizes the high voltage devices is crucial. A set of SPICE models for low

(a) (b)

Fig. 3.9: Micrographs of the high voltage transistors in BATMOS-5: a) NMOS and b) PMOS

voltage components in the BATMOS process has already been developed [13]. By developing similar models for the high voltage devices, both low and high voltage sections of the circuit can be simulated simultaneously, greatly simplifying the design process. For this reason, a number of high voltage test devices were fabricated and characterized.

The measured I-V characteristics of high voltage NMOS and PMOS transistors in BATMOS-5 are shown in Fig. 3.10 and Fig. 3.11, respectively. The breakdown voltage of the high voltage NMOS device is 33V while the PMOS device has a breakdown voltage of 40V. In BATMOS-10 process, NMOS and PMOS devices exhibit a breakdown voltage of 34 V and 48 V, respectively. As Fig. 3.10 illustrates, the breakdown voltage of NMOS transistor is reduced at gate voltages greater than zero. Although this effect would not cause any problem in switching applications where the device operates either in cut-off or in the triode region, it becomes important in amplifier configurations where a constant saturation current is required.

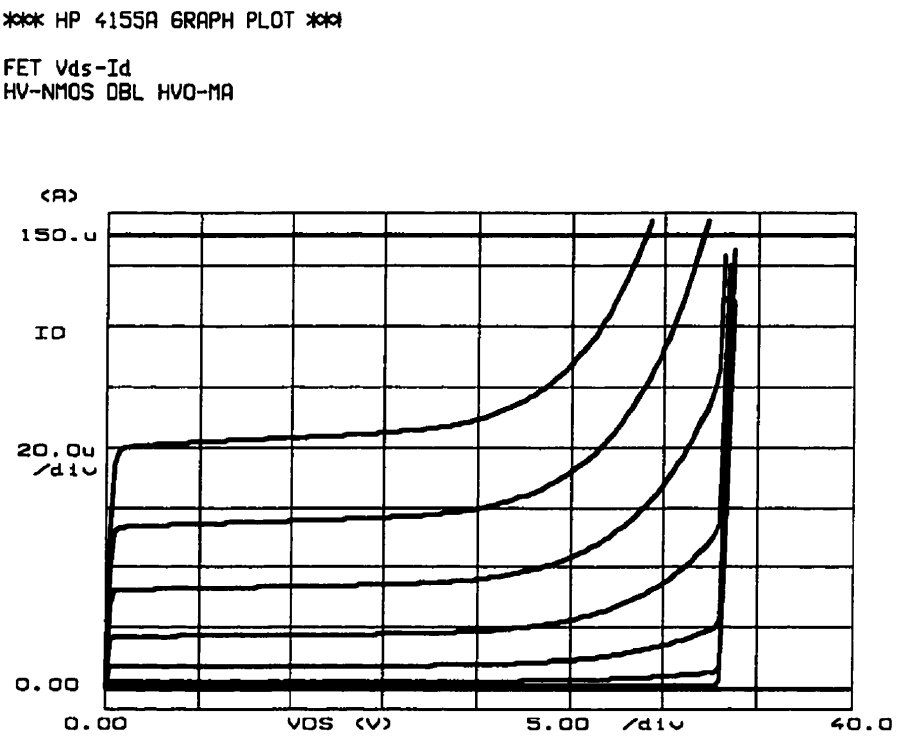


Fig. 3.10: Measured I-V characteristics of the high voltage NMOS transistor in BATMOS-5 (W/L=10/3, Drift region length=4.2μm)

The increase in the saturation current of the high voltage NMOS transistors is the result of impact ionization of the silicon lattice caused by hot electrons[14]. At high gate voltages, the current increases significantly in a localized area, resulting in a large current density. As a result, the number of electron-hole pairs generated by impact ionization multiplies, starting a weak avalanche breakdown. Moreover, the generated holes flow into the substrate and forward bias the source-substrate junction, turning on the parasitic NPN bipolar transistor (drain-substrate-source) in parallel with the NMOS device. This weak avalanche breakdown is not observed in PMOS devices because of the much lower ionization rate of holes as compared to electrons.

In order to avoid hot carrier effects, the high voltage NMOS transistors must be operated at low gate voltages and low current densities. Therefore, oversized devices must be used to handle moderate currents. Also substrate contacts must be placed as close as

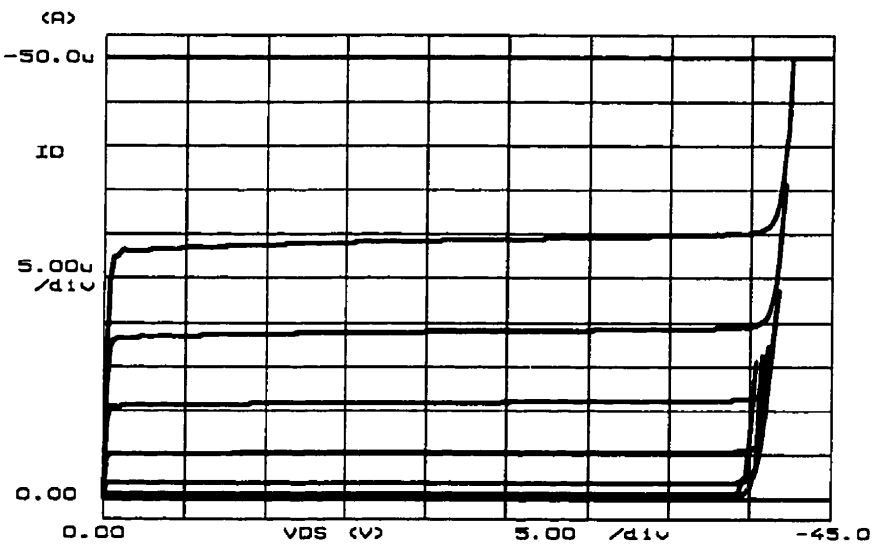


Fig. 3.11: Measured I-V characteristics of the high voltage PMOS transistor in BATMOS-5 (W/L=10/3, Drift region length=4.2μm)

possible to the source terminal to reduce the base resistance of the parasitic bipolar transistors, increasing the minimum base current required to turn them on. Other techniques have also been proposed which mainly require some modifications in the process and hence, are not attractive [15].

A conventional MOSFET with a series drain resistor was used to model the high voltage transistors as shown in Fig. 3.12. The MOSFET M1 models the channel underneath the gate electrode, while the resistor R_D is used to model the extended drain region[1].

The extraction of model parameter were performed in three separate steps for R_D, drain current (I_D) parameters and the parasitic capacitances of M1. These parameters are shown in Fig. 3.13. In the first two steps, the DC I-V characteristics of the high voltage devices

1. In some double-diffused high voltage MOS transistors [16], JFETs, rather than resistors are used to model the modulation of current in the drift region by the substrate voltage. However, due to the existence of the buried layers, the back-gate effect of the substrate on the drift region is negligible in this process. Therefore, there is no advantage in using JFET instead of resistor in the model in terms of accuracy.

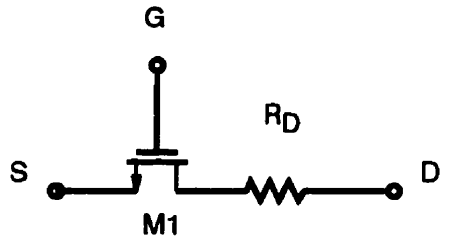


Fig. 3.12: Circuit models for the extended-drain high voltage devices

were used to extract R_D and the current parameters of M1. Using an iterative optimization process, the extracted parameters in each step were tuned to fit the measured results to the values predicted by the model. In the third step, the parasitic capacitances of M1 were extracted from the device structure.

In order to extract R_D , the drain current I_D , must be measured at low drain voltages when M1 is in the triode region. Under these conditions, the drain current is given by

$$I_D = \frac{V_{DS}}{R_D + R_{DS}} \cong \frac{V_{DS}}{R_D} \tag{3.3}$$

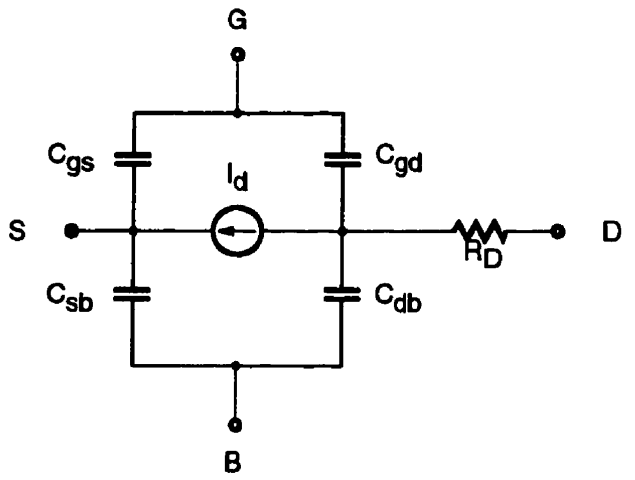


Fig. 3.13: Simplified model structure used for parameter extraction

where R_{DS} is the small drain-source resistance of M1 in the triode region. Assuming $R_{DS}<<R_D$, R_D can be extracted using equation 3.3. This value can then be used as an initial guess in an optimization program[1] to find the best fit to the I-V characteristics in the linear part of the curves (where V_{DS} is small).

In the second step, the drain current of transistor M1 was modeled using the level 3 MOSFET model in SPICE. This model incorporates an empirical set of equations for the drain current with several fitting parameters [18]. Because the high voltage device structures are similar to low voltage transistors in the channel and source regions, many of the low voltage device parameters can be applied to the high voltage devices. However, other parameters must be specifically extracted for the high voltage transistors by optimization. These parameters include VTO and ETA for threshold voltage adjustment, VMAX and KAPPA for drift velocity saturation and THETA for mobility degradation [18]. In order to eliminate the effect of R_D in this extraction step, the I-V data points in the saturation region (i.e. horizontal parts of the I-V curves) were used for curve fitting. In this region where the drain voltage is high, I_D is mainly determined by M1 regardless of the drain resistance R_D.

For NMOS devices, the impact ionization parameters such as ALPHA and VCR [18] were also extracted using the weak breakdown region of the I-V characteristics (i.e. the bent section of the curves in Fig. 3.10). A complete list of the extracted parameters for both BATMOS-5 and BATMOS-10 devices are provided in Appendix A.

Fig. 3.14 and Fig. 3.15 show the measured and simulated I-V characteristics of the high voltage NMOS and PMOS devices, respectively. All the extracted model parameters were iteratively optimized to best fit the measured characteristics. The simulated characteristics using the extracted models are in good agreement (less than 5%) with the experimental results.

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1. The HSPICE optimization tool was used for parameter extraction[17].

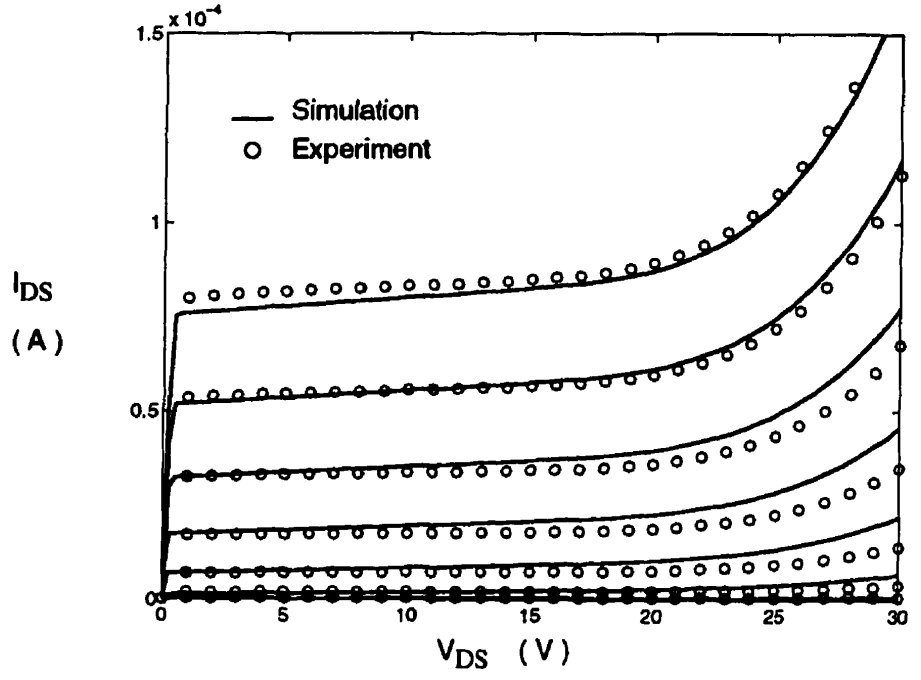

Fig. 3.14: Experimental and simulated I-V characteristics of the high voltage NMOS in BATMOS-5 (W/L=10/3, Drift region length=4.2μm, R_D=0.94kΩ)

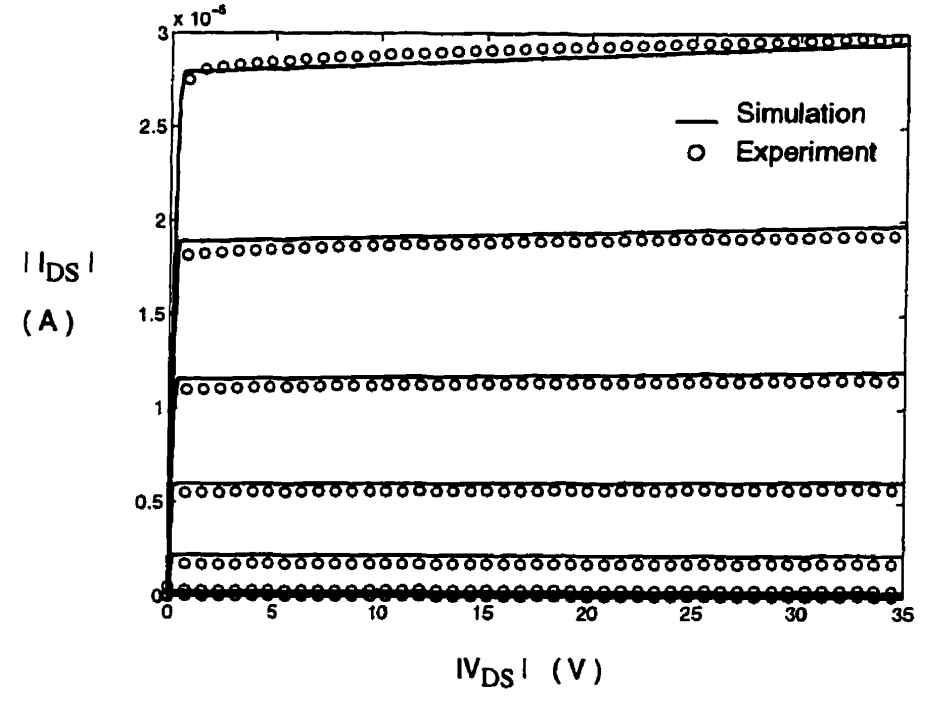

Fig. 3.15: Experimental and simulated I-V characteristics of the high voltage PMOS in BATMOS-5 (W/L=10/3, Drift region length=4.2μm, R_D=12.4kΩ)

The final step of modeling process involves the extraction of the parasitic capacitances associated with the devices. These capacitances are included in the SPICE model as shown in Fig. 3.13. C_{gd} and C_{gs} are the gate-drain and gate-source overlap capacitors and C_{sb} and C_{db} are the source-bulk and drain-bulk junction capacitors.

The parasitic capacitances of a high voltage device is shown in Fig. 3.16. Three of the four parasitic capacitances can be directly extracted from the available low voltage devices models[13]. The gate-source overlap capacitance C_{gs} and the source-bulk capacitance C_{sb} of the high voltage device are the same as those of the low voltage MOSFET because of the similar source structure. Therefore, the same parameter values in the low voltage device models can be used for these capacitances. As can be seen from Fig. 3.2, the n-well drain of the high voltage device is very similar to the collector region of a low voltage NPN transistor. Consequently, the parasitic drain-bulk capacitance C_{db} must also be equal to the collector-substrate capacitance C_{cs} of the NPN transistor.

The only specific parasitic capacitance of the high voltage devices is the gate-drain overlap C_{gd} capacitance. This capacitance is of great importance for two reasons:

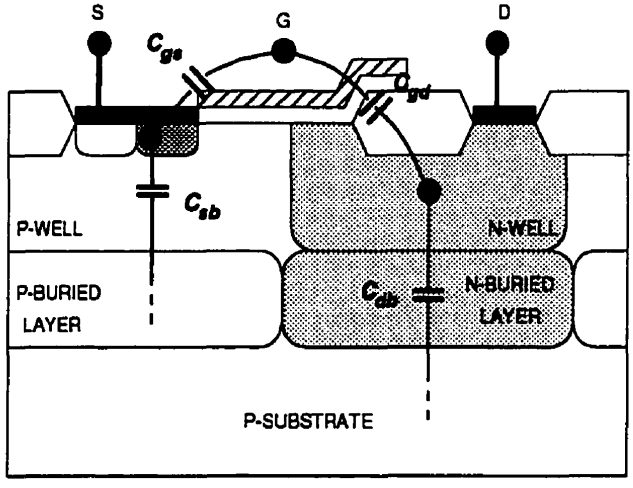

Fig. 3.16: Modeling of the parasitic capacitances of the high voltage device

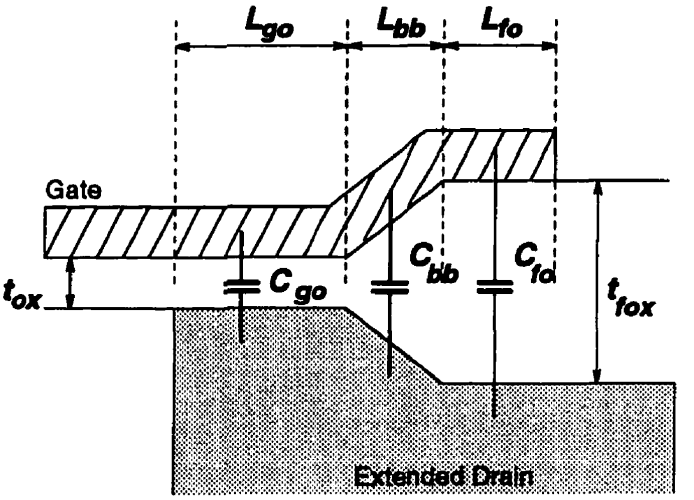

Fig. 3.17: Model of the gate-drain capacitance of the high voltage device

- its value is much larger than other parasitics due to the thin gate oxide at the overlap area, and
- it acts as a Miller capacitance in amplifier configurations.

The value of C_{gd} (per unit channel width) can be calculated by dividing the overlap region into three different sections: gate oxide (C_{go}), bird's beak (C_{bb}) and field oxide (C_{fo}) as shown in Fig. 3.17

$$C_{gd} = C_{go} + C_{bb} + C_{fo} \tag{3.4}$$

Based on the geometrical structures of C_{go}, C_{bb} and C_{fo}, equation 3.4 can be expressed as

$$C_{gd} = L_{go}\frac{\varepsilon_{ox}}{t_{ox}} + L_{bb}\frac{\varepsilon_{ox}}{t_{fox} - t_{ox}} ln\left(\frac{t_{fox}}{t_{ox}}\right) + L_{fo}\frac{\varepsilon_{ox}}{t_{fox}} \tag{3.5}$$

This equation can be used to find the gate-drain overlap capacitance. In order to verify the calculations, the gate-drain overlap capacitance of a large high voltage NMOS

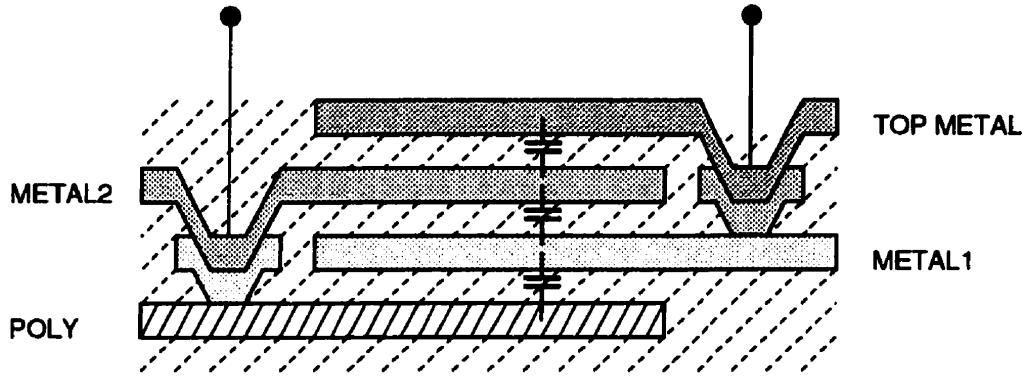

Fig. 3.18: Structure of the high voltage capacitor

(2100μm/1μm) was measured using HP4280 capacitance meter. The measured and calculated values were within 10% of each other. Using the capacitance parameters, the SPICE models were completed and used for simulating the high voltage circuits.

3.6 Other Components

Besides the high voltage NMOS and PMOS devices, other components such as resistors and capacitors are also required in the design of high voltage circuits. Therefore, the voltage handling capabilities of such components must be investigated in the low voltage BiCMOS process.

Poly-silicon resistors are implemented over the thick field oxide which provides good isolation from the silicon surface. As a result, they are able to handle the high voltages necessary for SLIC applications (>30V).

The poly-poly capacitors are not able to withstand more than 5V across their terminals due to the very thin dielectric layer. In order to overcome this problem, capacitors with thicker dielectrics must be used[11]. As shown in Fig. 3.18, using the three metal layers and

a poly-silicon layer, stacked on top of each other, a high voltage capacitor can be implemented. This technique increases the breakdown voltage of the capacitor to more than 100V. The average dielectric thickness between the metal layers is 20 times that of the poly-poly capacitor resulting in a 20 times increase in area. However, by stacking three such capacitor on top of each other, the area is reduced by a factor of 3. As a result, the overall area is increased by only 6 times rather than by 20.

3.7 Summary

In this chapter, the high voltage capabilities of Nortel's BiCMOS process were investigated. The high voltage MOS transistor structures that were used to implement the SLIC building blocks were introduced. These lateral devices use the p-well and n-well regions as the extended drain to provide high breakdown voltages. The devices are implemented by appropriate layout modifications without any changes in the process. As a result, they retain full compatibility with the low voltage components.

In order to facilitate the design of the high voltage circuits, the fabricated high voltage MOS devices were characterized and a set of SPICE models were developed. These models are based on the level 3 MOSFET model in SPICE with the drift region modeled as a large drain resistor. The model parameters were optimized to fit the I-V characteristics of the transistors.

The parasitic capacitances of the high voltage devices were also modeled to allow the frequency analysis and transient simulation of the high voltage circuits. Finally, High voltage capacitors were also implemented using inter-layer parasitic capacitances.

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CHAPTER 4

High Voltage Circuit Design

4.1 Introduction

After developing and characterizing the high voltage devices as described in the previous Chapter, the short loop SLIC architecture, proposed in Chapter 2 was realized. However, designing high voltage circuits in a low voltage process is not a trivial task. Because of their limited breakdown voltage, the high performance low voltage components such as bipolar transistors cannot be used in critical portions of the circuits (such as output stages). The protection against high voltage spikes must be carefully considered. Even the available high voltage PMOS and NMOS devices face certain limitations such as restricted gate and source voltage, substrate isolation, weak avalanche breakdown and large parasitics. These design constraints are aggravated by limited area and power budget in addition to other specific requirements such as bandwidth.

In this chapter, the design process of each block of the system is described in detail. The circuits include the preamplifier, the common-mode feedback circuit, the power switch, and line drivers. Substantial attention is paid to the line driver because of its critical role in the system as well as challenging requirements. As a result, three different designs for this block are presented as optimized for specific processes. The experimental results for the complete SLIC front-end are also included in this Chapter.

4.2 Preamplifier Design

The schematic diagram of the differential preamplifier is illustrated in Fig. 4.1. A symmetrical OTA configuration is used in this design [1]. The advantages of an OTA structure include wide bandwidth and small power dissipation. In addition, an OTA is easily compensated by the load capacitance at its outputs. This feature allows the use of parasitic capacitances at the input of the following stage (i.e. the line drivers) to compensate the OTA, saving additional compensation capacitors. Also, as will be explained shortly, the common-mode voltage at the output can be easily controlled using the output current sources.

The input stage of this opamp is implemented using high voltage PMOS transistors (M1,M2) to withstand large input swings. Low voltage transistors rather than high voltage devices are then used in the current mirrors (M3-M6) to achieve better matching and frequency response. However, they are protected against high voltage swings using cascode high voltage devices (M7,M8,M11,M12). The gain of the opamp is also increased as a result of the cascode configuration.

In order to provide adequate output current, the low-side current mirrors M3-M6 use a 1:3 ratio to scale up the current as well as the gain. A cascode current source M13-M16 is used to provide the bias current of the input stage. This current source also generates the bias voltage for the high-side cascode transistors M7 and M8.

The common-mode voltage of the output stage is adjusted by the current sources M9 and M10. A control voltage V_{cntrl}, produced by a common-mode feedback circuit, keeps the current in M9 and M10 equal to that of the lower current mirrors M5 and M6. In this way, the average of the two output voltages remains at a reference level in the middle of the power supply range.

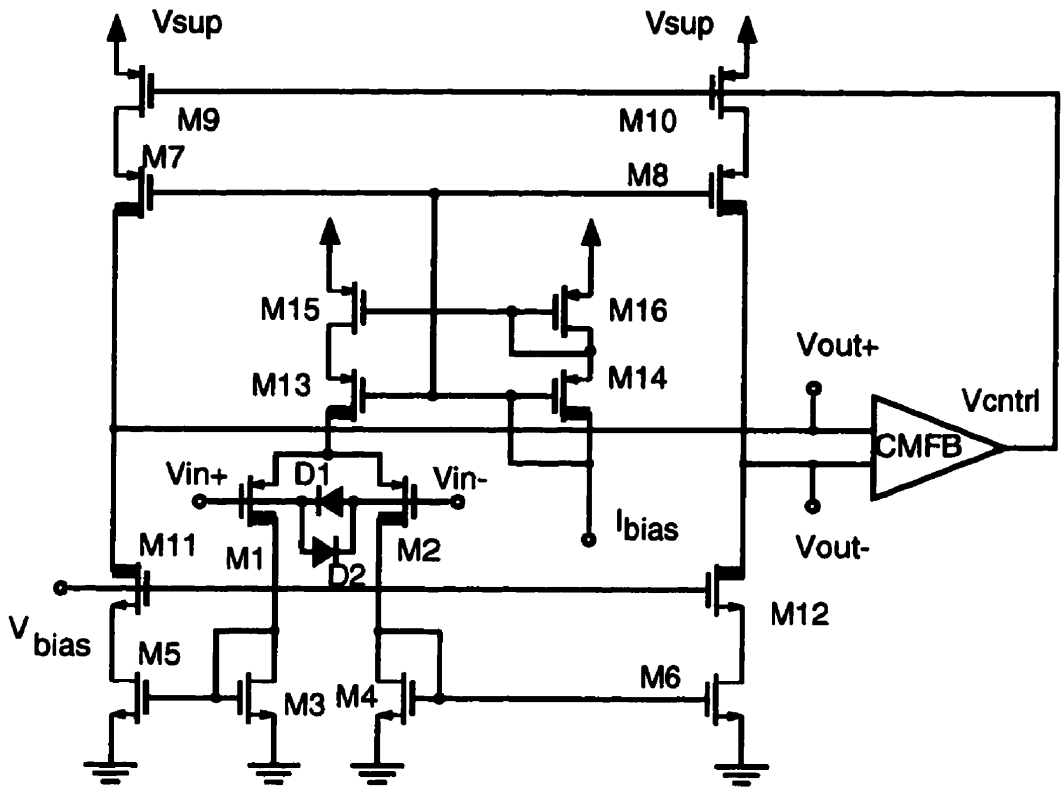


Fig. 4.1: Schematic diagram of the differential opamp

Table 4.1: Device parameters of the differential opamp

Device		Parameter[1]
Low Voltage MOS	M3,M4	5μ/1.2μ
	M5,M6	15μ/1.2μ
	M7-M10	30μ/1.2μ
High Voltage MOS	M1,M2,M11-M16	84μ/3μ

1. Aspect ratio for MOS device, emitter area for bipolars

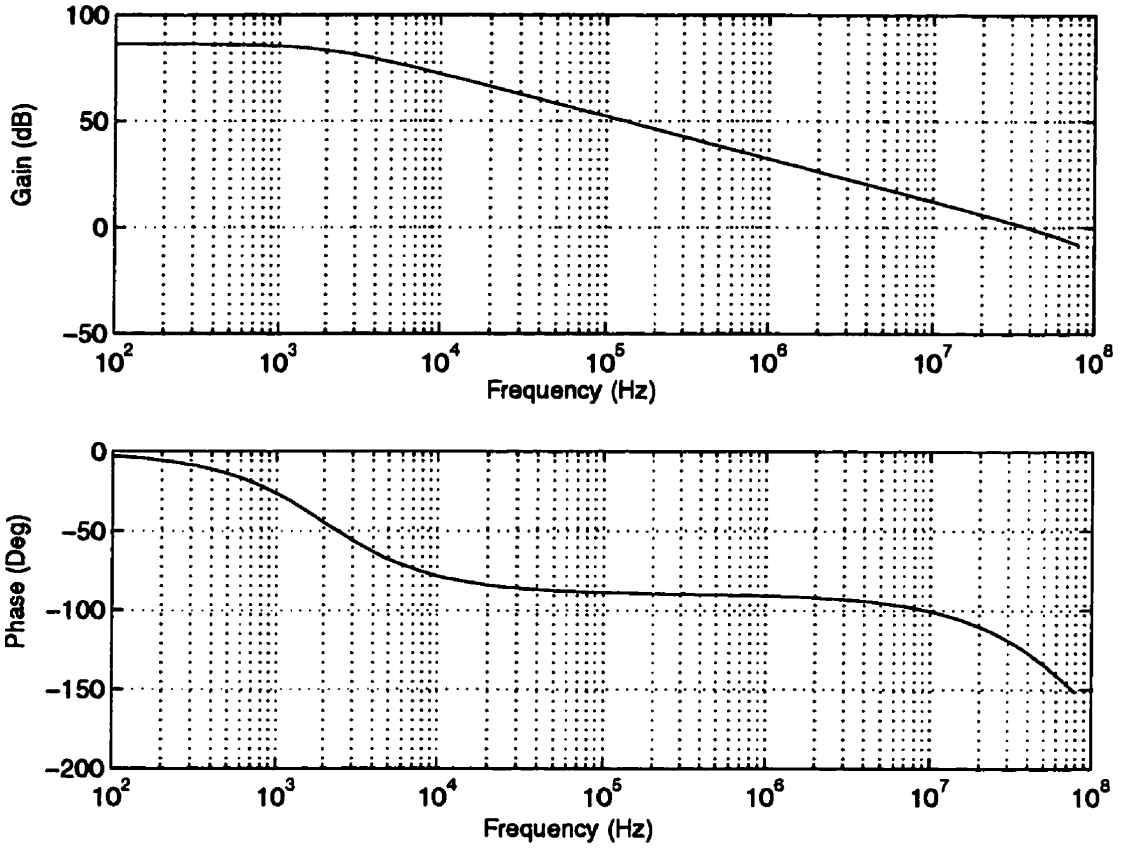


Fig. 4.2: Frequency response of the differential opamp

The frequency response of the amplifier with 1pF load capacitance is shown in Fig. 4.2. The differential DC gain is more than 86 dB with a unity-gain bandwidth of 35MHz and more than 50° phase margin. The unity-gain bandwidth of the amplifier is determined as $w_u = g_m/C_l$ where g_m is the transconductance of the input stage and C_l is the load capacitance. Larger load capacitances contribute to stability by decreasing the bandwidth without moving the higher order poles. Therefore, greater phase margins will be achieved with larger capacitive loads. The bandwidth penalty is not important as the SLIC bandwidth is limited by the line drivers.

4.2.1 Common-Mode Feedback Circuit

Fig. 4.3 shows the schematic diagram of CMFB circuit, designed for high voltage applications. The objective of this design was to provide a large input voltage range with minimum area and power dissipation. The design is based on the idea of using the output resistance of the high voltage PMOS devices (M15-M17) instead of large resistors. In this circuit, two source-follower buffers M1 and M2, apply the input voltages, V_{out+} and V_{out-} to the current sources M16 and M17. Because of the output resistance of M16 and M17, the currents in M1 and M2 change proportional to the input voltages. These currents are then added in node A and are compared to a reference current in the lower current mirrors M4-M9. The reference current is generated from a reference voltage V_{ref}, using a replica stage composed of M3 and M15. These devices were chosen twice as large as those in the input stages (M1,M17 or M2,M16) to match the current in M3 to the sum of currents in M1 and M2. A low voltage cascode current mirror, M4-M9, reflect the reference current back into node A. When $V_{out+} = V_{out-} = V_{ref}$

$$I_{M1} + I_{M2} = I_{M3} = I_{ref} \tag{4.1}$$

Therefore, the voltage on node A is equal to that on the drain of M6. However, if the average of V_{out+} and V_{out-} is not equal to V_{ref},

$$(I_{M1} + I_{M2}) \neq I_{M3} = I_{ref} \tag{4.2}$$

As a result, V_A start to change, modulating the current in the current source M10. This current passes through M18 to adjust the control voltage V_{cntrl} that is fed back to the differential amplifier. The bias current of the output stage of the differential amplifier (Fig. 4.1) would then change with V_{cntrl} to bring the common-mode level back to V_{ref}.

It is necessary for all the current mirrors in this circuit to be matched when the input voltages are equal to V_{ref}. Therefore, the voltage across all the current sources must be

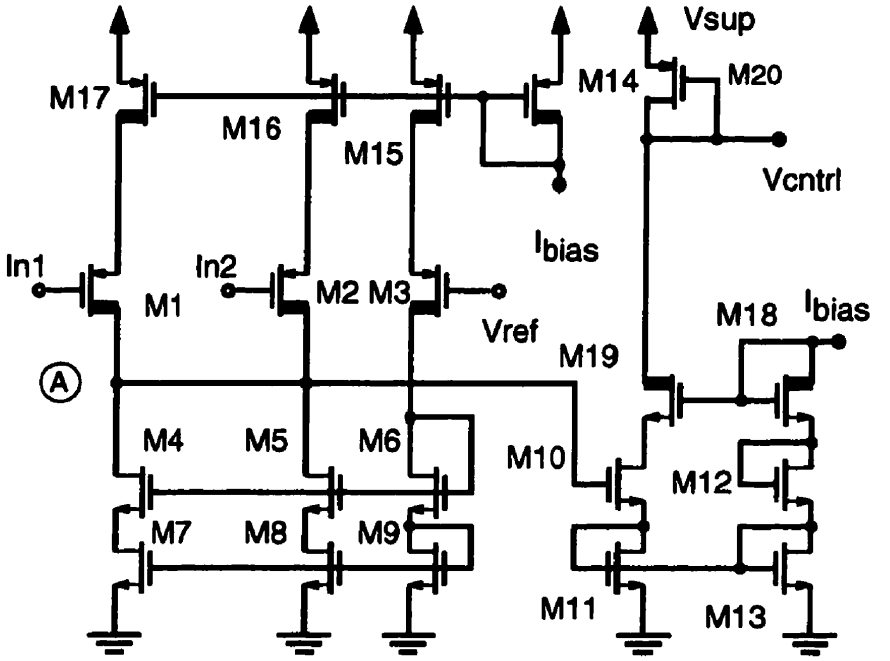


Fig. 4.3: Schematic diagram of the common-mode feedback circuit

Table 4.2: Device parameters of the CMFB circuit

Device		Parameter[1]
Low Voltage MOS	M4-M13	10μ/1.2μ
	M20	15μ/1.2μ
High Voltage MOS	M1-M3,M14-M19	64μ/3μ

1. Aspect ratio for MOS device, emitter area for bipolars

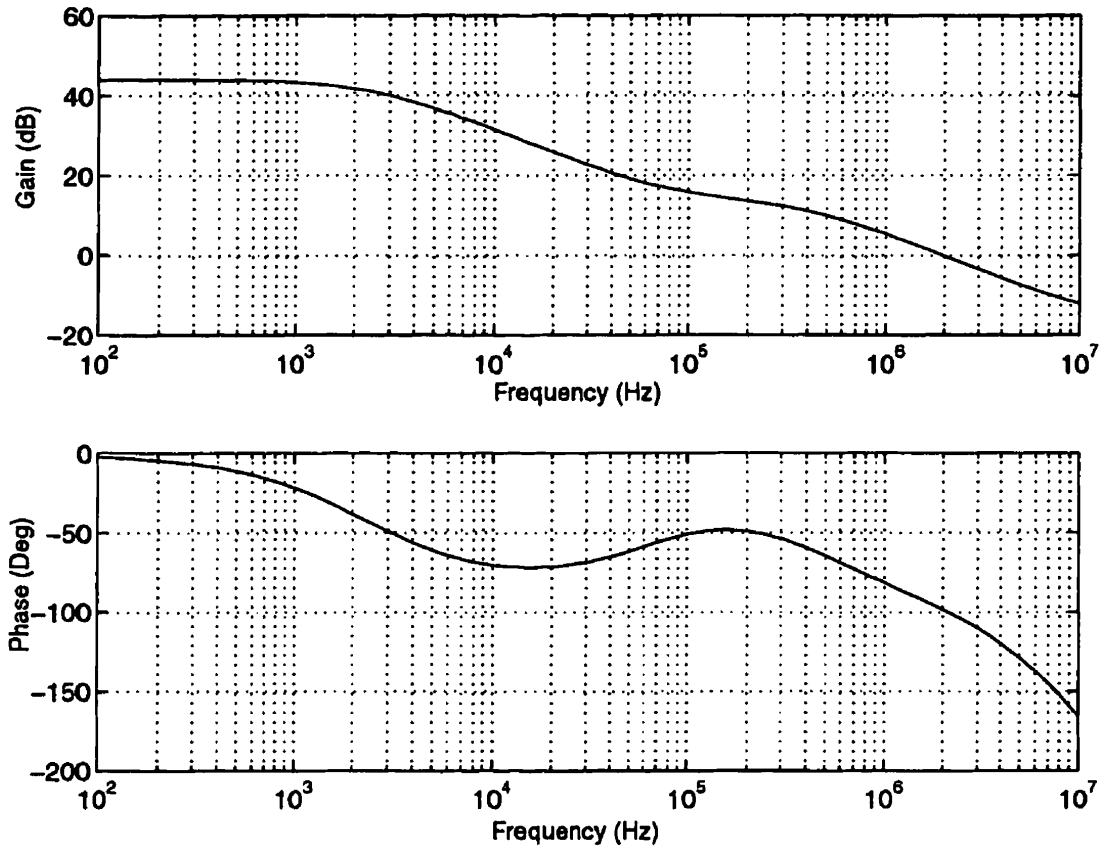


Fig. 4.4: Frequency response of the CMFB loop

identical. For this reason, diode-connected transistors M11-M13, were used as level shifters to match the terminal voltages of M10 to those of M4, M5 and M6. The high voltage devices M18 and M19 protect the current source M10-M13 from the high supply voltage. A chain of diode-connected bipolar transistors where also used to protect the gate of M10.

Similar to any other feedback system, the stability of the CMFB loop must be ensured. The open-loop frequency response of the CMFB circuit is presented in Fig. 4.4. Because of the much smaller transconductance of the input stage, the DC gain of the CMFB loop is lower than that of the differential opamp. The limited loop gain, ensures the stability in all operating conditions. This loop exhibits enough phase margin without the need for extra compensation capacitance. In fact, since the main high impedance node in the loop is the output of the differential amplifier, the load capacitances also help compensate the loop.

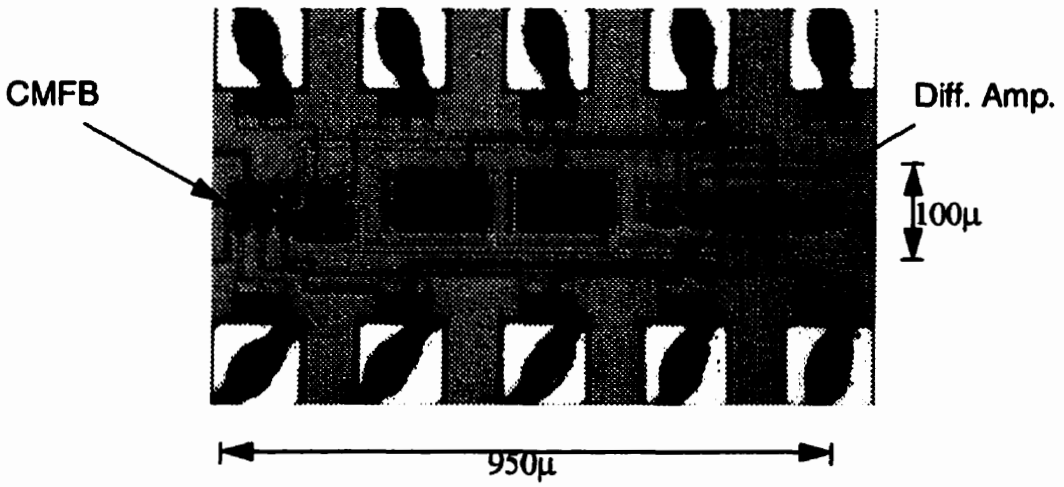


Fig. 4.5: Micrograph of the differential opamp and the CMFB circuit

4.2.2 Implementation and result

The preamplifier and common-mode feedback circuits were implemented in BATMOS-5 process. Fig. 4.5 shows the micrograph of the circuit. Total area for both circuits is less than 0.1 mm^2.

The transfer and gain characteristics of the preamplifier including the CMFB circuit are illustrated in Fig. 4.6. This block provides around 80 dB gain with a unity-gain bandwidth of 30MHz with more than 50° phase margin. Total power dissipation is less than 10mW. The transfer characteristics of the CMFB circuit are also shown in Fig. 4.7. This graph shows the output current of the CMFB circuit (the current in transistor M20) with respect to the common-mode voltage at the inputs. This current is mirrored back into the differential amplifier to adjust its common-mode output voltage. Table 4.3 summarizes the performance of the differential amplifier with the CMFB circuit. The agreement between the simulation and experimental results is better than 15%.

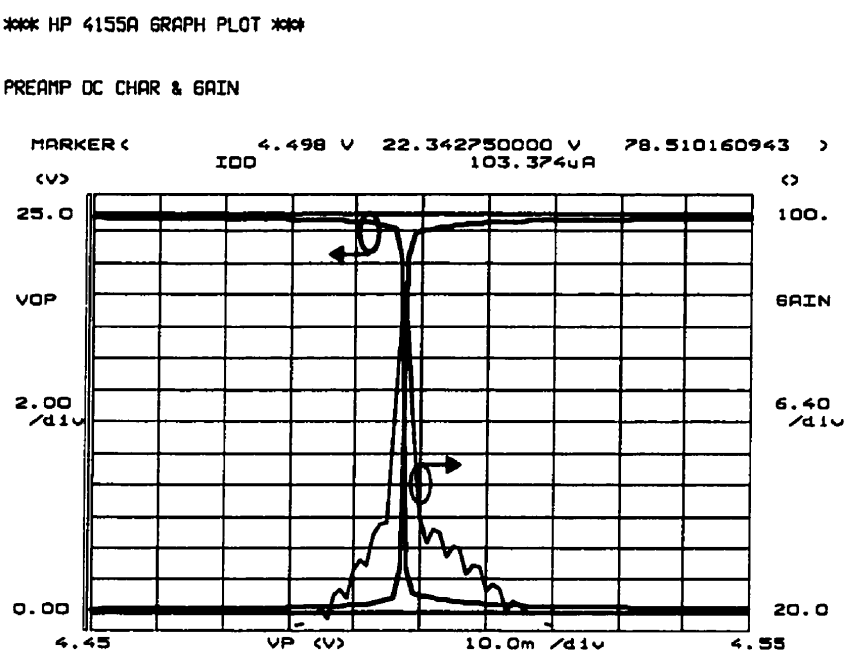


Fig. 4.6: Transfer characteristics and gain of the differential opamp

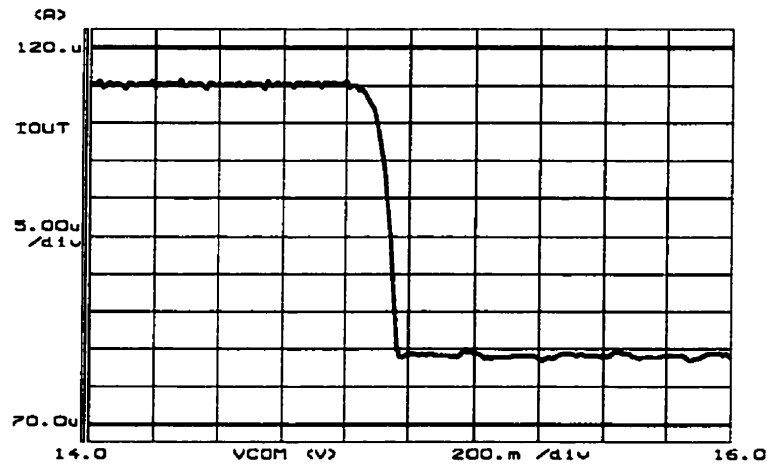


Fig. 4.7: Transfer characteristics of the CMFB circuit

Table 4.3: Preamplifier characteristics

Parameter	Post-layout Simulation	Measurement
Area		0.1 mm^2
Max. Power Supply	30 V	30 V
Power	8.5 mW	10 mW
Unity-Gain Bandwidth	35 MHz	30 MHz
Phase Margin	50°	>50°

4.3 Power Supply Switch

Since a high-side switch is required to connect the power supply to the line driver circuits, only the high voltage PMOS device can be used to implement the switch. However, such a switch requires a driver circuit to provide a proper switching signal on its gate. The power switch and the associated driver circuit is illustrated in Fig. 4.8. The power switch is a large high voltage PMOS transistor (MSW), controlled by the driver circuit. The function of the driver circuit is to shift up the DC level of the control input V_{in}, close to the supply voltage. In order to apply the switching signal to the gate of MSW, the driver must be able to provide enough charging and discharging current for the large gate capacitance of MSW.

The low voltage control signal V_{in} is compared with a reference voltage V_{ref}, using a comparator, made up of Q1 and Q2. V_{ref} is adjusted according to the amplitude and the DC level of the control voltage. The output of the comparator is latched by transistors M1 and M2. The diode-connected M3 and M4, reduce the gain of the latch to allow easy switching from one state to the other. A pair of high voltage NMOS devices M15,M16, isolate Q1 and Q2 from the high voltage rail.

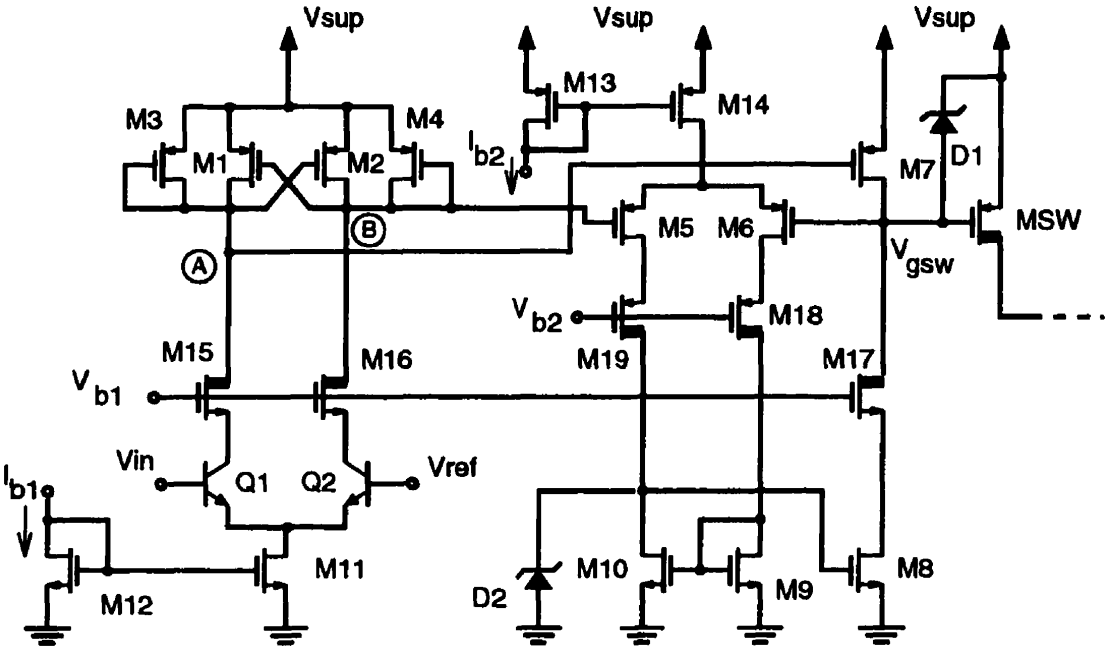


Fig. 4.8: Schematic diagram of the power switch driver

Table 4.4: Device parameters of the power switch driver

Device		Parameter[1]
Low Voltage MOS	M1,M2,M9,M10	1.8μ/1.2μ
	M3,M4	3.6μ/1.2μ
	M5,M6,M11-M14	30μ/1.2μ
	M7	60μ/1.2μ
	M8	40μ/1.2μ
	M9,M10	1.8μ/1.2μ
	M20	15μ/1.2μ
High Voltage MOS	M15-M19	64μ/3μ
	MSW	15000μ/3μ
Low Voltage NPN	Q1,Q2	4x0.8 μ^2

1. Aspect ratio for MOS device, emitter area for bipolars

When V_{in} becomes larger than V_{ref}, the voltage on node A drops, turning the pull-up transistor M7 on. As a result, the gate capacitance of MSW is charged up to V_{sup}, turning the switch MSW off. If V_{in} goes lower than V_{ref}, the latch changes its state, V_A rises to V_{sup} and V_B drops. Although the pull-up transistor M7 turns off, still a discharging current is needed to pull the gate voltage of the switch down. The pull-down transistor M8 is controlled by a comparator made up of M5 and M6. When V_B is lower than V_{gsw}, M5 turns on and makes the gate voltage of M8 rise. Therefore, the pull-down transistor M8 starts discharging the gate of MSW. However, this process must be stopped when V_{gsw} becomes low enough to turn MSW on, otherwise V_{gsw} keeps decreasing until the gate of MSW breaks down.

The function of M5,M6 comparator is to shut down M8 as soon as V_{gsw} becomes smaller than V_B. In that case, M7 passes all the current in that stage, causing the gate voltage of M1 to drop to zero. Therefore, both pull-down and pull-up paths remain off until the control input changes.

Table 4.4 lists the device sizes used in this design. Gate protection diodes D1 and D2, are implemented using a chain of diode connected NPN transistors.

4.3.1 Experimental results

The micrograph of the power switch and its driver circuit is illustrated in Fig. 4.9. The power switch is implemented using an array of high voltage PMOS transistors. The switch occupies about 0.23 mm^2 of area. The area of the driver circuit (0.02 mm^2) is almost negligible compared to that of the switch. The switch driver circuit is tested with a 1.8 Vp.p switching signal (V_{in}) and 2.5 V reference voltage (V_{ref}). The switching waveforms at the input and output of the driver (V_{gsw}) are shown in Fig. 4.10. The negative transient is caused by the pull-down transistor M8 to charge the gate capacitance of the switch and turn it on. The discrepancy between the simulated and experimental results is no larger than 15%.

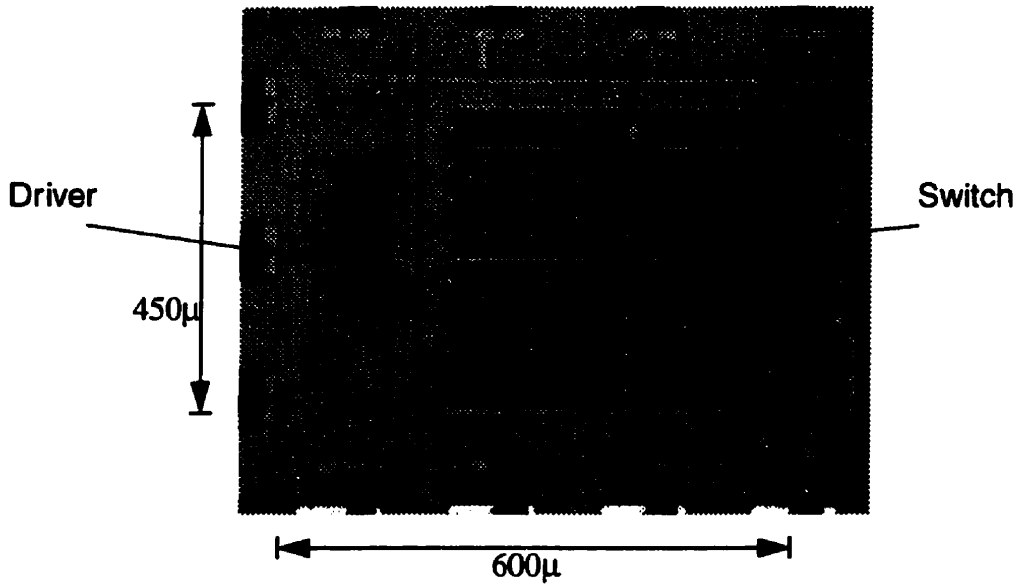


Fig. 4.9: Micrograph of the power switch and the driver circuit

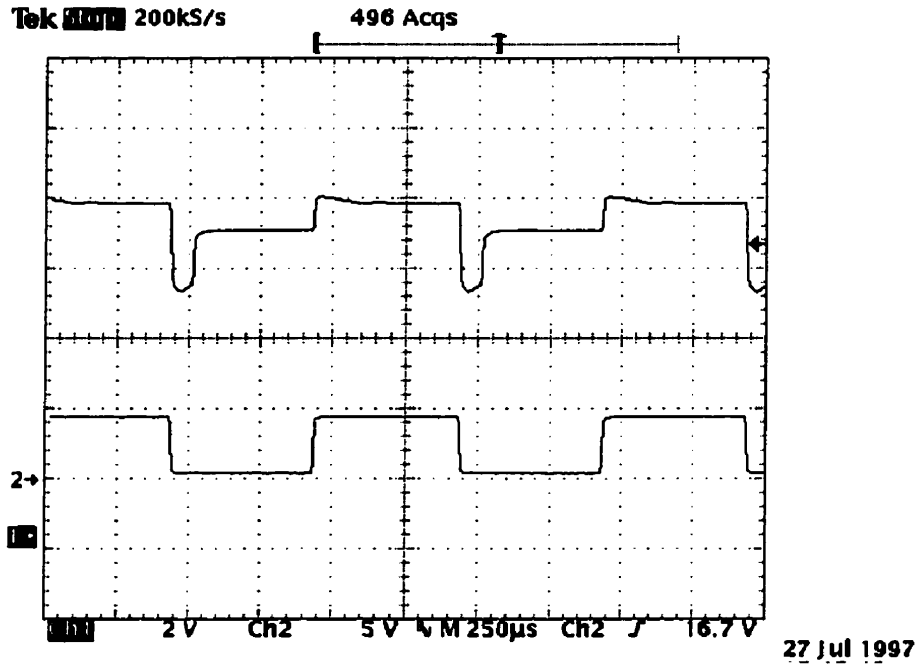


Fig. 4.10: Waveforms of the switch driver circuit: Upper trace: Ch2-output, Lower trace: Ch1-input

4.4 Line Driver Design

Because of the heavy load at the output of the line driver, a two stage architecture must be used for the line driver as illustrated in Fig. 4.11. The first stage, usually a transconductance amplifier, provides a differential input with a large amount of gain. The output stage is usually a push-pull circuit with a low output impedance and a large current driving capability. Acting as a buffer, this stage is able to provide high voltages and currents to a large resistive and capacitive load.

One of the main characteristics of the output stage is its power efficiency. While a large amount of power must be delivered to the load, the internal power dissipation must be kept at a minimum. Therefore, the main design objective is to obtain a high ratio between the peak current to be delivered to the load and the quiescent current which must be very well-controlled. This constraint prevents the use of conventional class A stages with current mirror biasing, illustrated in Fig. 4.12. In order to provide a large current at the output (in the mA range) and limit the bias currents in other stages (to the μA range), a high-ratio current mirror is required (more than 100). However, such a current mirror is not attractive because it results in a high quiescent current (I_q) in the output transistors (almost the same as the maximum output current) which is highly sensitive to any mismatch in the current mirror.

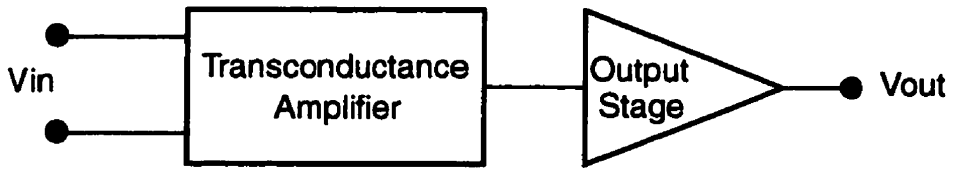


Fig. 4.11: Architecture of a line driver

For this reason, class AB or class B are preferred as output stages[2]. A class AB stage has a low quiescent current but it is capable of increasing its output current when needed. In class B, the quiescent current is actually zero while the load current can be quite large. Although class B schemes provide high power efficiencies, they suffer from crossover distortion problems. Especially, when signal amplitude is smaller than the offset voltage, the output stage cannot be turned on. Therefore, a class B stage is often accompanied by a class AB stage to handle small signals[3].

A class AB stage includes two output devices in a push-pull configuration and a quiescent current control mechanism as conceptually shown in Fig. 4.13. A complementary pair of PMOS and NMOS transistors are often used as pull-down (M1) and pull-up (M2) devices. However, output stages with a single type of device are also attractive when the behavior of NMOS and PMOS devices are asymmetrical [4].

The implementation of the output stage tends to vary widely depending on the specific application and the particular technology used. Classical source-coupled class AB stages are seldom used because of their limited output swing [5]. A large number of output stages

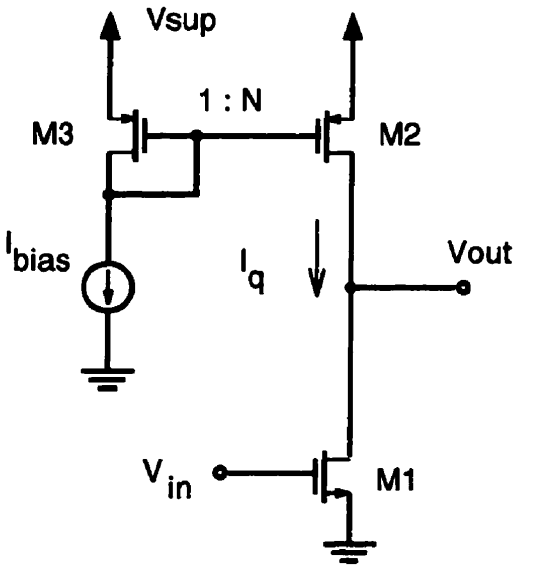


Fig. 4.12: Class A output stage with current mirror biasing

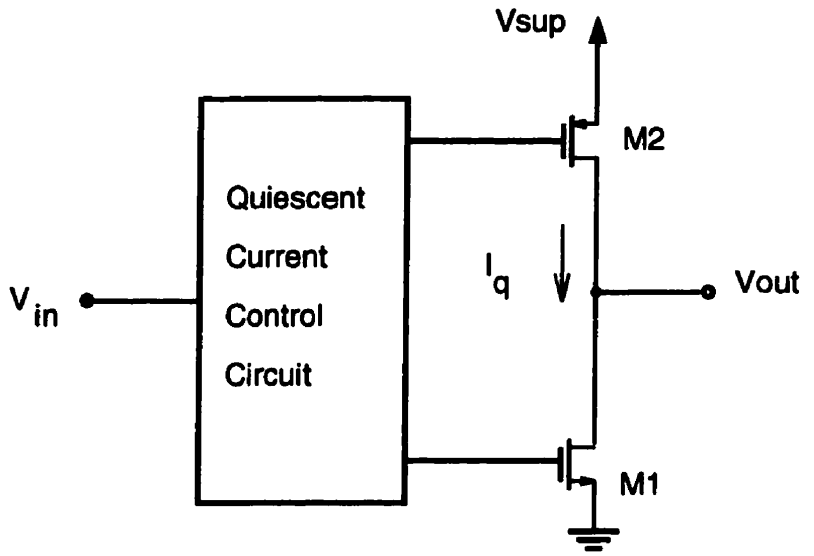


Fig. 4.13: General structure of a class AB output stage

use a pseudo-source-follower technique with feedback amplifiers to control the quiescent current [6-7]. In these circuits, the accuracy of the bias current is sensitive to the amplifier's offset voltage which is hard to control. Therefore, the output stage is usually forced to operate in class B mode to handle high currents and an extra class AB stage is added for small output currents. Because of the large amount of internal circuitry and power dissipation required, this technique is not suitable for high voltage applications.

Other proposed class AB stages are based on adaptive biasing schemes [8]. In these circuits, the bias current is proportionally increased with the load current. As a result the internal power dissipation also increases while driving high load currents. In addition, most of these circuits require the high voltage NMOS devices to operate in common-drain configurations with high voltage levels on their source terminal. As mentioned previously, this is not possible with the available high voltage NMOS devices (see Chapter 3).

For these reasons, two special output stages were chosen to implement the high voltage line drivers in this thesis. The first technique is based on a quasi-current-mirror (QCM) which is used for the first two line drivers presented in this chapter. This structure provides

good control over the quiescent current in a small area with a very low power dissipation. A CMOS QCM (CQCM) and a BiCMOS QCM (BQCM) line driver are implemented using this technique. The second approach uses a floating current mirror (FCM) technique to control the quiescent current of a PMOS only output stage. This structure is more robust with respect to hot-carrier problems associated with the high voltage NMOS devices as mentioned in Chapter 3. A FCM line driver is also presented.

4.5 CMOS Line Driver with QCM Output Stage (CQCM)

In this section, the design and implementation of a 30V CMOS line driver is presented. A quasi-current-mirror (QCM) technique is used in the design to control the quiescent current of the output stage. This low-cost compact line driver is suitable for twin-tub CMOS processes.

4.5.1 Circuit Description

The main objective in this design is to keep the idle power consumption as low as possible while providing high output current driving capability. Therefore, the number of bias current paths from the positive power supply to ground are kept small and the bias current for each individual stage is reduced to a minimum without degrading overall circuit performance.

A schematic diagram of the CQCM line driver is shown in Fig. 4.14. The circuit consists of a three stage amplifier with biasing circuitry. As explained in Section 3.4, high voltage NMOS devices cannot be used in a floating configuration because their source terminal is not capable of handling large voltage swings with respect to the substrate. Therefore, only HVPMOS transistors are used in the input stage without limiting the input common-mode range. Transistors M1-M8 at the input stage form an operational transconductance amplifier (OTA) with a g_m which determines the gain and bandwidth of

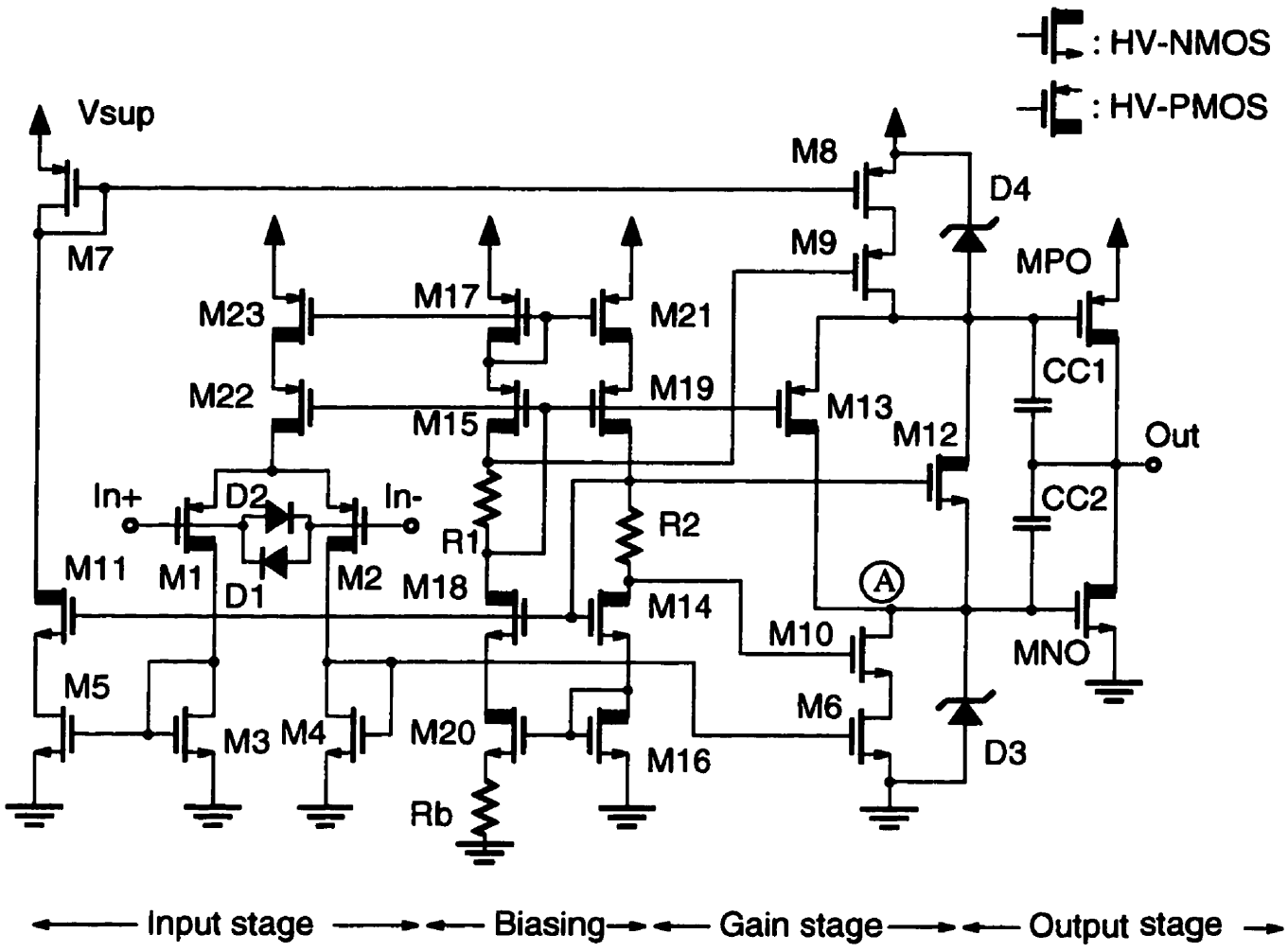


Fig. 4.14: Schematic diagram of the CQCM line driver

the whole circuit. The input transistors (M1,M2) are large enough to provide the required transconductance at low bias current. In order to minimize the parasitic capacitances in the signal path, all the current mirrors in the input OTA are implemented using small low voltage MOS transistors. However, the high voltage transistor M11 is used to withstand the large power supply voltage and limit the drain source voltage of M5. Operating in a cascode configuration, M11 does not degrade the gain or frequency response of the OTA.

The input common-mode voltage range of the line driver is limited on the high side by the current source transistors M22 and M23. The upper limit for the input voltage is

$$V_{i_{max}} = V_{sup} - V_{gs_{22}} - V_{gs_{23}} - V_{gs_1} + V_T \tag{4.3}$$

where V_{sup} is the supply voltage, V_T is the threshold voltage of the high voltage PMOS devices, $V_{gs_{22}}$, $V_{gs_{23}}$ and V_{gs_1} are the gate-source voltages of M22, M23 and M1, respectively.

Typical values for V_{gs} and V_T result in a $V_{i_{max}}$ around 2.3V below V_{sup}. Although this limit can be increased if M22 is taken out of the circuit, the cascode combination of M22 and M23 decreases the sensitivity of the bias current of the input stage (hence, the gain and bandwidth of the line driver), to the input common-mode voltage which can vary over a wide range. Stabilizing the bias current of the input stage is very important since it controls the current in the QCM stage through the current mirrors M4,M6 and M3,M5. Other advantages such as higher common-mode and power supply rejection ratios are also achieved.

4.5.2 QCM Output Stage

A quasi-current mirror (QCM) output stage was chosen for this line driver because it requires a minimum amount of quiescent current control circuitry resulting in minimal idle power and area. The QCM structures consist of the four transistors M12, M14, M16 and

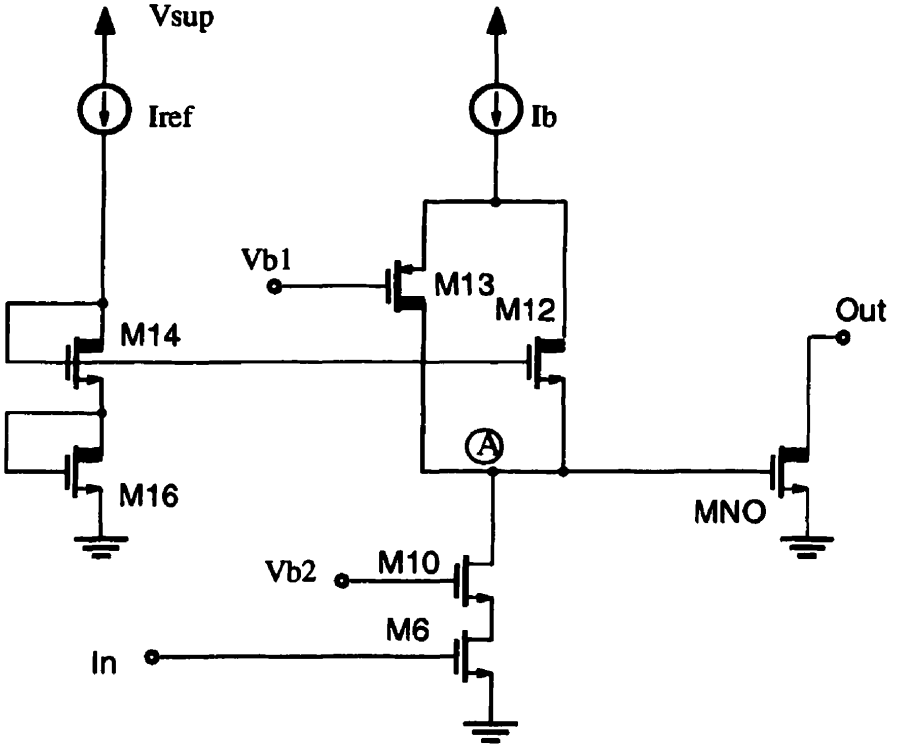


Fig. 4.15: Simplified diagram of the low-side CMOS quasi-current-mirror

MNO at the low-side and M13, M19, M21 and MPO at the high side (Fig. 4.14). A simplified diagram of the low-side QCM is illustrated in Fig. 4.15. With no load current, both transistors M12 and M13 are on and the bias current I_b is divided equally between them. Assuming that the current density in M12 and M14 is the same, i.e.,

$$\frac{I_b/2}{I_{ref}} = \frac{(W/L)_{M12}}{(W/L)_{M14}} \tag{4.4}$$

where I_{ref} is the reference current in M14 (Fig. 4.15). The ratio of the quiescent current in MNO (or MPO) I_q to the bias current of M16, I_{ref} is determined by the size ratio of MNO and M16 as

$$\frac{I_q}{I_{ref}} = \frac{(W/L)_{MNO}}{(W/L)_{M16}} \tag{4.5}$$

Whenever a large current must be sunk from the load, the current I_b is steered into M13 and M12 is turned off allowing the voltage at node A to rise. As a result, enough gate drive for MNO can be provided to sink load currents much larger than the quiescent current. Meanwhile, M13 limits the gate-source voltage of MPO keeping its current at a low level.

Similarly, when sourcing current to the load, M13 is turned off and M12 passes the current I_b . Therefore, the gate-source voltage of MPO can be increased as much as needed while the gate voltage of MNO is limited by M12 at node A. The upper and lower QCMs are merged to share the same bias currents (I_b and I_{ref}) saving additional current paths between power supply and ground and hence lower power consumption.

The gain stage is formed by transistors M6 and M10 on the low side and M8 and M9 on the high side. These small low voltage transistors in cascode configuration provide high voltage gain with minimal parasitics in the signal path. However, V_{b2} must be chosen properly such that both M6 and M10 operate in saturation region.

$$V_{gs_{10}} + V_{gs_6} - V_T < V_{b2} < V_{gs_{16}} + V_T \tag{4.6}$$

A typical value for the gate-source voltage V_{gs} at low current level is 1V while V_T is approximately 0.8V. Assuming all transistors have the same current density and hence the same V_{gs},

$$1.2\text{V} < V_{b2} < 1.8\text{V} \tag{4.7}$$

Therefore, the most suitable value for V_{b2} is 1.5V which leaves maximum margin for any voltage change due to process variations or mismatch. However, this bias voltage cannot be provided by the diode-connected transistors M14 and M16 because regardless of their size ratios, the voltage at node A, will always follow the voltage at the source of M14. Whereas V_{b2} must be 0.5V higher than node A voltage. Even the gate voltage of M14 cannot be used as V_{b2} because it is at least one V_T higher than node A. In order to save an

extra biasing stage for V_{b2}, the required voltage is made using a resistor in series with the drain of M14 (R2 in Fig. 4.14). The voltage drop across R2 is 0.5V, resulting in 1.5V at the drain of M14. Yet, the drain-source voltage of M14 is large enough to keep it in the triode region.

4.5.3 Device Parameters and Compensation

The aspect ratios of all transistors in this design are listed in Table 4.5. All high voltage transistors use a 3μm channel length to avoid punch-through and provide higher output resistance. The input devices M1 and M2 are chosen with large aspect ratio to provide adequate g_m for the required gain and bandwidth (Table 4.14). A 5kΩ bias resistor Rb, provides a 20μA current (I_{ref}) in the biasing stage which consists of transistors M15 to M21 (Fig. 4.14). The bias current of the input stage would then be determined by a 4:1 size ratio between M23 and M17 to be $4I_{ref}$. One half of this current is mirrored back by M4,M6 and M7,M8 pairs to the gain stage to make $I_b=2I_{ref}$.

For the QCM stage, both equations 4.4 and 4.5 must hold. With $I_b=2I_{ref}$, equation 4.4 results in the same size ratio for M12 and M14 (as well as M13 and M15). Output transistors MNO and MPO were chosen large enough to provide high output current at small gate voltages. The intention was to keep the current density low to avoid hot-carrier effects in the output transistor MNO. Therefore, MNO and M16 have a size ratio of 20:1 which according to equation 4.5 results in a quiescent current I_q of 400μA in the output stage.

The circuit is compensated using a conventional Miller technique. The advantage of this method is that the parasitic gate-drain capacitances of the large output transistors contribute to compensation, reducing the size of the extra compensation capacitors CC1 and CC2. As illustrated in Fig. 4.16, a unity-gain bandwidth of 2.5 MHz is expected with 50°

phase margin for a nominal 20 mA line current. A total of 8 pF capacitance was used to compensate for this circuit.

4.5.4 Gate Protection

As mentioned in Chapter 2, the gate-source voltage of all high voltage transistors must not exceed the 5V limit. Therefore, all the gate terminals must be protected against high voltage spikes. In this circuit, only the input and output transistors (M1,M2, MNO,MPO) are exposed to high voltage swings and hence must be protected.

Table 4.5: Device parameters of the CQCM line driver

Device		Parameter[1]
Low Voltage MOS	M3-M6	10μ/1μ
	M7,M8	20μ/1μ
	M9	40μ/1μ
	M10	20μ/1μ
High Voltage MOS	M1,M2	480μ/3μ
	M11-M15 M18,M19,M22	20μ/3μ
	M16	50μ/3μ
	M17,M21	100μ/3μ
	M20	200μ/3μ
	M23	400μ/3μ
	MNO	1000μ/3μ
	MPO	2000μ/3μ
Resistors	R1,R2	25kΩ
	Rb	5kΩ
Capacitors	CC1,CC2	4pF

1. Aspect ratio for MOS devices

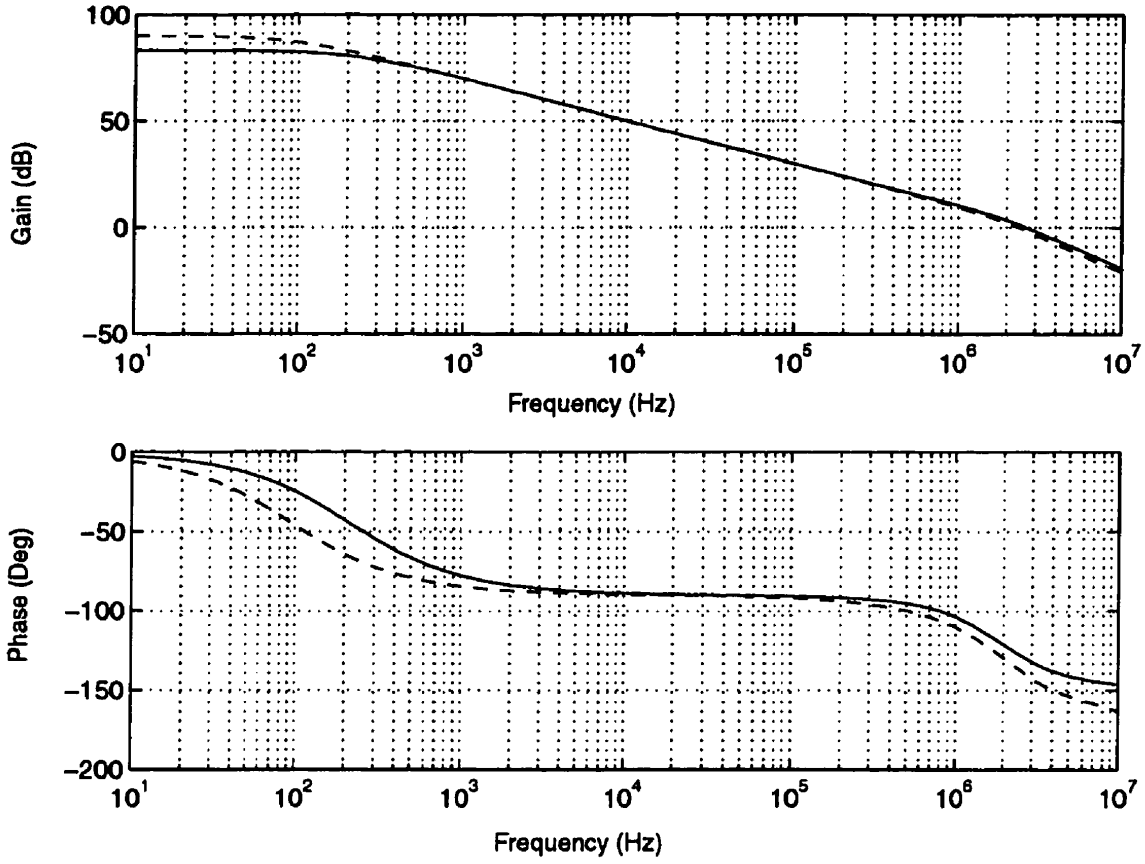


Fig. 4.16: Frequency response of the compensated (CC1=CC2=4pF) CQCM line driver in current-sink (solid line) and current-source (dashed line) modes.

The input transistors M1 and M2 can experience high voltage peaks during fast voltage transitions. If the non-inverting input voltage V_{in+} changes rapidly, due to the delay of the feedback loop, the inverting input cannot follow the change. Therefore one of the input transistors is completely turned on and the other one is turned off with a large reversed gate-source voltage on it. The function of protection diodes D1 and D2[1] (Fig. 4.14) is to limit that reverse voltage. Because there is no Zener diode available in the BiCMOS process used, a series chain of diode-connected bipolar transistors is used to implement D1 and D2.

Protection diodes are also used in the output stage (D3 and D4) to limit the gate voltage of the output transistors MNO and MPO. When the line driver tends to sink a large current

1. NPN bipolar transistors with connected base and collector were used as diodes.

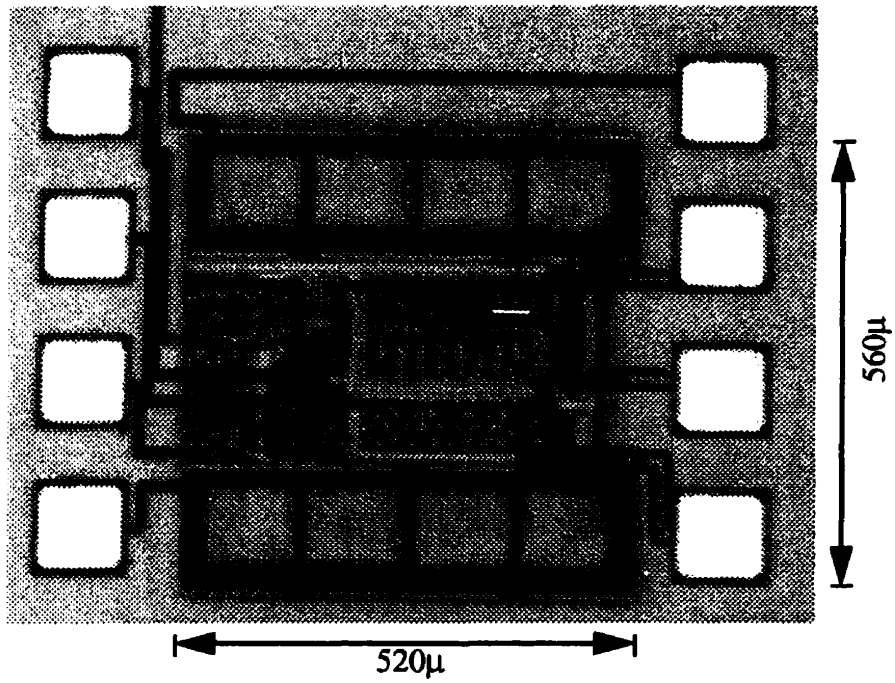


Fig. 4.17: Micrograph of the line driver

from the load, transistor M12 is turned off and the voltage on node A starts to rise (Fig. 4.14). Without D3, this voltage can rise to a voltage level close to V_{sup} which would damage the gate of MNO. Therefore, the role of D3 is to keep the voltage on node A less than 5V. Diodes D3 and D4 were also implemented using diode-connected NPN transistors in series.

4.5.5 Implementation and Results

The circuit of Fig. 4.14 was implemented in the BATMOS-10 process. A micrograph of this circuit is shown in Fig. 4.25. The total area of the line driver is less than 0.3 mm^2 with high-voltage compensation capacitors occupying a large portion of the chip area. The large high-voltage output transistors are laid out as 10 parallel smaller devices to distribute the power and improve the matching in current mirrors. Each high-voltage device is surrounded by substrate contact rings to reduce substrate noise and prevent latch-up.

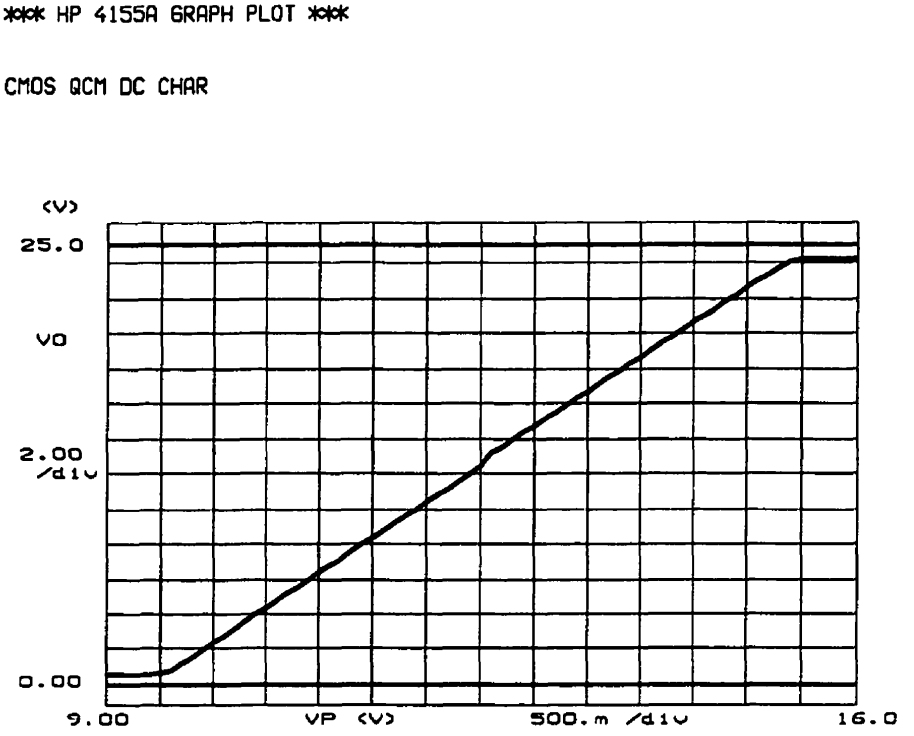


Fig. 4.18: DC characteristic of the CQCM line driver

Fig. 4.18 shows the DC transfer characteristic of the line driver. The line driver was tested in a non-inverting feedback configuration with a gain of 4 to eliminate the need for an extra preamplifier. A wide output range within 1.4 V of the power supply rails was achieved with the nominal 20 mA load current. The circuit is operational up to a maximum supply voltage of 30V. While more than 30 mA can be delivered to the load, the total internal idle current is no larger than 830 μA. The step response of the line driver is illustrated in Fig. 4.19. The circuit features a slew rate of more than 1.4 V/μs.

The unity-gain bandwidth of the line driver is more than 2.1 MHz with a phase margin of greater than 44° at the nominal 20 mA line current. Fig. 4.20 shows the dependence of the bandwidth to the line current. This dependence is a result of the modulation of the output stage transconductance by the line current. Because of the pole-splitting characteristic of the Miller compensation loop, increasing the transconductance of the

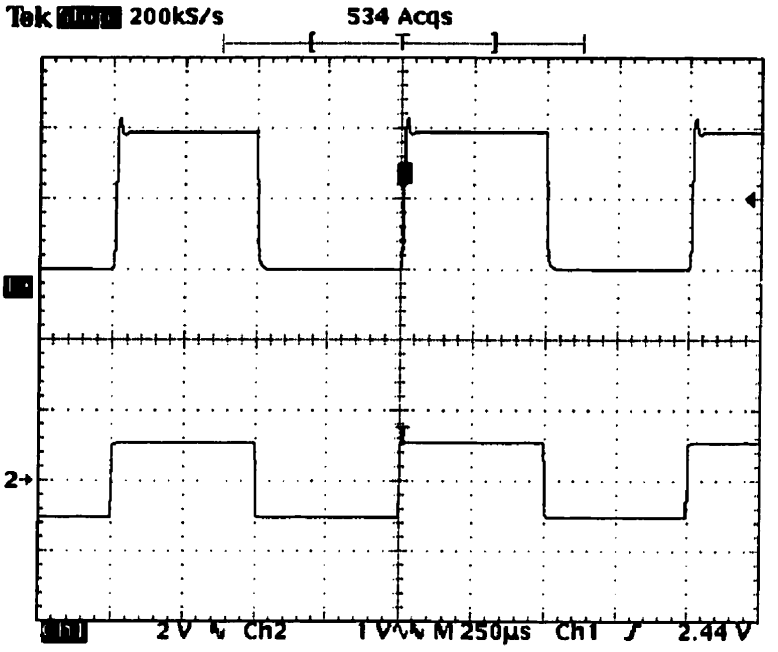


Fig. 4.19: Step response of the CQCM line driver, Upper trace: Ch1-Output, Lower trace: Ch2-Input:

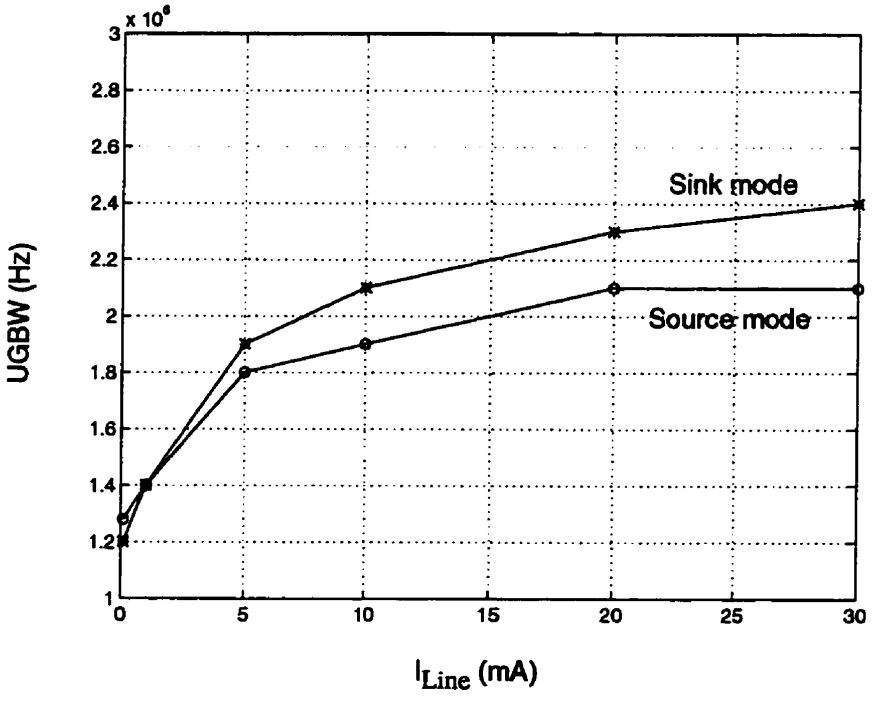


Fig. 4.20: Unity-gain bandwidth (UGBW) of the line driver vs. the output current

output stage would extend the bandwidth by pushing the second pole to higher frequencies. Therefore, the bandwidth is minimum at zero line current.

The output impedance of the line driver is less than 0.2Ω satisfying the SLIC longitudinal balance requirement. The circuit also feature a PSRR of more than 54 dB in the voice band which helps reduce the supply noise injected to the lines. Total harmonic distortion (THD) for a standard metering signal (1.5 V_{rms} at 16 KHz) [4] is less than 0.08%.

Table 4.5 summarizes the characteristics of the line driver. In general, the experimental results are within 20% agreement with the simulated values. To further investigate the sensitivity of the circuit to process variations, Monte Carlo simulations were performed with 10% tolerance for the high voltage device parameters such as length, width and threshold voltage[1]. For low voltage components, the best and worst case model sets provided by Nortel were used. The quiescent current, as the most critical circuit parameter, exhibited less than 30% variation. However, due to the inherent design margins, it never exceeds the 1mA target limit. Thermal stability of the circuit was also investigated over a wide range of temperatures (-40 to 125 °C) with simulation results indicating less than 20% variation in the quiescent current.

1. The worst-case tolerances for the high voltage device dimensions cover the channel length variations due to the NWELL lateral diffusion (0.2-0.3μm) as well as any inaccuracy in the channel width measurement due to the circular shape of the devices.

Table 4.6: CQCM line driver characteristics

Parameter	Post-layout Simulation	Measurement
Area		0.3 mm^2
Maximum Supply Voltage	30V	30 V
Maximum Output Current	30 mA	>30 mA
Idle Current	710μA	830 μA
Unity-Gain Bandwidth :		
Source Mode (I_{Load} > 10 mA)	2.2 MHz	>1.9 MHz
Sink Mode (I_{Load} > 10 mA)	2.4 MHz	> 2.1 MHz
Power Supply Rejection Ratio :		
at 4 KHz	57 dB	< 54 dB
at 1 MHz	5 dB	< 0 dB
Output Impedance :		
at DC	0.05 Ω	< 0.15 Ω
at 10 KHz	0.5 Ω	< 0.9 Ω
Slew Rate	1.5 V/μs	> 1.4 V/μs
Total Harmonic Distortion for a 2Vp.,16 KHz metering signal	0.06%	< 0.08%
Output Swing	V_{sup} - 1.1 V	V_{sup} -1.4 V

4.6 BiCMOS line driver with QCM output stage (BQCM)

In this section, the design and implementation of a 30V BiCMOS line driver is presented. Similar to the CQCM line driver presented in Section 4.5, this circuit uses a QCM output stage. However, by using complementary bipolar transistors available in the BATMOS-10 process, considerable improvements in performance are achieved.

4.6.1 Circuit Description

The schematic diagram of the BQCM line driver is shown in Fig. 4.21. The general architecture of the circuit is similar to the CQCM line driver with an OTA input stage (M1-M8) and QCM class AB stage at the output (M12-M15). However, low voltage bipolar transistors are added at appropriate places to boost up the circuit performance. The two major objectives sought by using bipolar transistors in this design are:

a) improving the matching in the QCM stages to achieve a better controlled quiescent current in the output stage, and
b) increasing the gain of the output stage thus increasing the bandwidth and reducing the compensation capacitance.

In a QCM output stage, the quiescent current is susceptible to the matching between the current mirror transistors. Unlike their low-voltage counterparts, HVMOS devices are not self-aligned on the drain side and are more sensitive to process variations. A well-controlled quiescent current can be achieved, if the QCM stages rely only on the matching between low-voltage components such as low voltage CMOS and bipolar transistors available in the BiCMOS process. Moreover, the high transconductance of bipolar transistors provides higher gain and superior frequency response for the line driver.

Fig. 4.22, shows the low-side QCM stage of the BQCM line driver. Due to their limited breakdown voltage (8V), bipolar transistors cannot be used to simply replace the HVMOS

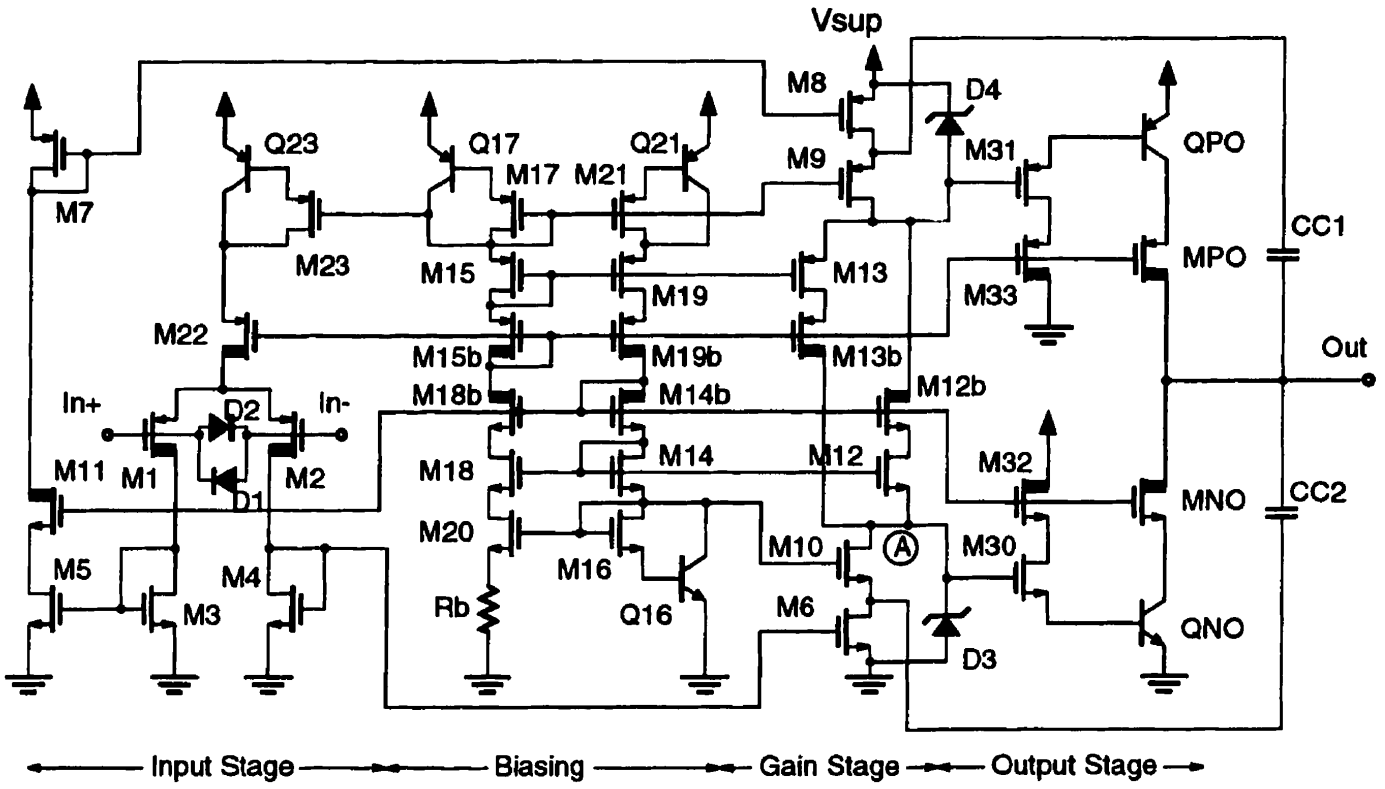


Fig. 4.21: Schematic diagram of the BQCM line driver

devices . The best solution is to use a BJT with a HVMOS device in a cascode configuration to achieve both high transconductance and high breakdown voltage simultaneously. MNO is the cascode transistor which handles the high voltage swing and M30 acts as a buffer, isolating the base current of QNO from the previous gain stage.

The relation between the bias currents I_b and I_{ref} (shown in Fig. 4.22) is the same as equation 4.4. The quiescent current I_q in QNO, is given by

$$\frac{I_q}{I_{ref}} = \frac{(W/L)_{M30}}{(W/L)_{M16}} = \frac{A_{QNO}}{A_{Q16}} \tag{4.8}$$

where A_{QNO} and A_{Q16} are the emitter areas of QNO and Q16 respectively. Note that only the parameters of well-matched low-voltage devices appear in equation 4.4 and 4.5,

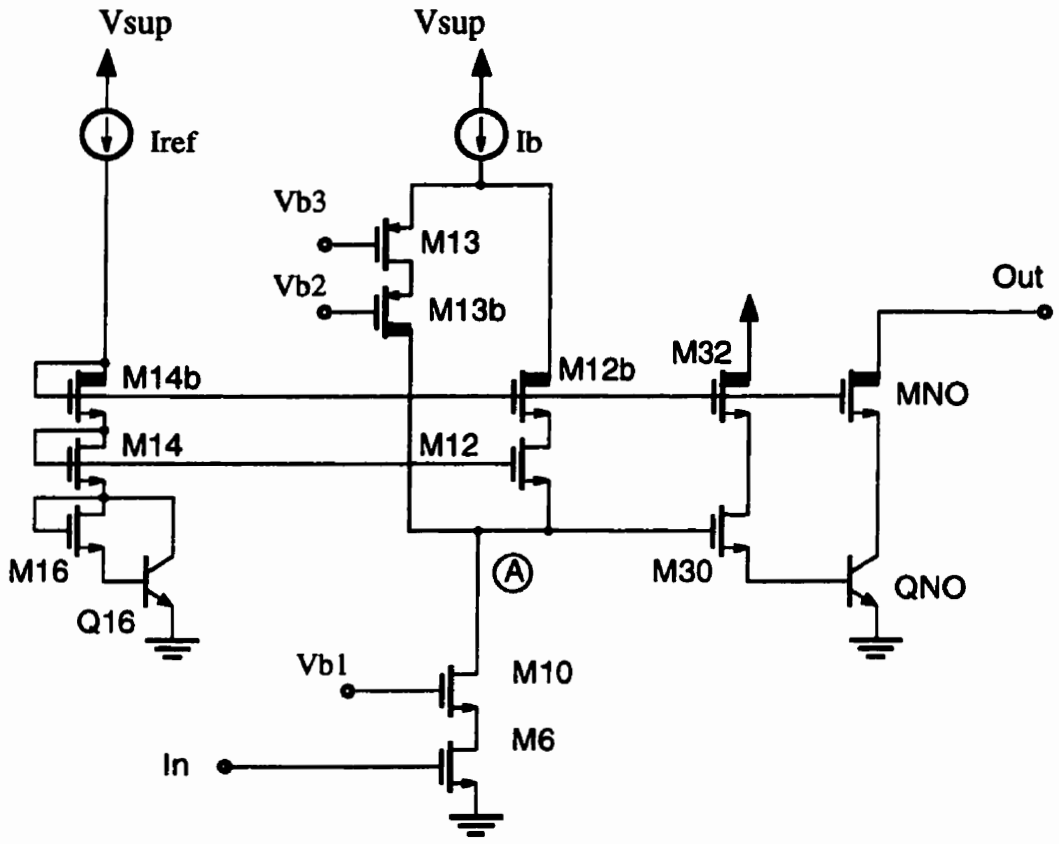


Fig. 4.22: Simplified diagram of the low-side BiCMOS quasi-current mirror stage

resulting in a more accurate quiescent current in the output stage. The high voltage devices M14b, M12b, M32 and MNO are all used in a cascode configuration with no impact on the quiescent current of the output stage. As a result, the sensitivity of the idle power consumption to process variations is greatly reduced.

The low voltage transistors M6 and M10 in Fig. 4.22, form a cascode gain stage boosting the overall gain of the line driver. The stacked BJT and HVMOS devices in the output stage tend to reduce the output voltage range. To withstand the high operating voltage, stacking devices in the output stage is inevitable. However, the output HVPMOS and HVNMOS transistors (MNO,MPO), are chosen large enough to let the output swings within 1.5 volts from the supply rails.

4.6.2 Device Parameters

Table 4.5 shows the aspect ratio of all transistors in this design as well as the values for resistors and capacitors. The bias current ratios are similar to those of the CQCM line driver. A 25kΩ bias resistor Rb, provides a 30μA current (I_{ref}) in the biasing stage consisting of transistors M14 to M21, Q16, Q17 and Q21 (Fig. 4.21). The bias current of the input stage, $4I_{ref,}$ is determined by a 4:1 aspect ratio between M23 and M17 to be . The current I_b in the QCM stage is $2I_{ref}$. The size of the devices in the output stage can then be determined from equation 4.4 and equation 4.5.

4.6.3 Compensation

The use of the BJTs increases the gain of the output stage which is heavily loaded by the loop impedance. As a result, a cascode Miller compensation technique [9] can be efficiently used in this case to increase the bandwidth using a smaller compensation capacitor than in the case of the CQCM line driver.

In the cascode Miller technique, the compensation capacitor C_C is connected to the source terminal of the cascode transistor (M9 or M10) in the gain stage rather than the high-impedance node A (Fig. 4.21). The high frequency feedback through C_C and M10 (or M9) provides the classical Miller effect and pole splitting. However, there is no feed-forward path from node A to the output through C_C. As a result, the right-half-plane zero of the transfer function, present in conventional compensation methods, is eliminated and the second pole is pushed up to higher frequencies.

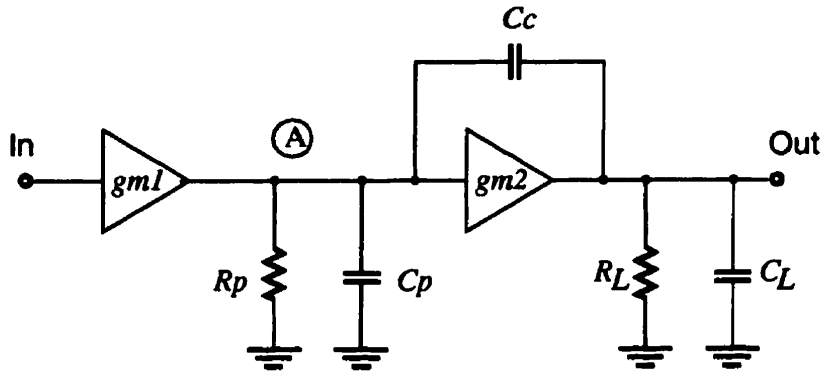
To clarify the advantage of this compensation method, simplified models for both the conventional Miller and the cascode Miller techniques are illustrated in Figs 4.23a and 4.23b. In these figures, g_{m1} and g_{m2} (g'_{m1} and g'_{m2}) represent the transconductances of the first and second stages respectively. The impedance at node A is modeled by C_P and R_P (C'_P and R'_P), the load impedance consists of R_L and C_L, and C_C (C'_C) is the compensation

capacitor. The unity-gain cutoff frequency for both configurations depends on the transconductance of the first stage and the compensation capacitance: $\omega_t = g_{m1}/C_C$ for circuit

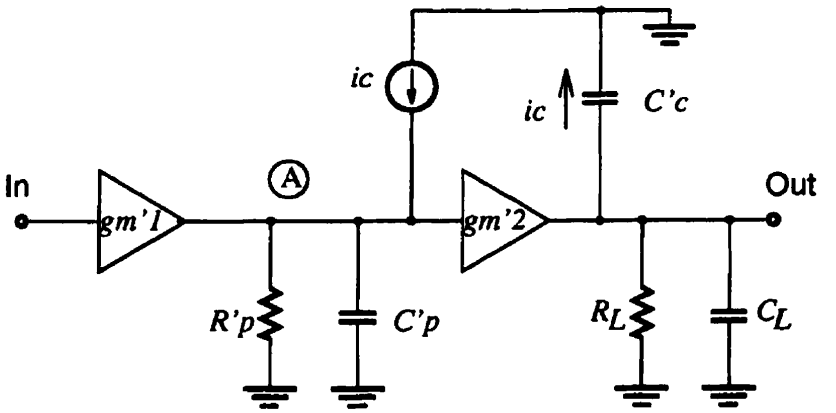
Table 4.7: Device parameters of the BQCM line driver

Device		Parameter[1]
Low Voltage MOS	M3-M6	10μ/1μ
	M7,M8,M10,M30,M31	20μ/1μ
	M9	40μ/1μ
	M12-M15,M18,M19	2.6μ/1μ
	M16,M17,M21	2μ/1μ
	M20	6μ/1μ
	M23	8μ/1μ
High Voltage MOS	M1,M2	100μ/3μ
	M11,M12b-M15b, M18b,M19b,M22	10μ/3μ
	M32,M33	100μ/3μ
	MNO	1000μ/3μ
	MPO	2000μ/3μ
Low Voltage NPN	Q16	3x4x0.8 μ^2
	QNO	2x60x0.8 μ^2
Low Voltage PNP	Q17,Q21	80x0.8 μ^2
	QPO	10x80x0.8 μ^2
	Q23	4x0.8 μ^2
Resistors	Rb	25kΩ
Capacitors	CC1,CC2	2pF

1. Aspect ratio for MOS device, emitter area for bipolars



(a)



(b)

Fig. 4.23: AC models for a) Miller, and b) cascode Miller compensation techniques

(a) and $\omega'_t = g'_{m1}/C'_C$ for circuit (b). There is a right-hand-plane zero, $z = g_{m2}/C_C$ in circuit (a) and the second pole is at

$$P_2 = \frac{g_{m2}C_C}{C_P C_C + (C_P + C_C)C_L} \tag{4.9}$$

On the other hand, there is no zero in circuit (b) and the second pole is at a higher frequency

$$P'_2 = \frac{g'_{m2}C'_C}{C'_PC'_C + C'_PC_L} \tag{4.10}$$

For stability, the unity-gain cutoff frequency ω_t must be smaller than the frequency of the second pole P_2 (or P'_2). Therefore, the ratio between the second pole frequencies P'_2/P_2 is a measure of the improvement in the maximum achievable bandwidth. Assuming a large load capacitance: $C_L >> C_P$, C_C (or C'_P, C'_C) , the ratio can be expressed as

$$\frac{P'_2}{P_2} = \frac{g'_{m2}}{g_{m2}}\frac{C'_C}{C_C}\frac{C_P + C_C}{C'_P} \tag{4.11}$$

For the same C_C and g_{m2} (C_C=C'_C , g_{m2}=g'_{m2}), the improvement factor is $(C_P+C_C)/C'_P$. This is a considerable increase in the maximum bandwidth if $C_P \leq C_C$. As a result, the compensation capacitor C'_C in circuit (b), can be reduced while increasing the bandwidth. However, if C_P is large, the improvement factor becomes insignificant, reducing the efficiency of the cascode Miller compensation method. In the CQCM line driver of Fig. 4.14, the gate capacitance of the large output transistors (MNO and MPO) result in a large value for C_P hence there is no advantage in using cascode Miller method in that circuit. Whereas in the BQCM line driver of Fig. 4.21, the large parasitic capacitance of the output transistors (QNO,QPO) are isolated from node A by the Darlington buffers (M30,M31), resulting in small C_P , making the cascode Miller technique quite advantageous in this case.

The bipolar output stage, furthermore, contributes to the improvement factor of P'_2/P_2, through the transconductance ratio g'_{m2}/g_{m2}. It provides higher g'_{m2} in the BQCM design compared to the CQCM one. The overall bandwidth can be improved by a factor of two with half the compensation capacitor. The frequency response of the line driver is illustrated

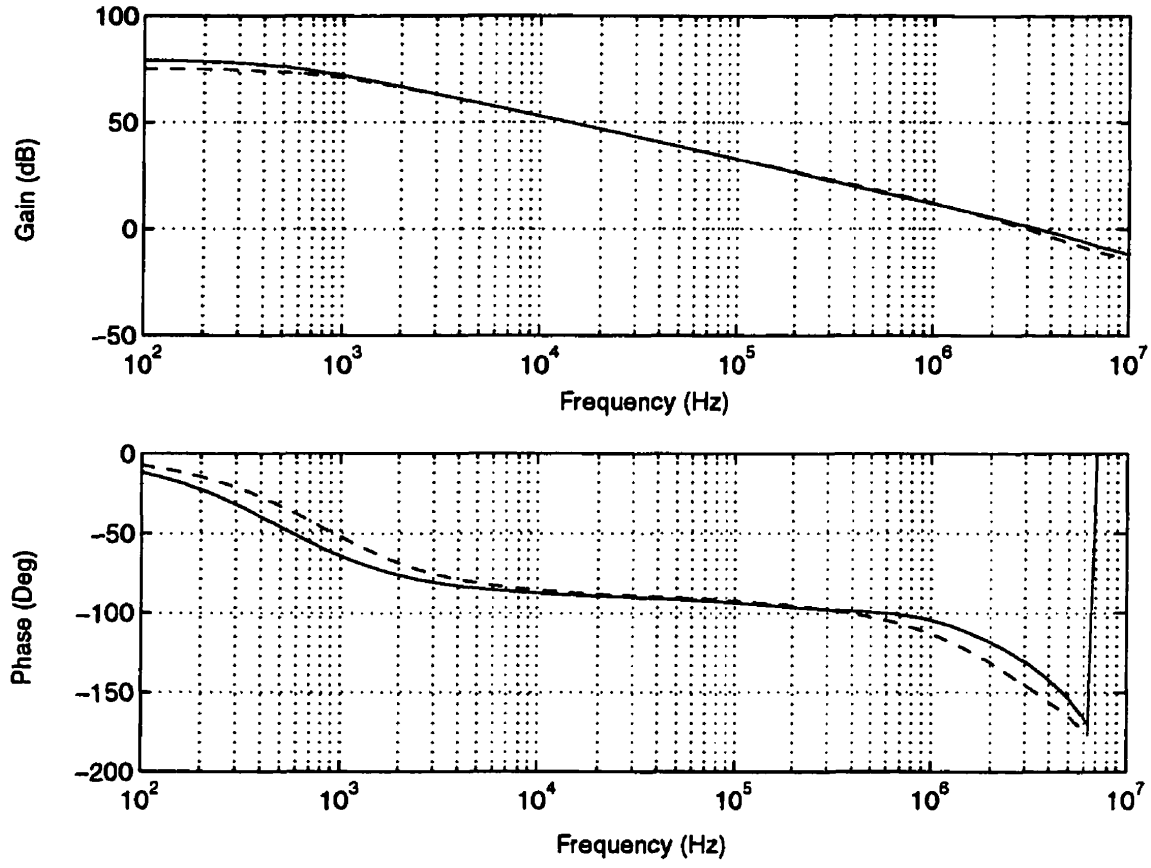


Fig. 4.24: Frequency response of the compensated (CC1=CC2=2pF) BQCM line driver in current-sink (solid line) and current-source (dashed line) modes.

in Fig. 4.24. A unity-gain bandwidth of 3.6 MHz is expected with a phase margin of greater than 45°. The circuit is compensated using a total of 4 pF compensation capacitance.

4.6.4 Implementation and Results

The circuit of Fig. 4.21 was successfully implemented in the BATMOS-10 V process. A micrograph of the implemented chip is illustrated in Fig. 4.25. The total core area of the line driver is less than 0.24 mm^2. Using the n-subwell layer available in this process, high-voltage NMOS devices are isolated from substrate reducing the body effect and substrate noise. This is specifically attractive for cascode devices specially in the output stage (MNO).

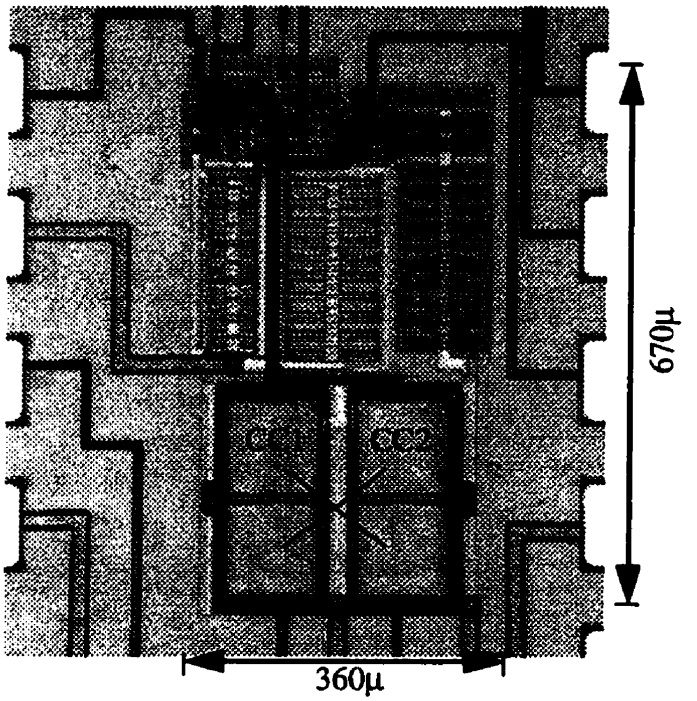


Fig. 4.25: Micrograph of the BQCM line driver

Fig. 4.26 shows the DC characteristics of the line driver measured in a non-inverting amplifier configuration with a gain of 4 (hence no need for a preamplifier) and maximum output load (R_L = 500Ω). The maximum output voltage range is 2.8 V below the power supply voltage. More than 30mA can be delivered to the load at full output swing. The driving current can be easily increased by using larger output devices at the expense of increased area. The step response of the BQCM line driver is also shown in Fig. 4.27. The circuit features a slew rate of more than 1.2 V/μs.

The bandwidth of the BQCM line driver compensated with two 2pF capacitors is larger than 2.9 MHz for a 500Ω, 1nF load at the nominal 20 mA line current. The phase margin is greater than 55 degrees. Fig. 4.28 illustrates the dependence of the bandwidth to the output current. Because of the high transconductance of the bipolar transistors in the output stage, the sensitivity of the bandwidth to the line current is much smaller than that of the CQCM line driver.

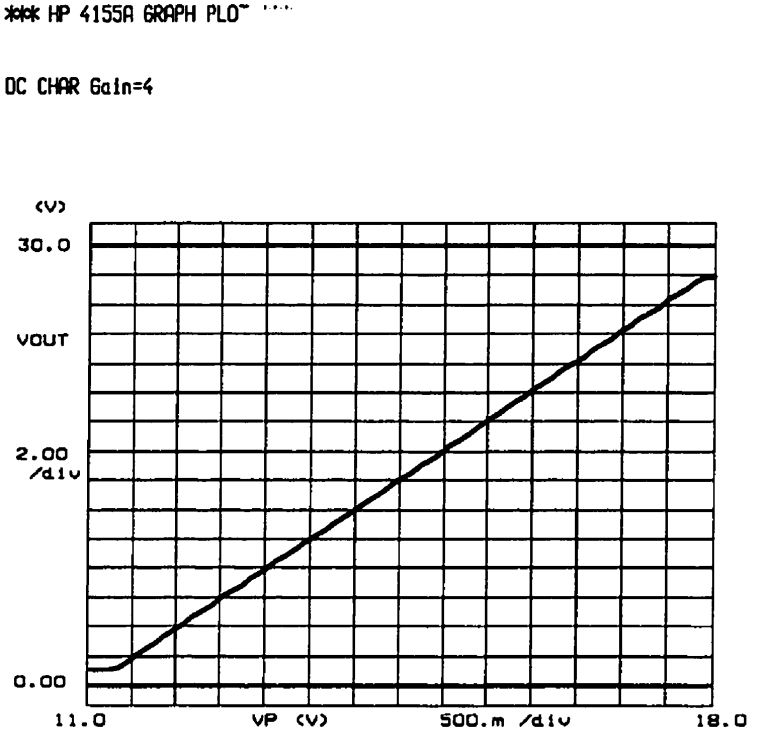


Fig. 4.26: DC characteristic of the BQCM line driver with a gain of 4

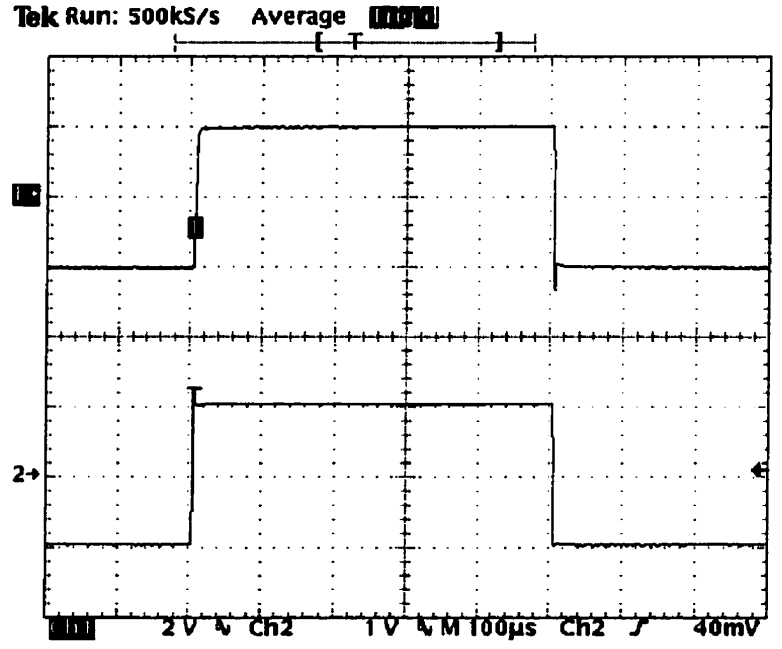


Fig. 4.27: Step response of the BQCM line driver, Upper trace: Ch1-Output, Lower trace: Ch2-Input

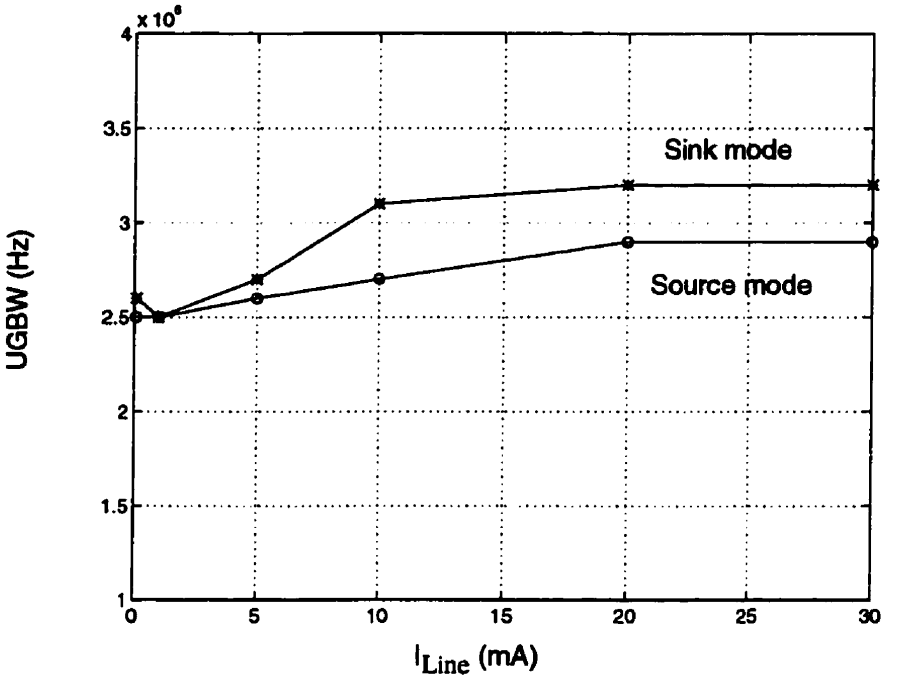


Fig. 4.28: Unity-gain bandwidth (UGBW) of the BQCM line driver vs. the output current

Compared to the CQCM line driver, the PSRR is also improved by 20 dB and the output impedance is decrease by a factor of 5 at higher frequencies which translates into 14 dB better longitudinal balance for the SLIC. This is a direct result of the superior frequency response provided by bipolar transistors. Measured characteristics of the BQCM line driver are summarized in Table 4.5. The overall discrepancy between the measured and simulated results is less than 20%.

The sensitivity of the quiescent current to process variations[1], obtained using Monte Carlo simulations is less than 15%. The smaller sensitivity of this design compared to that of the CQCM line driver is a result of using low voltage CMOS and bipolar devices in the QCM stage. The quiescent current variation also remains less than 20% over a wide range of temperatures (-40 to 125 °C).

1. A 10% tolerance for the length, width and threshold voltage of the high voltage devices was considered.

Table 4.8: BQCM line driver characteristics

Parameter	Post-layout Simulation	Measurement
Area		0.24 mm^2
Maximum Supply Voltage	30V	30 V
Maximum Output Current	30 mA	> 30 mA
Idle Current	890 µA	1.07 mA
Unity-Gain Bandwidth :		
Source Mode (I_{Load} > 10 mA)	3 MHz	> 2.7 MHz
Sink Mode (I_{Load} > 10 mA)	3.4 MHz	> 3.1 MHz
Power Supply Rejection Ratio :		
at 4 KHz	74 dB	< 68 dB
at 1 MHz	23 dB	< 19 dB
Output Impedance :		
at DC	0.15 Ω	< 0.19 Ω
at 10 KHz	0.2 Ω	< 0.26 Ω
Slew Rate	1.4 V/µs	> 1.2 V/µs
Total Harmonic Distortion for a 2Vp.,16 KHz metering signal	0.05%	< 0.07%
Output Swing	V_{sup} -2 V	V_{sup} -2.8 V

4.7 Floating-Current-Mirror Line Driver (FCM)

As mentioned in Chapter 3, the high voltage NMOS devices available in the BiCMOS process are susceptible to the weak avalanche breakdown effect which reduces their safe operating area (SOA) at high currents. As a result, the current density must be limited to avoid lowering the breakdown voltage. This translates into small gate-source voltage (less than 2V) and hence oversized transistors for driving high output currents. Meanwhile, the high voltage PMOS devices exhibit higher breakdown voltages with no weak avalanche breakdown effect at high current densities. Therefore, an output stage, made up of only high voltage PMOS devices can offer better performance and higher reliability.

With this objective in mind, a line driver was designed and implemented using a PMOS-only output stage [1,20]. The circuit uses smaller devices at the output and features a very well-controlled quiescent current with less sensitivity to the component matching as compared to other complementary output stages. A detailed description of this circuit is presented in this chapter.

4.7.1 Circuit Description

The structure of the floating-current-mirror (FCM) line driver is illustrated in Fig. 4.29. The class AB output stage consists of only HV-PMOS devices M1 and M2. The pull-up transistor M1 operates in a common-source configuration while M2 is used as a source-follower buffer in the pull-down path. The quiescent current in the output stage is controlled by the floating current mirror M4 and M2.

In order to explain the circuit operation, a simplified diagram of the output stage is illustrated in Fig. 4.30. With no load at the output, the quiescent current I_q in transistors M1 and M2 is controlled by the floating current mirror M2 and M4. The feedback loop made up of the opamp OP1 and transistor M1, forces the voltage on node A, V_A to be equal to the

output voltage V_{out} . As a result, the gate-source voltage of M2, (V_{gs2}) and M4 (V_{gs4}) are equal

$$V_{gs2} = V_{gs4} \tag{4.12}$$

The quiescent current I_q in the output transistor M2 (as well as M1) would then be determined by the reference current I_{ref} and the aspect ratios of M2 and M4

$$I_q = \frac{(W/L)_{M2}}{(W/L)_{M4}} I_{ref} \tag{4.13}$$

Therefore, I_q only depends on the reference current I_{ref} and the sizes of M1 and M2. The role of the feedback loop is to control and stabilize the quiescent current. Unlike class-B

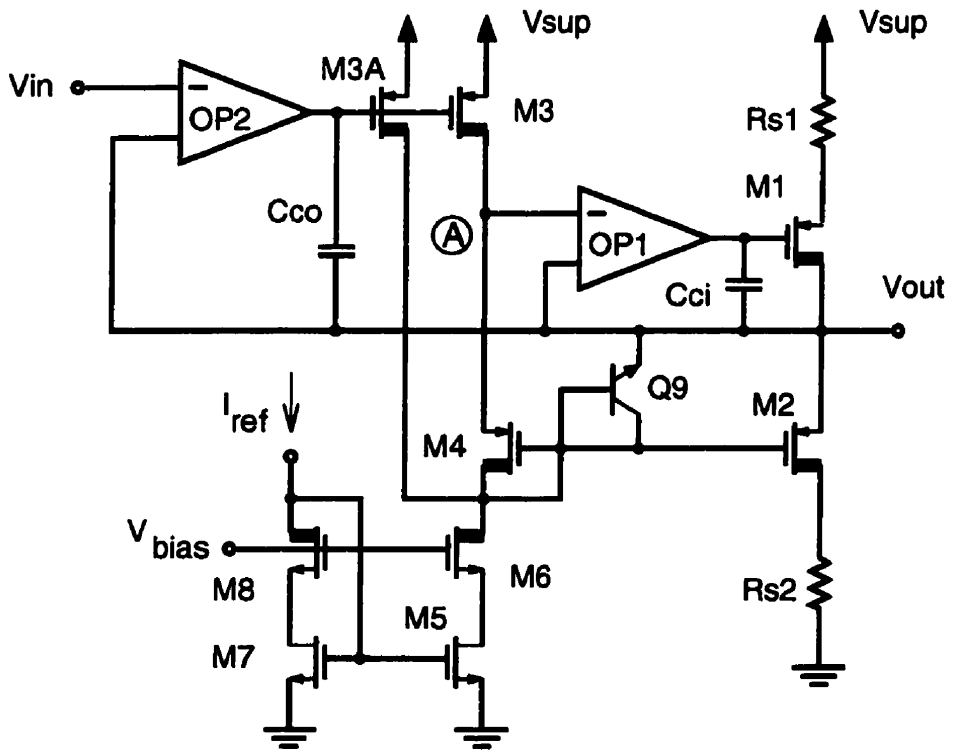


Fig. 4.29: Schematic diagram of the FCM line driver

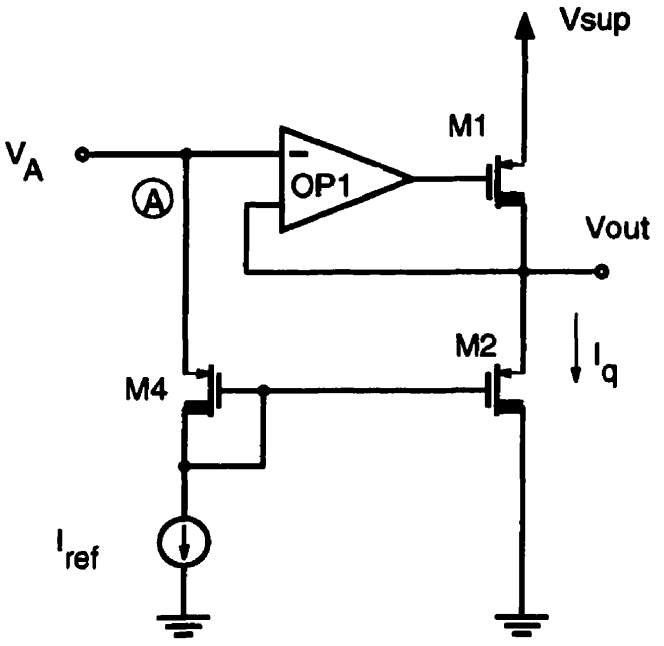


Fig. 4.30: Simplified diagram of the FCM output stage

feedback structures [10], the opamp's offset voltage has negligible effect on the accuracy of I_q because it is much smaller than the gate-source voltage of M2, V_{gs2}.

When the line driver is sourcing current into the line, the opamp OP1 provides adequate gate-source voltage for M1 keeping V_A and V_{out} equal. Therefore, M1 can supply currents much larger than I_q . At the same time, the current in M2 is limited to I_q by the floating current mirror.

In order to sink current from the load, V_A goes down and M2 operates as a source-follower buffer pulling the output voltage V_{out} down. While the large load current I_{out} passes through M2, the current in M4 remains I_{ref}. Because I_{out} is larger than I_q

$$I_{out} > I_q = \frac{(W/L)_{M2}}{(W/L)_{M4}} I_{ref} \tag{4.14}$$

as a result

$$V_{gs2} > V_{gs4} \tag{4.15}$$

Therefore, the positive input of opamp OP2 would be at a higher voltage (V_{out}) than the negative input (V_A). The output voltage of OP2 would then rise to V_{sup} and turns M1 off so there would be no wasted current in the pull-up path during load current sink.

Because of equation 4.15, V_{out} does not follow V_A while sinking load current. This results in an asymmetrical transfer characteristic as shown in Fig. 4.31-a. When the pull-down path is active, the transfer curve diverges from the ideal $V_A = V_{out}$ line (dotted line in Fig. 4.31-a) as the load current increases. This effect does not appear in the pull-up part of the characteristic because of the local feedback loop around M1. To fix this problem, another feedback loop is required to correct the transfer characteristic.

The role of OP2 and the global feedback loop is to linearize the transfer characteristics and force V_{out} to follow the input voltage V_{in} (Fig. 4.29) over the whole voltage range. The combination of OP2 and M3 acts as a gain stage in the loop adjusting V_A such that V_{out} and

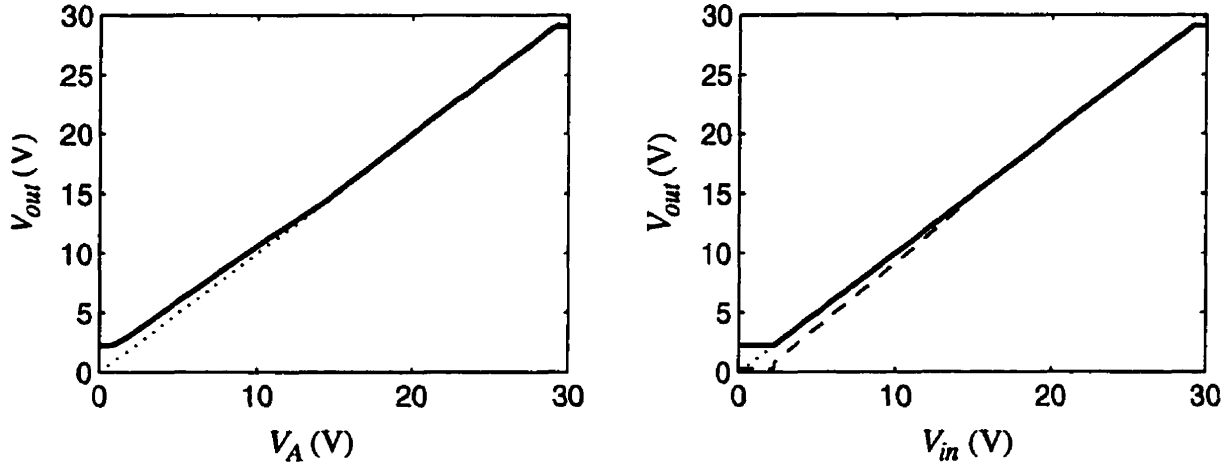


Fig. 4.31: DC transfer characteristics of the FCM output stage: a) from V_A to V_{out} (The dotted curve shows the $V_{out} = V_{in}$ line, b) from V_{in} to V_{out} (V_A is also shown in dashed line)

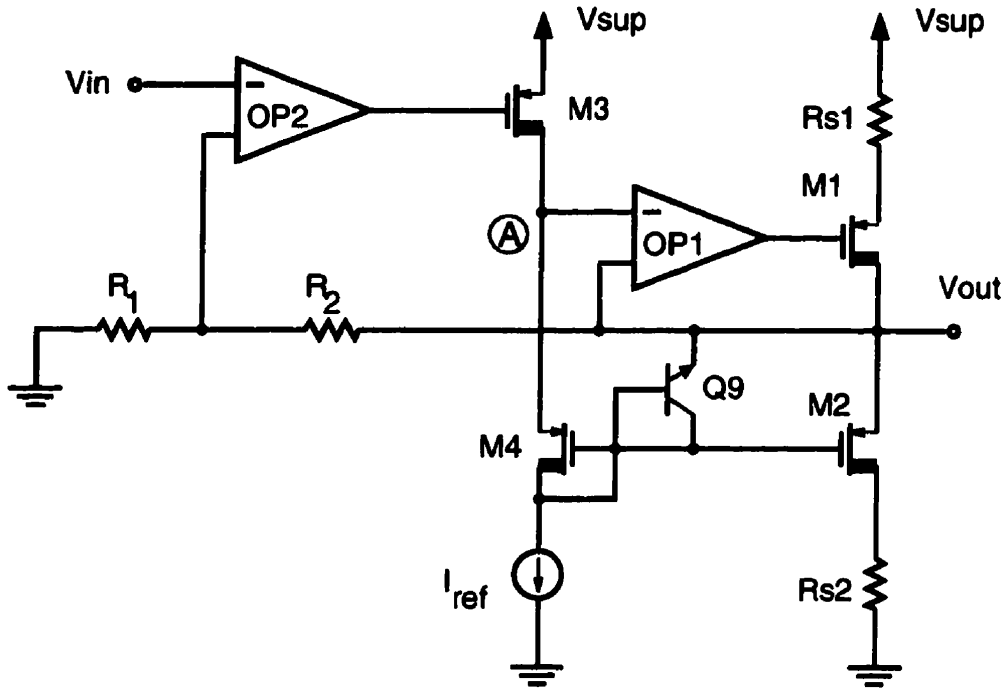


Fig. 4.32: FCM output stage with a gain of more than one

V_{in} are equal. The whole circuit can then be considered as an amplifier in a unity-gain configuration. The effect of the global feedback loop on the transfer characteristics of the line driver is shown in Fig. 4.31-b. The transfer curve (solid line) now lies on the $V_{out} = V_{in}$ line (dotted line) by predistorting V_A (dashed line) using the second feedback loop.

Although the circuit of Fig. 4.29 provides a gain of one from V_{in} to V_{out}, higher gains can be achieved by using a resistive feedback as illustrated in Fig. 4.32. In this figure, the output stage is used in a non-inverting amplifier configuration whose gain can be determined as

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{4.16}$$

The resistors Rs1 and Rs2 are small current sense resistors that can be used to monitor the line current for SLIC's supervision functions[11].

The output voltage range of the line driver is limited by the on-resistance of M1 on the high side and the gate-source voltage of M2 on the low side. Assuming the minimum required voltage across the I_{ref} current source is V_{min}, the output voltage range would be

$$V_{min} + V_{gs_2} < V_{out} < V_{sup} - V_{sat_1} - V_{Rs1} \tag{4.17}$$

where V_{sat1} is the drain-source saturation voltage of M1 and V_{Rs1} is the voltage drop across Rs1.

In order to increase the output voltage range large size ratios for M1 and M2 and small resistance for Rs1 must be used to reduce V_{sat1}, V_{gs2} and V_{Rs1}, respectively. V_{Imin} can also be minimized by using a large swing cascode current source (M5-M8) as shown in Fig. 4.29. The low voltage transistors M5 and M7 provide superior matching while high voltage devices M6 and M8 handle large operating voltages. The cascode current source also decreases the variation of the reference current I_{ref} with respect to the large (almost rail to rail) voltage swings of V_A.

The gates of the high voltage devices must be protected against large voltage transients. This is the function of the diode-connected transistor Q9 which is normally off. Similarly, to protect M1 and M3, the output voltage of OP1 and OP2 must be limited within 5V from the positive supply voltage. This feature is implemented internally in the opamps as will be explained later in this chapter.

4.7.2 Device Parameters and Biasing

Table 4.5 shows the parameters of devices in the output stage. The quiescent current in the output transistors is determined by a 1:10 size ratio between the floating current mirror M4 and M2. As illustrated in Fig. 4.29, another current path through M3A is added in parallel with M3 which passes part of the current I_{ref}. This technique results in a lower quiescent current without decreasing I_{ref} as will be explained shortly.

The oversized output transistors involve large gate capacitances that require sufficient driving current specially during fast voltage transients. In the pull-up path, the opamp OP1 provides sufficient gate drive for M1. However, in the pull-down path I_{ref} is the only driving current for M2. Although larger I_{ref} results in faster switching of M2, according to equation 4.13, it would increase the quiescent current of the output stage by the size ratio of M1 and M2. It is not desirable to compensate this effect by reducing the size factor in equation 4.13 because a large device would then be required for M2 adding more parasitic capacitance to node A. A novel solution to overcome this trade-off is to keep I_{ref} large but pass only a part of it through the floating current mirror (M4). As shown in Fig. 4.29, transistor M3 is divided by a 1:4 ratio (M3, M3A) providing a bypass current path through M3A. As a

Table 4.9: Device parameters of the FCM line driver

Device		Parameter[1]
High Voltage MOS	M1,M2	1280μ/3μ
	M3	64μ/3μ
	M4	128μ/3μ
	M3A	256μ/3μ
	M6,M8	50μ/3μ
Low Voltage MOS	M5,M7	50μ/1.2μ
Low Voltage NPN	Q9	4x0.8 μ^2
Resistors	Rs_1,Rs_2	16Ω
Capacitors	CC1	1pF
	CC2	3pF

1. Aspect ratio for MOS device, emitter area for bipolars

result, only one fifth of I_{ref} passes through M2 which controls the quiescent current I_q . Consequently, with a size ratio of 1:10 between M4 and M2

$$I_q = 2 \cdot I_{ref} \tag{4.18}$$

4.7.3 Internal Opamps

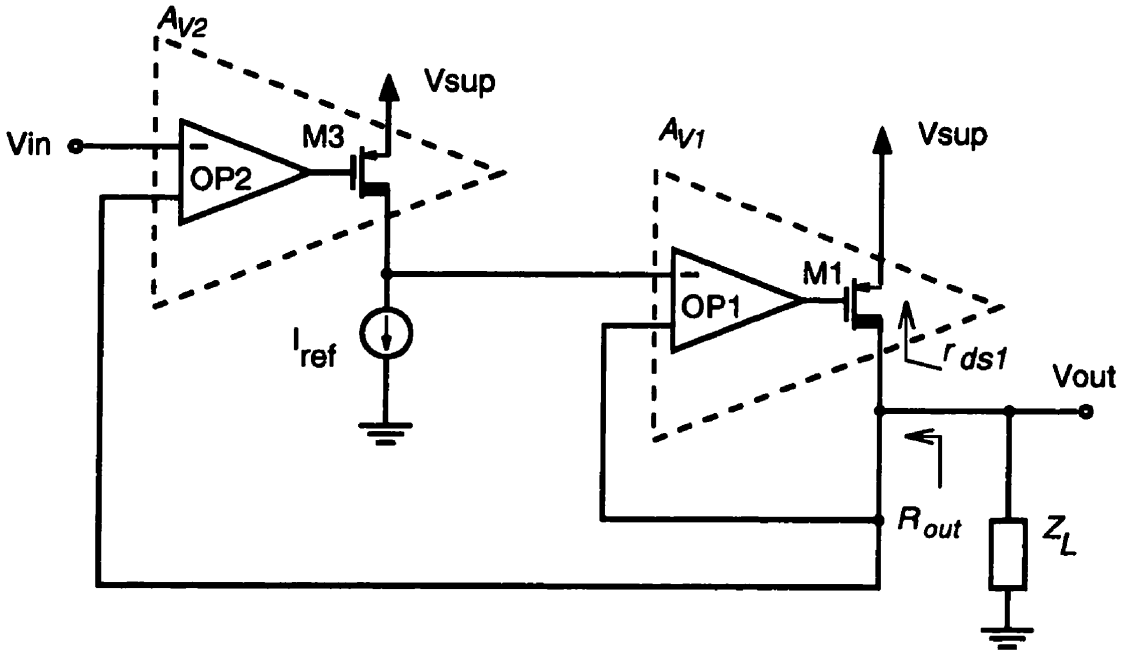
The internal opamps OP1 and OP2 are the main gain elements inside the feedback loops. The design objective is to obtain adequate loop gain by using minimum bias currents in conformity with the power constraint. Therefore, it is necessary to carefully estimate the minimum required gain for the feedback loops.

The gain constraint on the opamps is imposed by the output impedance requirement for the whole line driver. The feedback loops around the output stage reduce the output impedance by dividing the output resistance of transistors M1 and M2 by the loop gain. Simplified models for pull-up and pull-down paths are shown in Fig. 4.33. When the line driver sources current into the load, the pull-up path is active (Fig. 4.33-a) and the output impedance can be estimated as

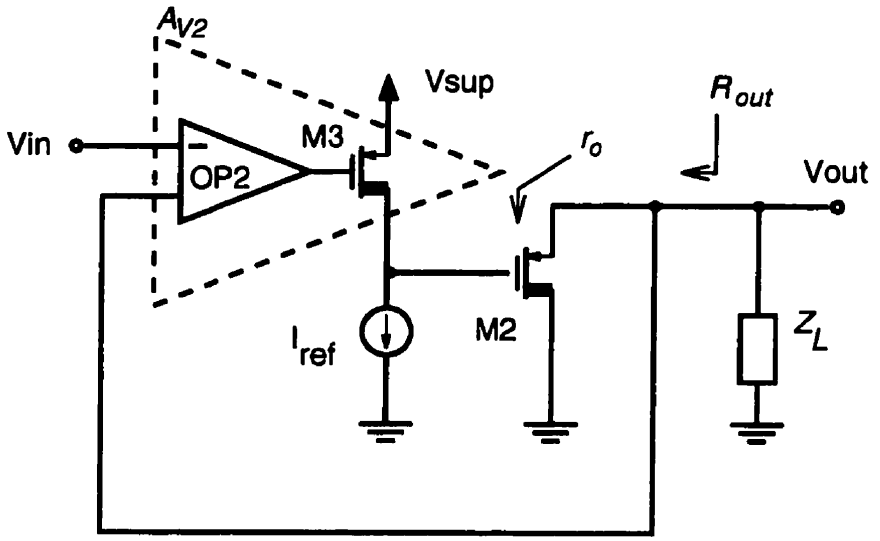
$$R_{out} \cong \frac{r_{ds1}}{A_{V1} \cdot A_{V2}} \tag{4.19}$$

where r_{ds1} is the output resistance of M1 in the active region and A_{V1} and A_{V2} are the combined gains of OP1 plus M1 and OP2 plus M3, respectively. Typical value for r_{ds1} varies between 100KΩ to 1MΩ for different line currents. In order to satisfy the output impedance requirement (Chapter 2), R_{out} must be less than 0.2Ω. Therefore, the gain factor $A_{V1}.A_{V2}$ must be greater than 10^7 or 140 dB.

On the other hand, in the pull-down path (Fig. 4.33-b) there is only one feedback loop around the output transistor M2. At first, it might seem that R_{out} is much higher in this case



(a)



(b)

Fig. 4.33: AC models for FCM output stage for a) pull-up and b) pull-down paths

because only A_{V2} is in the loop. However, the output transistor M2 is operating in a source - follower configuration. Therefore, its output impedance r_o is $r_{m2}=1/g_{m2}$ which is much smaller than r_{ds1} in the previous case. The output impedance R_{out} can then be expressed as

$$R_{out} \cong \frac{r_{m2}}{A_{V2}} \tag{4.20}$$

Typical value for r_{m2} is less than 100Ω. Obviously, the output impedance requirement can be met with A_{V2} greater than 10^3 or 60 dB. Therefore, considering both equations 4.19 and 4.20, a gain of 70 dB for each feedback loop (A_{V1} and A_{V2}) is a reasonable guideline for this design.

The circuit diagram of internal opamps (OP1,OP2) is shown in Fig. 4.34. Transistor sizes are provided in Table 4.5. The circuit is a single stage OTA with cascode high voltage transistors (M11-M15) to handle the high voltage swings and boost up the gain. Because the input voltages of opamps can swing over the whole supply range, high voltage PMOS devices are the only suitable choice for the input stage (M1,M2). The bias current for this stage is provided by a large-swing cascode current mirror (M9,M10,M15,M16). With V_{bu} biased at V_{sup} - V_{gs15} - V_{sat9} , a wide input range can be achieved as

$$0 < V_{in} < V_{sup} - V_{sat9} - V_{sat15} - V_{gs1} \tag{4.21}$$

where V_{sat9} is the saturation voltage of M9, V_{gs1} and V_{gs15} are the gate-source voltages of M1 and M15, respectively. Meanwhile, the outputs of OP1 and OP2 must be able to drive the gates of M3 and M4. Therefore, their voltage range must be limited to within 5V from the positive supply rail to protect the gates of M3 and M4. The function of Q1 is to limit the output range between

$$V_{sup} - V_{bb} - V_{be} < V_{out} < V_{sup} - V_{sat1} \tag{4.22}$$

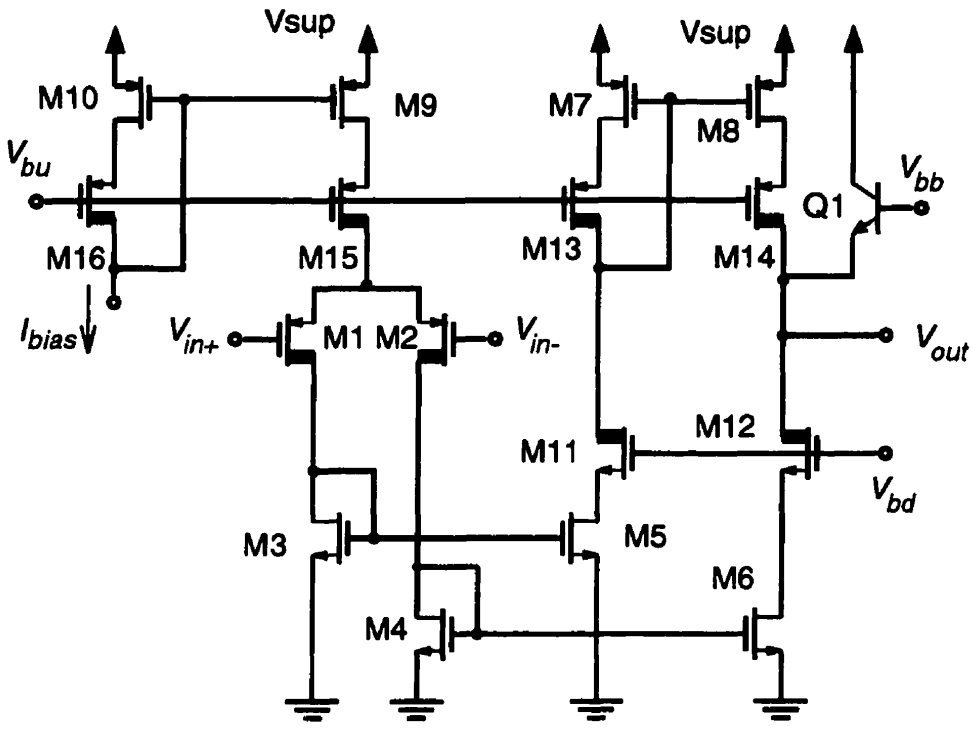


Fig. 4.34: Schematic diagram of the internal opamps OP1 and OP2

Table 4.10: Device parameters of the internal opamps

Device		Parameter[1]
Low Voltage MOS	M3,M4	5μ/1.2μ
	M5,M6	15μ/1.2μ
	M7-M10	30μ/1.2μ
High Voltage MOS	M1,M2,M11-M16	84μ/3μ
Low Voltage NPN	Q1	4x0.8 μ^2

1. Aspect ratio for MOS device, emitter area for bipolars

when V_{bb} is set to

$$V_{bb} = V_{sup} - 5 \tag{4.23}$$

In these equations, V_{bb} is the base-emitter voltage of Q1 and V_{sat1} is the saturation voltage of M1.

The capability of compensation by load capacitance, is an advantageous feature of OTA structure in this design. This allows the use of the parasitic gate capacitances of M1 and M3 for compensating OP1 and OP2. Note that the opamp must provide enough output current to charge and discharge these capacitances at a high slew rate. For this reason, the lower current mirrors (M3,M5 and M4,M6) have a size ratio of 1:3 to scale up the output current as well as the gain.

The opamps are optimized for maximum gain with limited bias current. With Ib=20μA, the total bias current of each opamp is 100 μA. This provides more than 80 dB gain and 20MHz bandwidth as shown in Fig. 4.35 .The load capacitance is 3pF which is the same as the gate capacitance of M1.The large bandwidth of the opamp would facilitate the compensation of the whole line driver.

4.7.4 FCM Stage Frequency Response and Compensation

The floating buffer line driver has two nested feedback loops and two different signal paths for pull-up and pull-down functions. Both of the feedback loops must remain stable for each signal path to guarantee the overall stability for every state of operation. This problem is investigated in this section starting with the stability of the inner loop followed by studying the frequency behavior of the outer loop for both pull-up and pull-down paths.

A simplified diagram of the inner loop is shown in Fig. 4.36-a. There are two signal paths between the input and output in this loop as shown in the block diagram of Fig. 4.36-

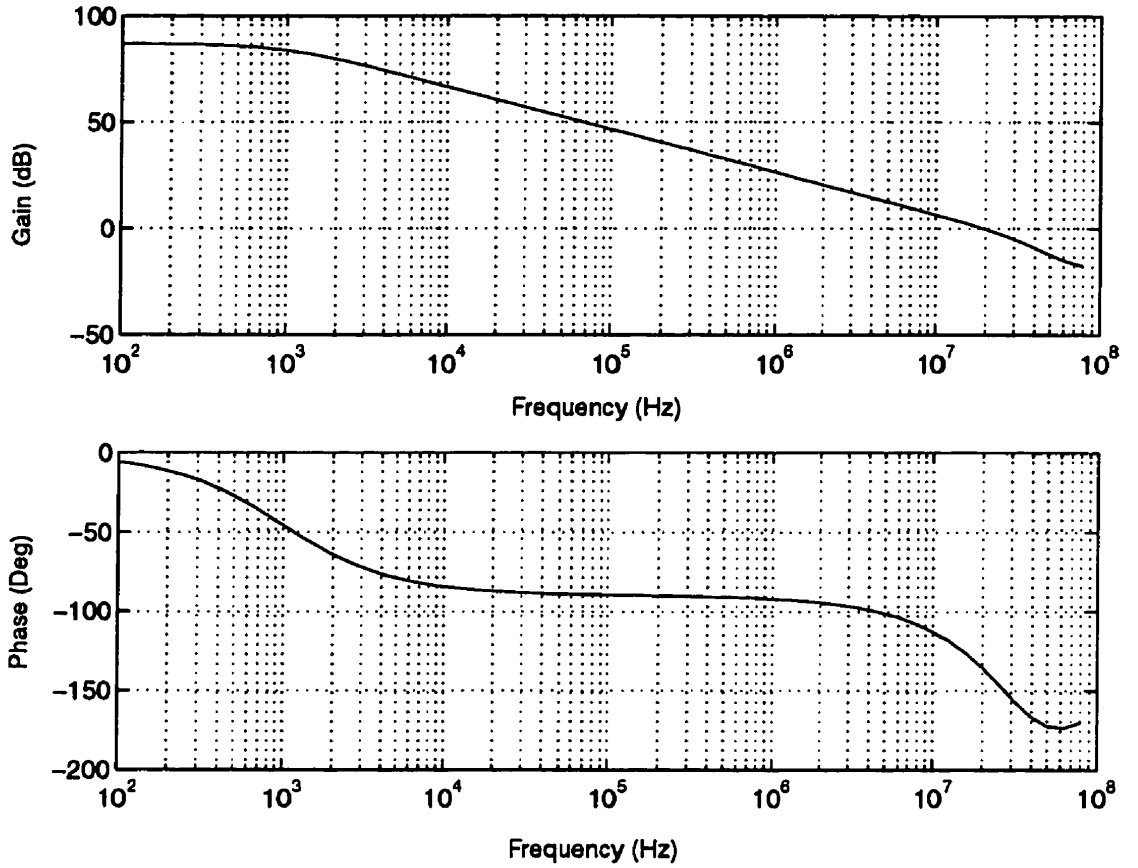
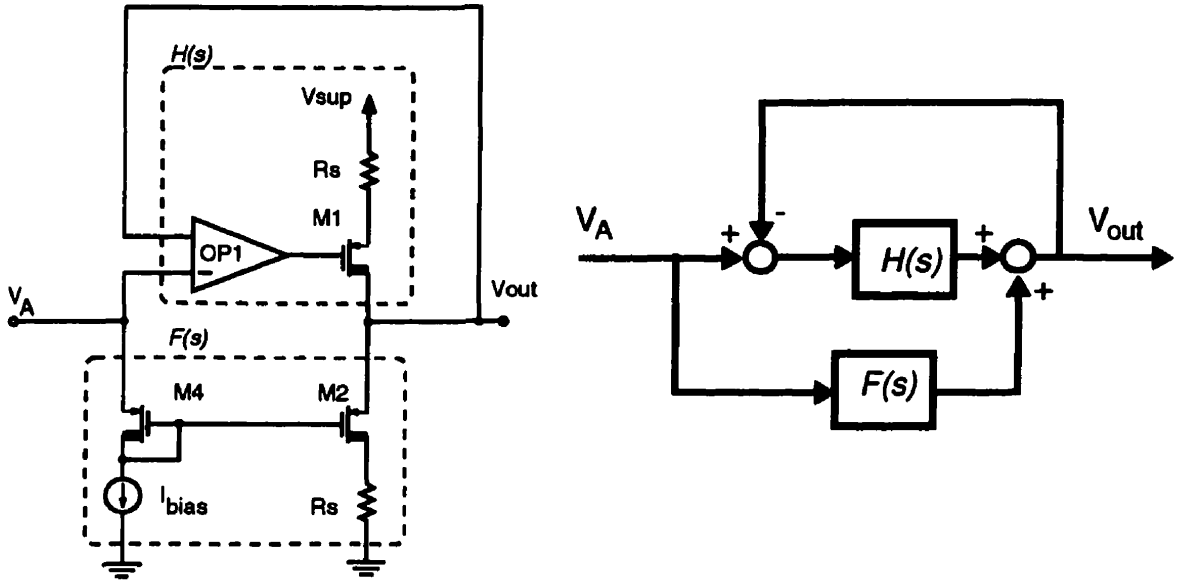


Fig. 4.35: Frequency response of the internal opamps (Compensated with 3pF load capacitance)

b. The main signal path is modeled as *H(s)* which represents the open loop transfer function of the pull-up path including OP1 and M1. This is a conventional pole-splitting loop compensated by the Miller capacitor Cci (Fig. 4.29). However, there is also another feedforward path through the floating buffer (M2,M4) that affects the frequency behavior of the loop. This signal path, shown as *F(s)*, can contribute to stability and increase the bandwidth as will be explained below.

As shown in Fig. 4.36-b, the transfer function of the output stage from V_A to V_{out} can be written as

$$\frac{V_{out}(s)}{V_A(s)} = \frac{H(s)+F(s)}{1+H(s)} \tag{4.24}$$



(a) (b)

Fig. 4.36: Inner feedback loop of the FCM output stage: a) AC signal paths and b) Block diagram

The compensated *H(s)* would have a single-pole frequency response that can be approximated as $H(s) \equiv w_u/s$ near its unity-gain frequency w_u. Assuming the feedforward buffer has a gain of 1 with a bandwidth larger than w_u , the transfer function would become

$$\frac{V_{out}(s)}{V_A(s)} \equiv \frac{\frac{w_u}{s} + 1}{1 + \frac{w_u}{s}} \tag{4.25}$$

equation 4.25 shows that the feedforward path adds a zero to the transfer function at w_u . This zero boosts up the frequency response and improves the phase margin by providing positive phase shift at frequencies near w_u.

In order to verify the assumption of $F(s) = 1$ for frequencies below w_u , a simple model of the feedforward path through M4 and M2 is provided in Fig. 4.37. In this model,

r_d is the resistance of the diode connected transistor M2, C_{gd} and C_{gs} are the gate-drain and gate-source capacitances of M4, g_m is its transconductance and R_L and C_L are the load impedances.

The effect of C_{gd} is to form a low-pass circuit with r_d and to cause the gain to decrease at very high frequencies. Since both r_d and C_{gd} are small, their effect appears at frequencies much higher than other poles and zeros of the circuit. Therefore, C_{gd} is ignored in calculations for simplicity. The transfer function of the circuit can then be calculated as

$$F(s) = \frac{g_m R_L\left(1+\frac{C_{gs}}{g_m}s\right)}{(1+g_m R_L)\left[1+\left(\frac{(r_d+R_L)C_{gs}+R_L C_L}{1+g_m R_L}\right)s+\frac{r_d R_L C_{gs} C_L}{1+g_m R_L}s^2\right]} \tag{4.26}$$

As a result, the low frequency gain of this stage is

$$F_o = \frac{g_m R_L}{(1+g_m R_L)} \tag{4.27}$$

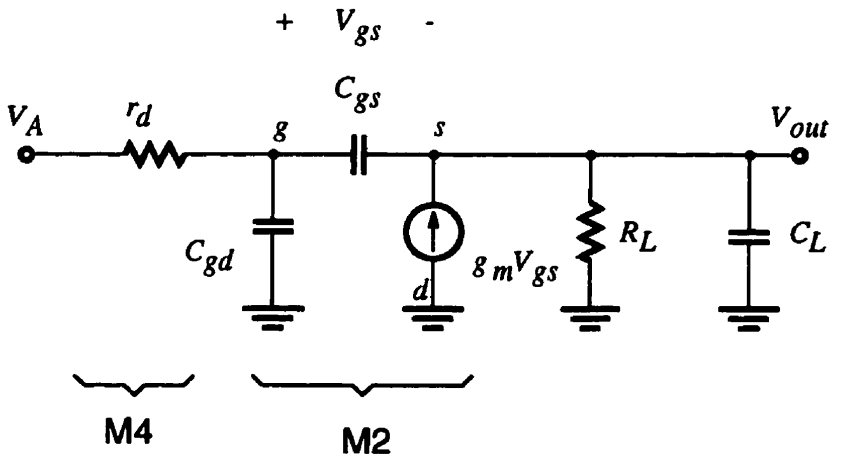


Fig. 4.37: AC model of the feedforward path

which is almost unity when $g_m R_L >> 1$. The zero and poles can be approximated as

$$z = -\frac{g_m}{C_{gs}} \tag{4.28}$$

$$p_1 = \frac{1 + g_m R_L}{(r_d + R_L) C_{gs}} \tag{4.29}$$

$$p_2 = \frac{1 + g_m R_L}{R_L C_L} \tag{4.30}$$

With both z_1 and p_1 located at high frequencies, the bandwidth is limited by p_2 as a result of large load capacitance C_L. However, with maximum load (500Ω and 1nF) and a worst case gain factor of $g_m R_L$ =10, p_2 would be at a frequency higher than 3MHz. Therefore, the assumption of *F(s)* = 1 in the desired frequency band is reasonably valid up to that frequency. The simulated frequency response of *F(s)* is illustrated in Fig. 4.38. It confirms that *F(s)* has a gain of almost unity and a bandwidth of 3 MHz, larger than the target 1MHz bandwidth for the line driver.

The inner loop stability can be guaranteed by compensating *H(s)* using a Miller capacitor, Cci. The frequency response of the circuit from V_A to V_{out} with compensated *H(s)* is presented in Fig. 4.39. The dashed line is the response of *H(s)* alone while the solid line presents the response of the combination of *F(s)* and *H(s)*. The effect of *F(s)* has appeared as more positive phase at high frequencies and hence increased phase margin.

With the inner feedback loop compensated, the stability of the whole output stage is now investigated. Although the main signal paths are different in current source and current sink modes of operation, their frequency behavior is almost similar. Referring to Fig. 4.36, in current sourcing mode, when the pull-up path is active, both *H(s)* and *F(s)* are in the signal path. The combination of the compensated *H(s)* and *F(s)* with the unity feedback

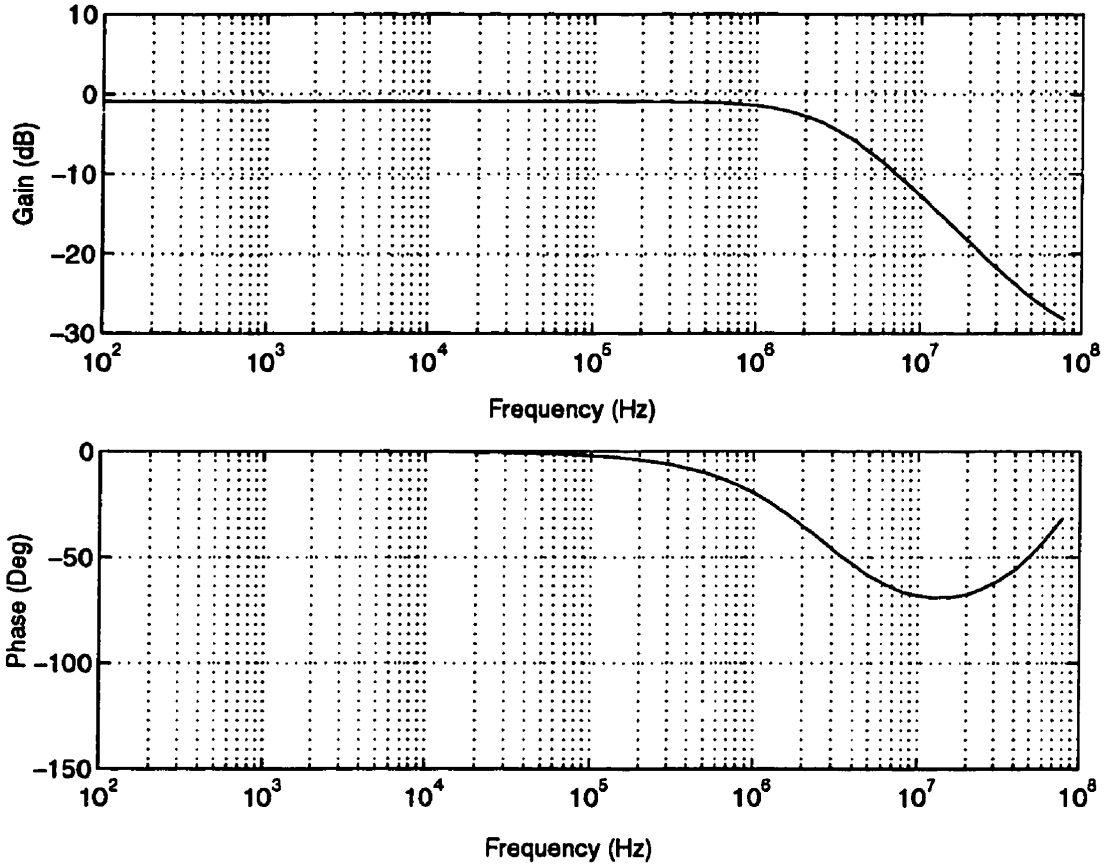


Fig. 4.38: Frequency response of feedforward path *F(s)*

loop around OP1 acts as a buffer with a gain of 1 and a bandwidth of ω_0 between V_A and V_{out}. The frequency response of this buffer is shown with solid lines in Fig. 4.40.

In current sinking mode, the pull-up transistor M1 is off and only *F(s)* is in the loop. Therefore, the frequency response (dashed lines in Fig. 4.40) is identical to that of *F(s)* (Fig. 4.38). However, in both modes of operation, the output stage between node A and the output can be approximated as a unity gain buffer. As a result, the simple model of Fig. 4.41 can be used for compensating the whole line driver in both current sink and current source modes of operation.

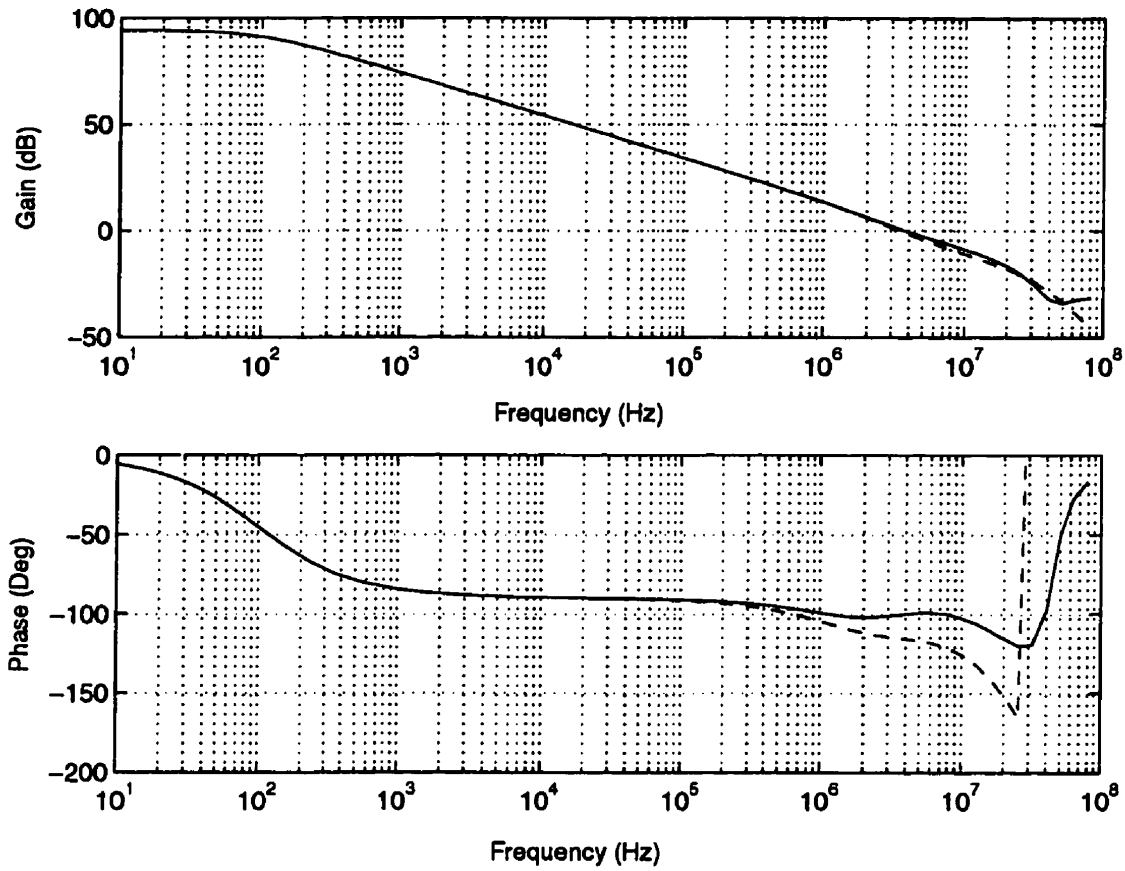


Fig. 4.39: Frequency response of the output stage from V_A to V_{out} with feedforward (solid line) and without feedforward path (dashed line)

A Miller compensation technique can be employed in this circuit by simply adding a capacitor across the gain stage M3. However, it is more advantageous if the compensation capacitor (Cco) closes the loop around both the gain stage M3 and the buffer stage. In this way, the pole-splitting effect of Cco would also affect the parasitic poles of the buffer stage, pushing them to higher frequencies. Fig. 4.42 illustrates the overall frequency response of the line driver, compensated with a 3pF capacitor. The simulated bandwidth is more than 4.5 MHz with more than 45° phase margin.

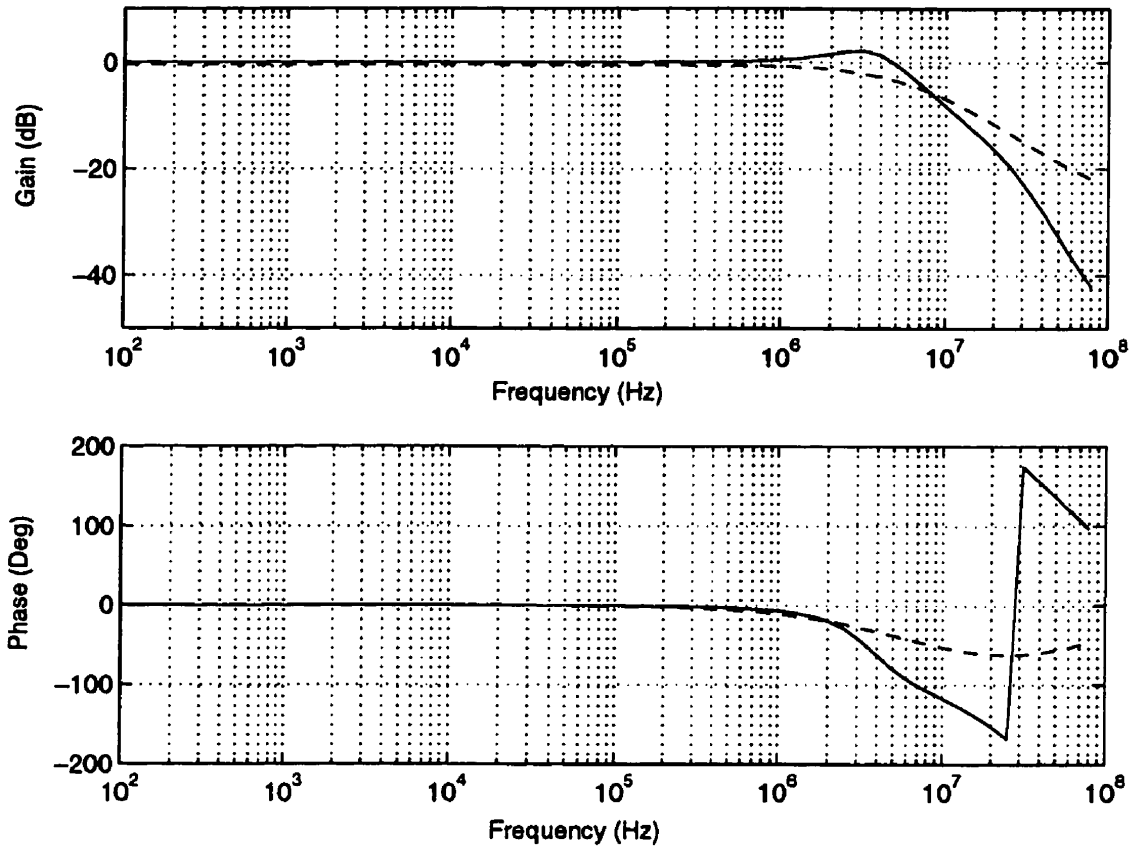


Fig. 4.40: Frequency response of the inner feedback loop with a unity-gain feedback

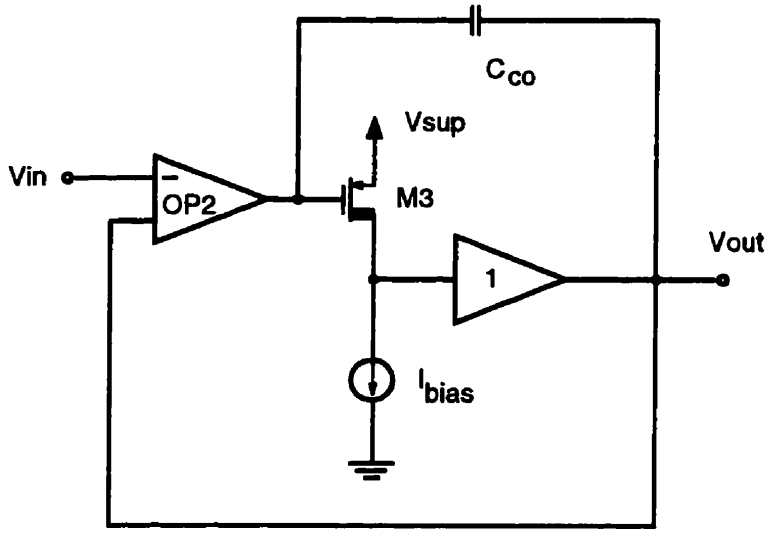


Fig. 4.41: AC model for compensating the outer feedback loop

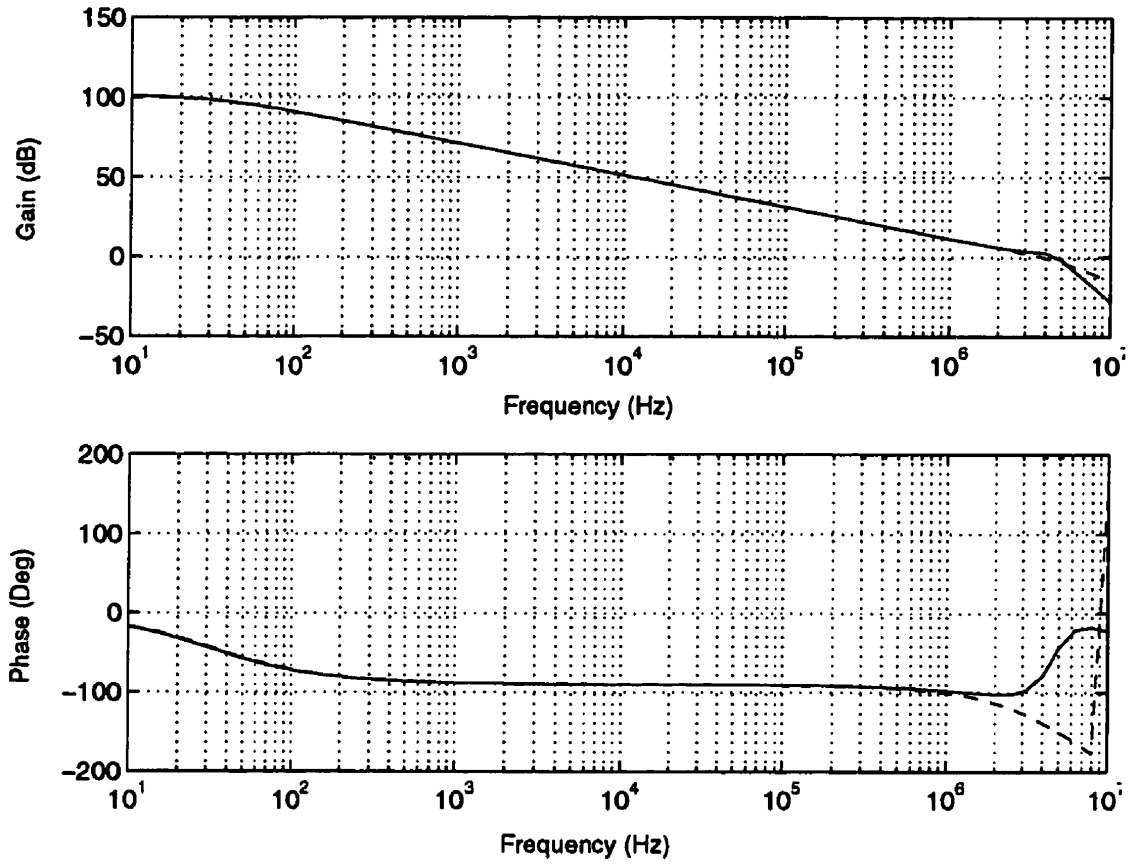


Fig. 4.42: Overall frequency response of the compensated FCM line driver

4.7.5 Experimental results

A micrograph of the FCM line driver implemented in BATMOS-5 process is illustrated in Fig. 4.43. This circuit occupies an area of 0.34 mm^2 including the compensation capacitors. The closed-loop DC transfer characteristic of the line driver is shown in Fig. 4.44. As shown in the figure, the output voltage range extends within 0.75V and 2V from the positive and negative supply rails, respectively. The low-side margin is higher than the high-side one because of the source-follower configuration of the pull-down path in the output stage. The step response of the line driver is illustrated in Fig. 4.45. The Slew rate of the line driver is greater than 2.2 V/μs.

The unity-gain bandwidth of the line driver is 3.6 MHz with more than 45° phase margin at the nominal 20mA line current. The dependence of the bandwidth on the line current is illustrated in Fig. 4.46. The bandwidth is much less sensitive to the load current as compared to the QCM circuits discussed in the previous chapter. The reason is that unlike the complementary output stages, the output stage in this design is a wideband buffer whose bandwidth is not directly dependent to the transconductance of the output devices. Therefore the modulation of the transconductance of the output devices with the load current has minimal effect on the overall frequency response of the circuit. .

The line driver features a PSRR of more than 70 dB in the voice band and an output impedance of less than 0.14Ω . Table 4.5 summarizes the characteristics of the line driver.

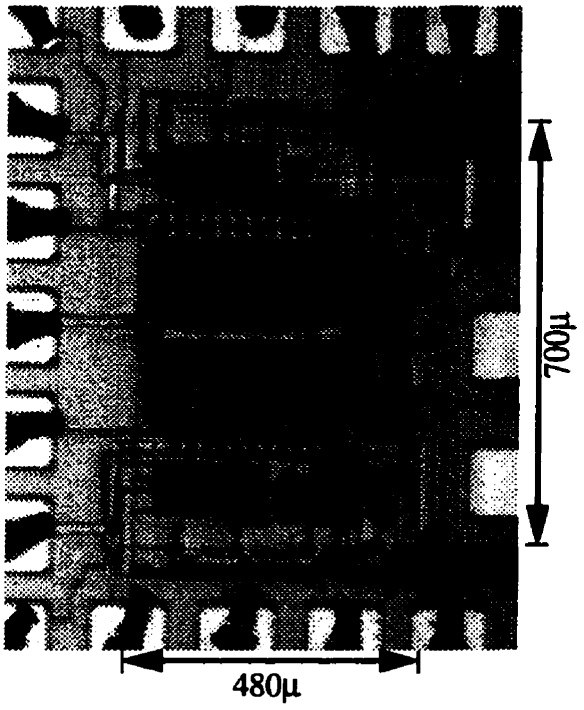


Fig. 4.43: Micrograph of the FCM line driver

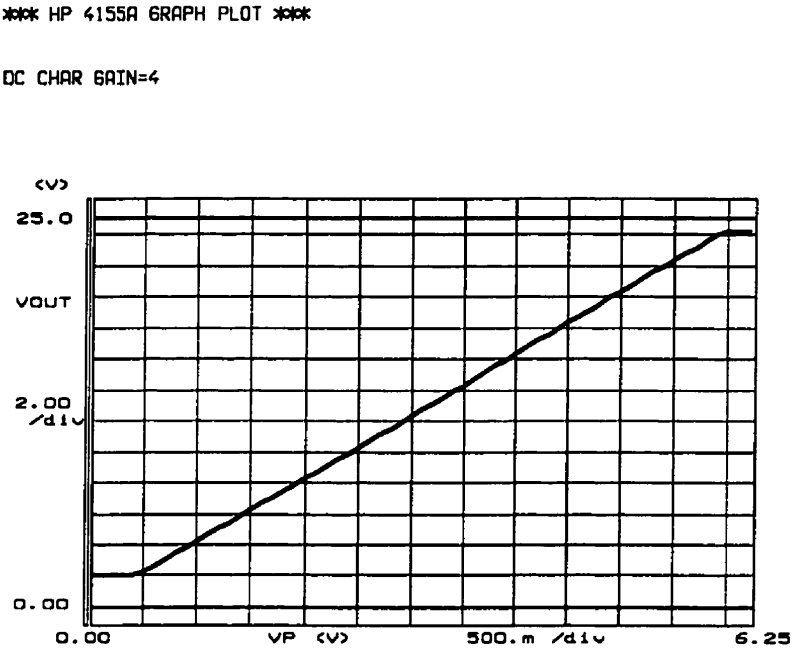


Fig. 4.44: DC characteristic of the FCM line driver (with a gain of 4)

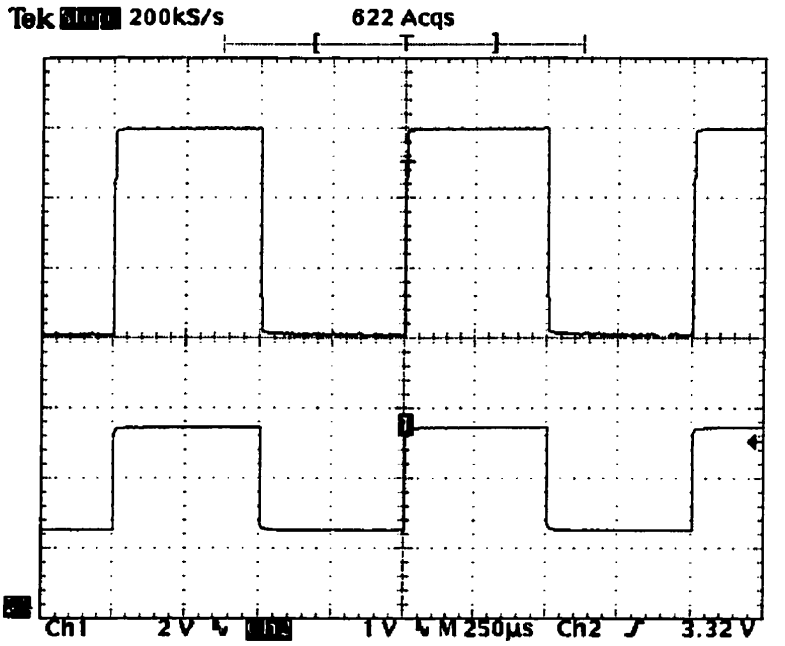


Fig. 4.45: Step response of the FCM line driver, Upper trace: Ch1-Output, Lower trace: Ch2-Input

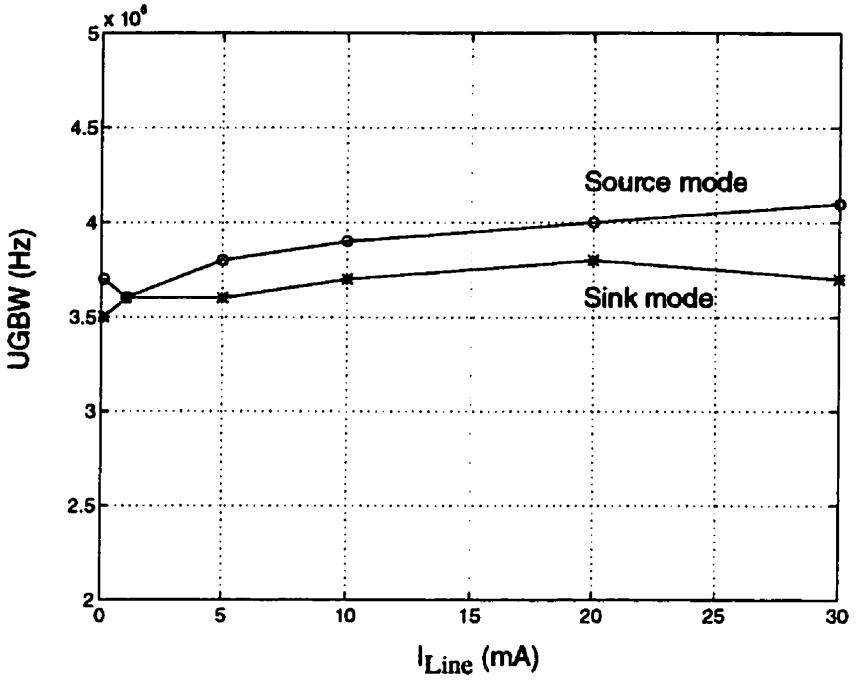


Fig. 4.46: Unity-gain bandwidth of the FCM line driver vs. the output current

The internal quiescent current of the line driver is limited to 600μA. As a result, the maximum power dissipation would be no larger than 15 mW. The quiescent current is much less sensitive to process and temperature variations. Monte Carlo simulations were performed to investigate the sensitivity of the circuit to process variations. Simulation results exhibited less than 5% variation in the quiescent current[1]. This is an advantage of using a feedback control loop to stabilize the quiescent current. Also simulation results for a wide temperature range (-40 to 125 °C) confirmed the stability of the quiescent current within 10% of its nominal value.

1. A 10% tolerance for the length, width and threshold voltage of the high voltage devices was considered.

Table 4.11: FCM line driver characteristics

Parameter	Post-layout Simulation	Measurement
Area		0.34 mm^2
Maximum Supply Voltage	30V	30 V
Maximum Output Current	30 mA	> 30 mA
Idle Current	520 µA	600 µA
Unity-Gain Bandwidth :		
Source Mode (I_{Load} > 10 mA)	4.5 MHz	> 3.8 MHz
Sink Mode (I_{Load} > 10 mA)	4 MHz	> 3.6 MHz
Power Supply Rejection Ratio :		
at 4 KHz	81 dB	> 70 dB
at 1 MHz	33 dB	> 22 dB
Output Impedance :		
at DC	0.01 Ω	< 0.1 Ω
at 10 KHz	0.1 Ω	< 0.14 Ω
Slew Rate	4 V/µs	> 2.2 V/µs
Total Harmonic Distortion for a 2Vp.,16 KHz metering signal	0.08 %	< 0.1 %
Output Swing	V_{sup} -2.4 V	V_{sup} -3 V

4.8 System Integration

Using the implemented building blocks, the complete high voltage front-end of the short loop SLIC was realized based on the proposed architecture in Chapter 2. The overall performance of the system is determined by the performance of the line drivers. While satisfying the 30mA maximum loop current, the system exhibits a wide bandwidth of 2 to 3.7 MHz (depend on the line driver type) which is very attractive for DSL applications. The whole high voltage front-end requires only $1mm^2$ of area leaving ample room for low voltage circuits on a single chip SLIC. The worst case power dissipation remains less than 70mW at maximum 30V supply voltage which is a remarkable advantage for the final integration. Careful isolation between low voltage and high voltage portions of the circuits using substrate contact and ground rings were effective in reducing the noise and crosstalk. Also no latch-up condition was observed for any of the circuits under all operating conditions tested.

4.9 Summary

In this chapter, the design of the high voltage front-end of the short loop SLIC was presented. The fully differential preamplifier featuring a novel common-mode feedback circuit provides a wide bandwidth with minimum power and area. The new concept used in the common-mode feedback circuit is based on the use of the output resistance of high voltage devices as a sense resistor resulting in a very compact and low power solution.

This chapter also demonstrated the feasibility of implementing high voltage line drivers in a low voltage BiCMOS process. The main challenge of the line driver design arises from the problem of controlling the internal current while providing large output currents. In addition, the internal power constraints and high operating voltages impose a tight restriction on the internal bias current. To circumvent these problems two class AB output configurations, a quasi-current mirror (QCM) and a floating-current mirror (FCM) were

shown to be the most suitable solutions. Based on the QCM structure a CMOS (CQCM) and a BiCMOS (BQCM) design have been presented. The CQCM line driver offers a compact solution attractive for low-cost twin-tub CMOS or BiCMOS (such as BATMOS-5) processes without PNP transistors . However, if a BiCMOS process with complementary bipolar devices such as (BATMOS-10) is available, the BQCM design can be used to yield improved performance and reliability. Using bipolar transistors, the component mismatch in the QCM stage is greatly reduced, decreasing the sensitivity of the circuit to process variations.

The FCM line driver uses a pure PMOS output stage with internal feedback loops to control the quiescent current. The high voltage NMOS transistors were not used in the output stage of the proposed line driver to avoid the hot-carrier problems in those devices resulting in higher reliability at high operating voltages close to the breakdown voltage of NMOS devices. In addition, the FCM circuit results in a highly stable quiescent current with a very low sensitivity to process variations. It also features a large bandwidth with a small idle current while meeting all the short-loop SLIC specifications.

The improvements in performance of the FCM line driver are achieved at the expense of increased complexity as compared to the QCM line drivers. Therefore, while the QCM line drivers offer a simple compact solution suitable for low cost systems, the FCM design provides improved performance with higher reliability. The complete short loop SLIC front-end, tested with supply voltages up to 30V, dissipates less than 70mW power.

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CHAPTER 5

Conclusions

New emerging technologies such as fiber-to-the-curb, hybrid-fiber-coax and wireless local loops incorporate a broadband medium (optical fiber, coaxial cable or wireless link) in the local access loop to increase the transmission capacity by reducing the length of the existing telephone lines. In these techniques, traditional twisted-pair copper wires are used only in the last 50 meters (or less) of the subscriber loop. Short loops, as compared to the conventional ones, involve higher bandwidth with less noise and interference allowing data transmission at much higher rates.

This thesis has targeted one of the most challenging parts of the short loop networks, the subscriber loop interface circuit (SLIC) which drives the copper loop. In addition to high voltage requirements and functional complexity, short loop SLICs require a high level of integration at very low cost. This work has proven the feasibility of integrating the high voltage building blocks of a short loop SLIC on the same chip with the rest of low voltage circuitry by implementing all the high voltage circuits in a low voltage technology. This approach results in a lower cost and better performance as compared with dedicated high voltage IC technologies.

The high voltage capabilities of the BiCMOS process were enhanced by using extended-drain high voltage NMOS and PMOS devices. These devices were implemented by appropriate layout manipulation without any extra mask or additional processing steps,

thus keeping the performance of the low voltage components intact. Breakdown voltages in the range of 30 to 50 V were achieved for the high voltage NMOS and PMOS transistors. Several high voltage test devices were fabricated and characterized to extract a set of accurate models for circuit simulations. Eventually, a complete CAD environment for high voltage circuit design was developed including a high voltage device library, design and verification rules and HSPICE models.

Because the submicron BiCMOS process was designed and optimized for low voltage applications, the design of high voltage circuits is particularly challenging in this process. The lack of high voltage bipolars and capacitors, specific restrictions on the gate and source voltages of the high voltage devices, second order breakdown effects and protection issues impose severe restrictions on circuit design. Considering these restrictions, an efficiently integrable architecture for a short loop SLIC's high voltage front-end was suggested. It consists of all necessary building blocks including the preamplifier, the common-mode feedback circuit, line drivers and power switch. These building blocks were successfully implemented in the 0.8μm BiCMOS process. All circuits are capable of operating at power supply voltages as high as 30V, satisfying the 24V supply voltage requirements of the short loop systems.

The proposed preamplifier uses a fully-differential high-voltage op amp featuring a bandwidth of 30MHz with more than 80 dB gain. Its output common-mode level is controlled by a novel common-mode feedback circuit (CMFB). The circuit is based on the idea of using the output impedance of the high voltage transistors rather than bulky resistors to sense the high swing voltages at its inputs. This technique results in a wide-range CMFB circuit with minimum power and area. The complete preamplifier and CMFB circuit dissipate less than 10mW power while occupying only $0.1mm^2$ area.

A power switch was also presented based on a high voltage PMOS used in a high-side configuration. It is activated by a level shifter and driver circuit driven by a low voltage control signal.

The line driver, as the most challenging block of the system, was the major focus of this work. The main concern in line driver design is to provide maximum current driving capability while keeping the internal power dissipation as low as possible with an accurate internal quiescent current control. Three high voltage line drivers were presented, all capable of driving more than 30mA current into the loop.

The first line driver relies on a CMOS design with a quasi-current-mirror (QCM) current control technique. With only 25mW power and 0.3 mm^2 area, a bandwidth of more than 2MHz was achieved. This design is ideal for low-cost twin-tub CMOS or BiCMOS processes without PNP transistors such as BATMOS-5.

For BiCMOS processes with complementary bipolar devices such as BATMOS-10, an improved QCM line driver was proposed and implemented. Using bipolar transistors, the matching in the current control circuits was significantly improved resulting in a much lower sensitivity to process variations. The bandwidth was also increased to 3MHz along with 20 dB improvement in supply rejection and 14dB increase in longitudinal balance.

The last line driver design uses a floating-current-mirror (FCM) architecture with an internal feedback loop to control the quiescent current. The advantage of this approach is that the output stage is made up of only PMOS devices avoiding the hot carrier effects in NMOS transistors. As a result, the circuit can operate more reliably at voltages very close to the off-state breakdown voltage of NMOS devices (more than 30V). A bandwidth of 3.8 MHz was achieved with a power dissipation of only 18mW. Due to internal feedback, the idle current of this circuit was highly stable (less than 5% variation).

Future work should consider replacing the high voltage MOS devices with advanced resurfed structures to increase the voltage handling capability of the circuits. This would expand the applications domain of the circuits presented to encompass central office SLIC applications. The development of high voltage bipolar transistors would also be useful in improving the performance of the circuits. Future work should also focus on using an advanced deep submicron CMOS process. Implementing the high voltage circuits in such a process would be a great advantage in a wide range of applications including short loop systems.

APPENDIX A

High Voltage Device Library

In order to facilitate the design of high voltage circuits, a high voltage device library was developed in Cadence. This library includes the symbols, layouts and models for high voltage NMOS and PMOS devices. New DRC and circuit extraction rules have also been developed and added to the high voltage device library. The complete design environment can be used to perform schematic entry, layout design, design rule check (DRC), circuit extraction, layout-versus-schematic (LVS) verification and post-layout simulations. The layouts and model parameters of the high voltage devices are provided in this appendix.

All the high voltage devices modeled and used in this thesis have the same channel length (3μm). Also the drift region and gate overlap dimensions are fixed as shown in Fig. A.1. The models must be updated for devices with other dimensions. However, there is no constraint on the width of transistors and the models can be used for different channel widths.

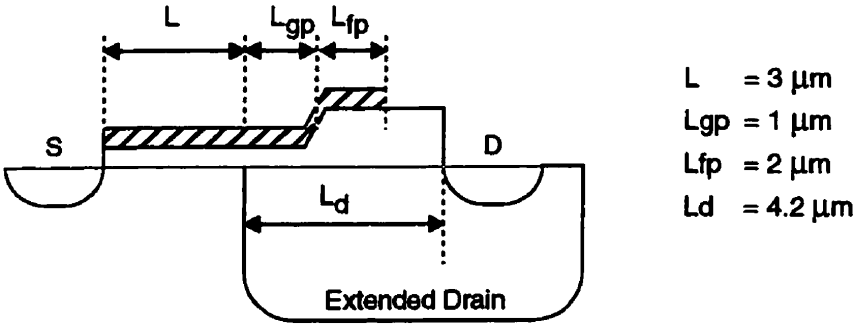

Fig. A.1: Dimensions of the high voltage structures

A.1 Device Layouts

The layouts of the high voltage NMOS devices in both BATMOS-5 and BATMOS-10 processes are illustrated in Fig. A.2. The layouts are similar in both processes except for the use of high voltage n-well instead of n-well and the additional n-subwell layer used in BATMOS-10 devices to isolate the body from the substrate. The n-subwell mask covers all the p-well area surrounded by the n-well.

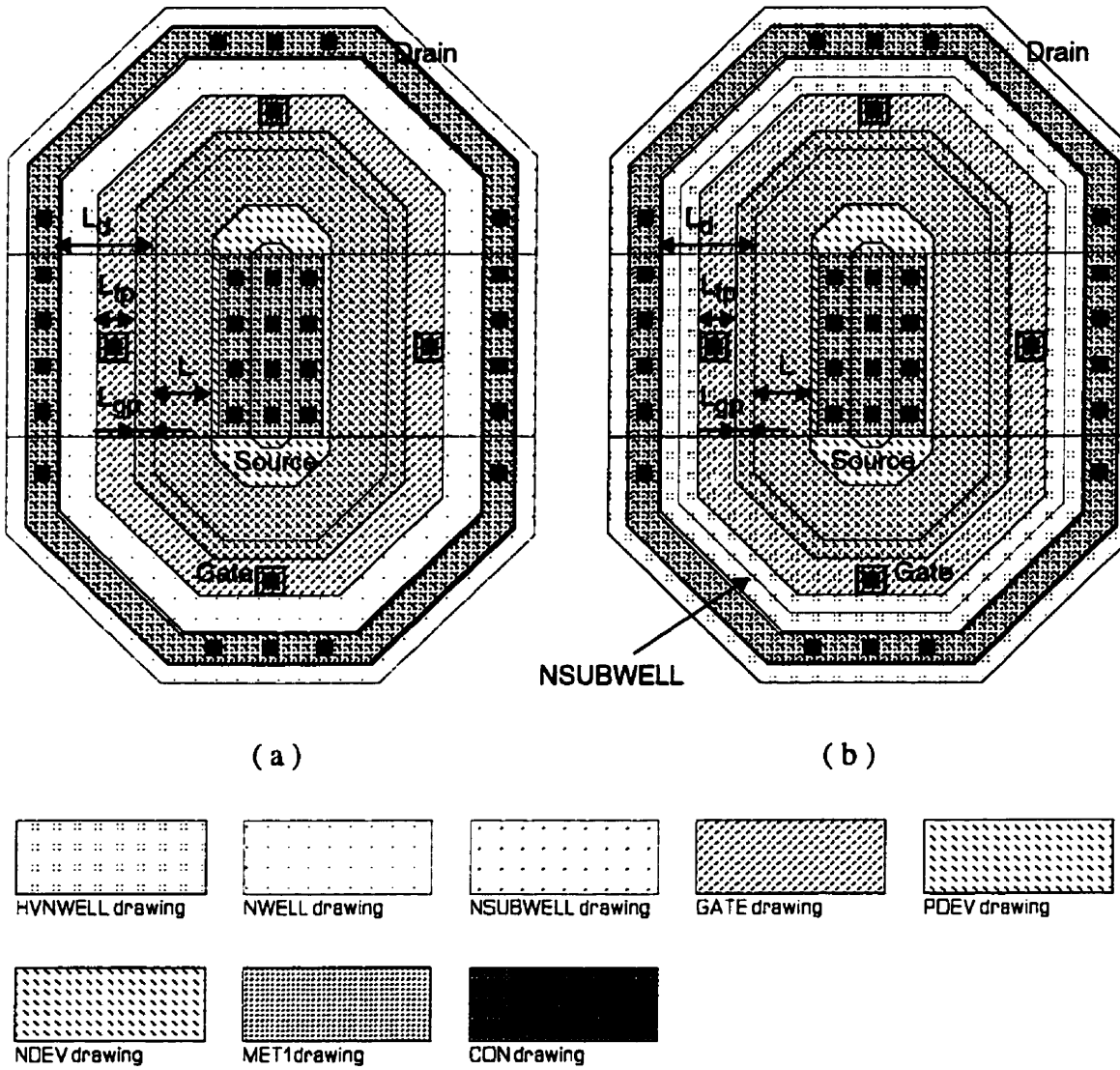

Fig. A.2: Layouts of the high voltage NMOS devices in a) BATMOS-5 and b) BATMOS-10

The layouts of the high voltage PMOS transistors are shown in Fig. A.3. In these layouts, the drain region is surrounded by the n-well. In BATMOS-5 the mask layer for n-buried layer (M_NBL) is used to isolate the drain region from the substrate while in BATMOS-10 the n-subwell mask can be used for this purpose.

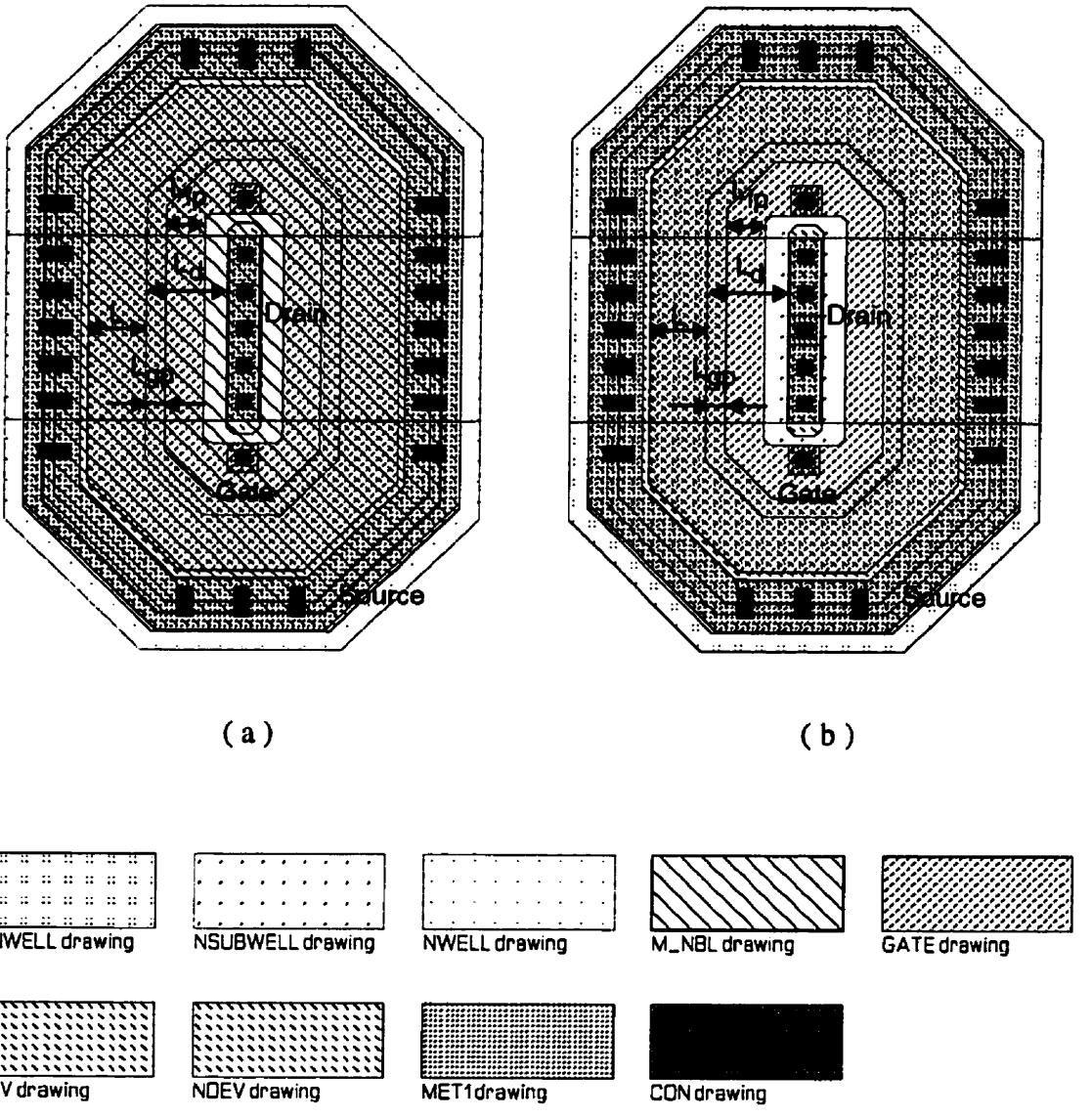

Fig. A.3: Layouts of the high voltage PMOS devices in a) BATMOS-5 and b) BATMOS-10

A.2 Using mask layers in BATMOS-5 and BATMOS-10

The n-well and n-buried layer regions are self-aligned in the standard BATMOS process. In order to implement the high voltage devices, it is necessary to create separate n-well, high voltage n-well (HV n-well) or n-buried layer regions. This requires drawing some features directly on the mask layers rather than the standard design layers, usually used in Cadence.

The standard design layers available in the BATMOS CAD environment, are usually used to specify the actual shape and size of different regions of the layout. A set of mask layers are then generated from the design layers at NORTEL according to some specific process rules. These mask layers contain the final data used to make the actual masks.

As illustrated in Fig. A.4, three different mask layers are automatically generated from the n-well design layer in BATMOS-5. Fig. A.5 shows similar mask layers generated from the HV n-well design layer in BATMOS-10. These set of mask layers result in self-aligned

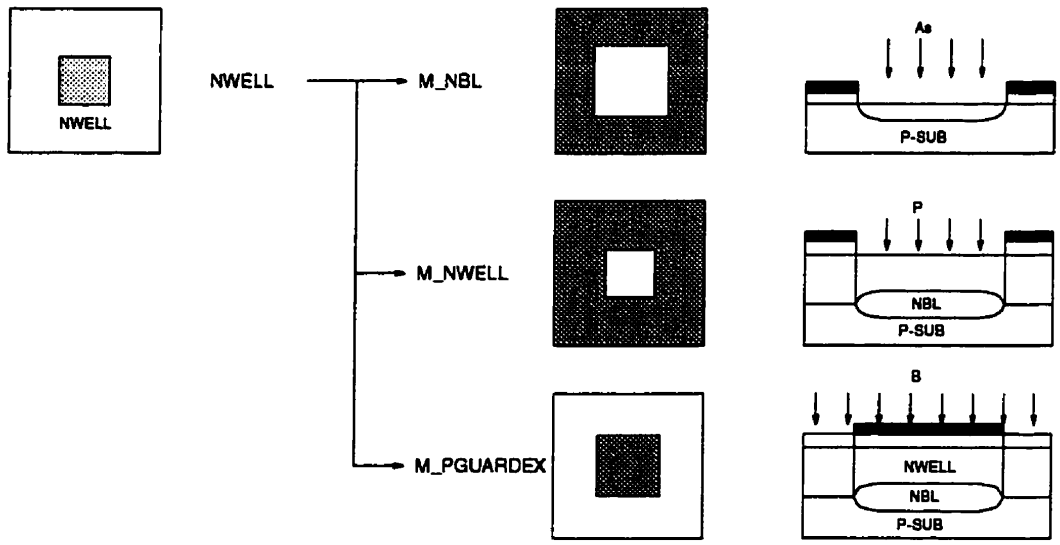

Fig. A.4: Mask layers generated from the n-well design layer in BATMOS-5

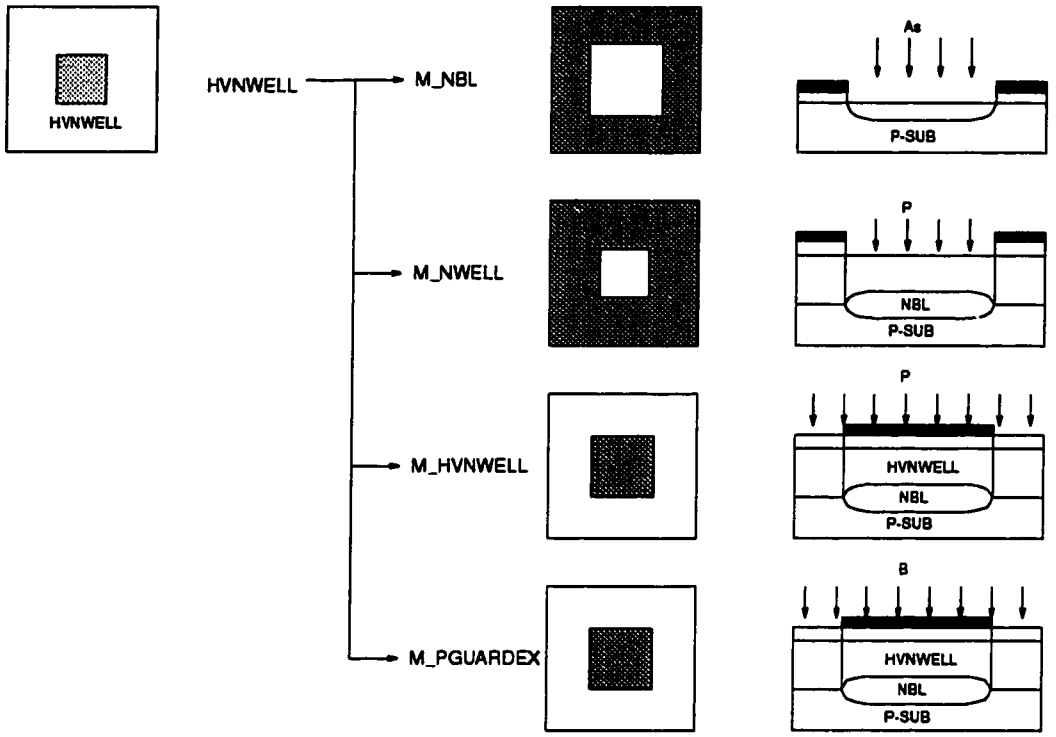

Fig. A.5: Mask layers generated from the HV n-well design layer in BATMOS-10

n-well, HV n-well and n-buried layer structures. To implement each one of these regions separately, proper mask layers instead of the design layers must be used to draw the layout of the high voltage devices. The features drawn on these layers are merged with those generated automatically for other low voltage components.

Fig. A.6 shows the mask layers that must be used to implement different layers. The guideline can be summarized as follows:

- To implement n-buried layer in both BATMOS-5 and BATMOS-10 (Fig. A.6-a) only n-buried layer mask layer M_NBL must be used. The actual dimensions would be about 2mm larger due to the lateral diffusion of the buried layer.
- To implement n-well without n-buried layer in both BATMOS-5 and BATMOS-10 (Fig. A.6-b), the mask layers of n-well, M_NWELL, and p-guard implant,

M_PGUARDEX must be used. The M_PGUARDEX mask must overlap the M_NWELL by 1μm.

- To implement HV n-well in BATMOS-10 (Fig. A.6-c), the mask layers for n-well, M_NWELL, HV n-well, M_HVNWELL and p-guard implant, M_PGUARDEX must be used. Both M_HVNWELL and M_PGUARDEX must overlap the M_NWELL area by 1μm.

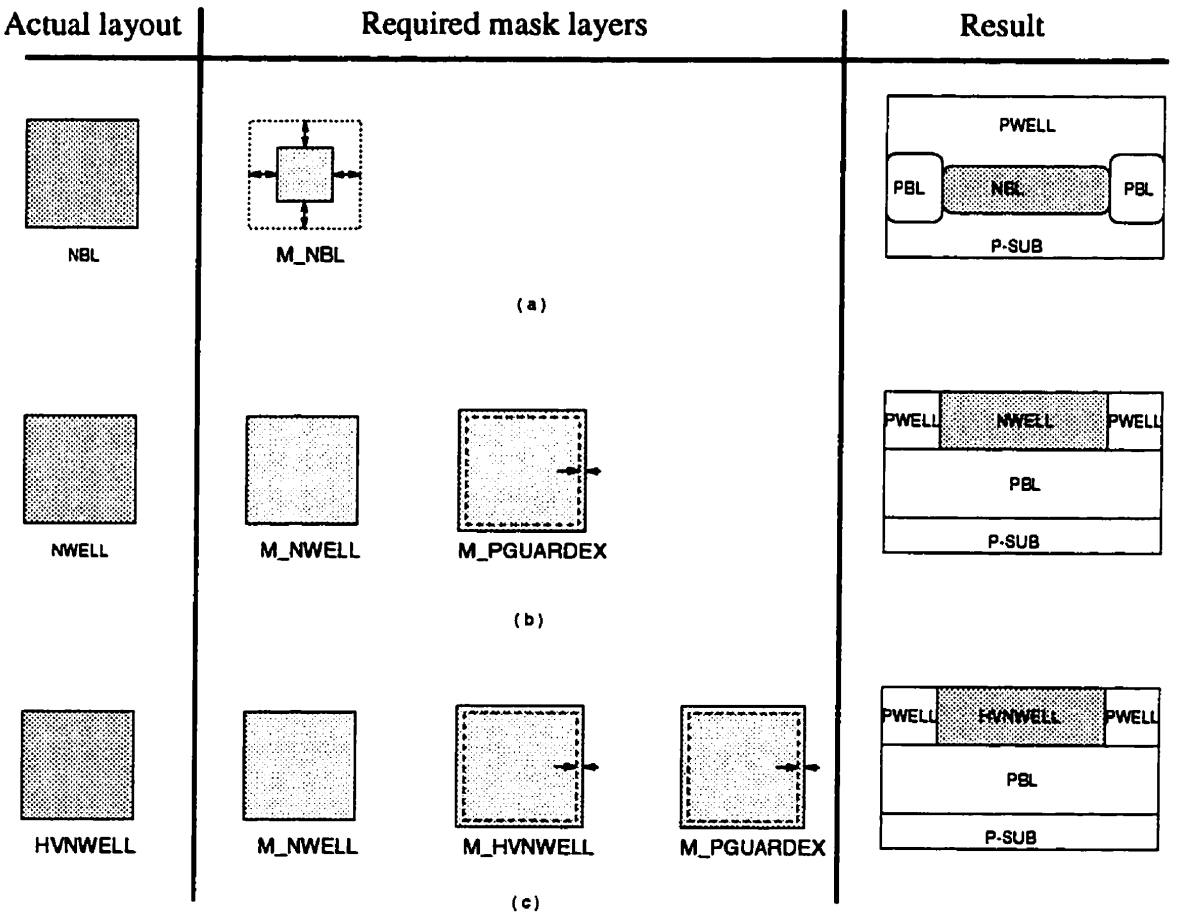

Fig. A.6: Required mask layers to implement: a) n-buried layer region in both BATMOS-5 and BATMOS-10, b) n-well in both BATMOS-5 and BATMOS-10, and c) HV n-well in BATMOS-10

A.3 Models

The extracted HSPICE model parameters for the high voltage NMOS and PMOS devices in both BATMOS-5 and BATMOS-10 processes are presented in this section. These models can be used for high voltage transistors with 3μm channel length and any channel width. Other structural dimensions are the same as those illustrated in Fig. A.1.

BATMOS-5 High Voltage NMOS Model:

```
** HIGH VOLTAGE N_CHANNEL MOSFET - BATMOS_5
** GATE LENGTH = 3.0 μm, GATE WIDTH = Any
* Common model parameters
.MODEL HVNMOS5 NMOS
+ XL=0.00          XW=0.00
+ LMIN=1.6E-6      LMAX=5.0E-6
+ WMIN=1.4E-6      WMAX=500E-6
+ LEVEL=3          ACM=2
* Current parameters
+ VTO=726.6E-3     UO=475          TOX=17.52E-9
+ NSUB=3.231E16    NFS=819.9E9     DELTA=2.12
+ THETA=859E-3     WD=0.00         PB=0.926
+ LD=55E-9         LDIF=940.5E-9   XJ=247.9E-9
+ VMAX=184E3       ETA=1.01E-3     KAPPA=693E-3
+ RS=595.6         RSH=0.0         HDIF=1.2E-6
* Impact ionization parameters
+ ALPHA=8.5        VCR=155
* Extended drain resistance
+ RD=9.463E3
* Capacitance parameters
+ JS=5.0E-4        JSW=5.5E-9
+ CJ= 322E-6       MJ=0.46
+ CJSW=322E-12     MJSW=0.20
+ CGSO=288.4E-12 CGBO=568.3E-12
```

+ CGDO=1.584E9

* Other parameters

+ TLEV=1 TCV=21.35E-6 BEX=-2.183

+ TLEVC=1 TRS=-1.121E-3 TRD=-1.121E-3

+ NLEV=2 KF=600E-27 AF=0.80

BATMOS-5 High Voltage PMOS Model:

** HIGH VOLTAGE P_CHANNEL MOSFET - BATMOS_5

** GATE LENGTH = 3.0 μm, GATE WIDTH = Any

* Common model parameters

.MODEL HVPMOS5 PMOS

+ XL=0.00 XW=0.00

+ LMIN=1.6E-6 LMAX=5.0E-6

+ WMIN=1.4E-6 WMAX=500E-6

+ LEVEL=3 ACM=2

* Current parameters

+ VTO=-755E-3 UO=172 TOX=17.5E-9

+ NSUB=3.041E16 NFS=432.3E9 DELTA=0.892

+ THETA=68E-3 WD=125.1E-9 PB=0.926

+ LD=1E-9 LDIF=999.0E-9 XJ=20.0E-9

+ VMAX=233.4E3 ETA=0.51E-12 KAPPA=60.1E-1

+ RS=1.2E3 RSH=0.0 HDIF=1.2E-6

* Extended drain resistance

+ RD=124.3E3

* Capacitance parameters

+ JS=5.0E-4 JSW=5.5E-10

+ CJ= 440E-6 MJ=0.57

+ CJSW=200E-12 MJSW=0.30

+ CGSO=214E-12 CGBO=568.3E-12

+ CGDO=1.584E9

* Other parameters

+ TLEVC=1 PTA=1.39E-3 PTP=4.55E-3

+ CTA=1.35E-3 CTP=941E-6

+ NLEV=2 KF=250.0E-27 AF=0.95

BATMOS-10 High Voltage NMOS Model:

** HIGH VOLTAGE N_CHANNEL MOSFET - BATMOS_10

** GATE LENGTH = 3.0 μm, GATE WIDTH = Any

* Common model parameters

.MODEL HVNMOS10 NMOS

+ XL=0.00 XW=0.00

+ LMIN=1.6E-6 LMAX=5.0E-6

+ WMIN=1.4E-6 WMAX=500E-6

+ LEVEL=3 ACM=2

* Current parameters

+ VTO=720E-3 UO=475 TOX=17.52E-9

+ NSUB=3.231E16 NFS=819.9E9 DELTA=1.06

+ THETA=70E-3 WD=0.00 PB=0.9236

+ LD=55E-9 LDIF=940.5E-9 XJ=247.9E-9

+ VMAX=189E3 ETA=35E-3 KAPPA=119E-2

+ RS=595.6 RSH=0.0 HDIF=1.2E-6

+ Impact ionization parameters

+ ALPHA=9 VCR=170

* Extended drain resistance

+ RD=10.5E3

* Capacitance parameters

+ JS=5.0E-4 JSW=5.5E-10

+ CJ= 386E-6 MJ=0.50

+ CJSW=185E-12 MJSW=0.25

+ CGSO=273E-12 CGBO=568.3E-12

+ CGDO=2.8E9

* Other parameters

+ TLEV=1 TCV=980E-6 BEX=-1.65

+ TLEVC=1 TRS=-1.0E-3 TRD=-1.0E-3

```
+ NLEV=2          KF=1.5E-24          AF=0.80
```

BATMOS-10 High Voltage PMOS Model:

```
** HIGH VOLTAGE P_CHANNEL MOSFET - BATMOS_10
** GATE LENGTH = 3.0 µm, GATE WIDTH = Any
* Common model parameters
.MODEL HVPMOS10 PMOS
+ XL=0.00          XW=0.00
+ LMIN=1.6E-6      LMAX=5.0E-6
+ WMIN=1.4E-6      WMAX=500E-6
+ LEVEL=3          ACM=2
* Current parameters
+ VTO=-716E-3      UO=172          TOX=17.5E-9
+ NSUB=3.045E16    NFS=432.3E9     DELTA=0.892
+ THETA=68E-3      WD=125.1E-9     PB=0.926
+ LD=1E-9          LDIF=999.0E-9   XJ=20.0E-9
+ VMAX=233.4E3     ETA=0.51E-12    KAPPA=8.27E-1
+ RS=1.2E3         RSH=0.0         HDIF=1.2E-6
* Extended drain resistance
+ RD=28E3
* Capacitance parameters
+ JS=5.0E-4        JSW=5.5E-10
+ CJ= 472E-6       MJ=0.57
+ CJSW=215E-12     MJSW=0.30
+ CGSO=214E-12     CGBO=568.3E-12
+ CGDO=1.584E9
* Other parameters
+ TLEVC=1          PTA=1.90E-3     PTP=4.49E-3
+ CTA=1.54E-3      CTP=40.5E-6
+ NLEV=2          KF=250.0E-27    AF=0.95
```