INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

Bell & Howell Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

A 1 V Floating-Point Analog-to-Digital Converter for Portable Communication Devices

by

Takayuki Hayashi

A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Department of Electrical and Computer Engineering
University of Toronto

© Copyright by Takayuki Hayashi 1998

National Library of Canada
Acquisitions and Bibliographic Services
395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque nationale du Canada
Acquisitions et services bibliographiques
395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

Our file Notre référence

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

0-612-45436-3

Canada

A 1 V Floating-Point Analog-to-Digital Converter
for Portable Communication Devices

Takayuki Hayashi
Master of Applied Science, 1998
Department of Electrical and Computer Engineering
University of Toronto

ABSTRACT

With the growing demand for portable communications devices, power consumption has become increasingly critical in VLSI designs. In mixed-signal circuits, the push for lower supply voltage to reduce power dissipation in digital systems has forced analog systems to lower their supply voltage as well.

This thesis deals with the design of a low power low voltage analog-to-digital converter (ADC) that operates from a single 1 V power supply. Two circuit techniques are utilized to enhance the performance of the converter. First, floating-point technique is employed to improve the dynamic range of the converter by providing a non-uniform quantization of the analog input. This allows the ADC to achieve a wide dynamic range without using high-resolution components. Second, current-mode technique is chosen because it offers characteristics such as good signal swings, high speed and small circuit area.

The ADC was implemented using a 0.5 μm, 1V CMOS process with low threshold voltage transistors. Simulation results of the core ADC cell indicate an 8-bit resolution while dissipating only 170 μW. The complete floating-point ADC exhibits a dynamic range of 12 bits, a conversion time of 63 μs and a power dissipation of 450 μW. The total area excluding bonding pads is 1 mm^2.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to Professor C. A. T. Salama for his guidance and encouragement throughout the course of this research.

I would like to thank John Gates for his invaluable contributions early on in this work, Jaro Pristupa for technical assistance with the CAD tools, and Mehran Aliahmad for helpful suggestions and comments. Also, my sincere thanks to Luigi Di Pede, Stanley Ma and Dusan Suvakovic for countless hours of valuable discussions. My appreciation also extends to all the members who reside in LP477 (or the CAD room in some cases) for creating an enjoyable working environment. Finally, I would like to thank my parents and my girlfriend, Wendy Fung, for making this all possible.

This work was supported by Micronet, ITRC, Gennum and Nortel.

TABLE OF CONTENTS

CHAPTER 1

Page

Introduction 1

1.1 Popular Analog-to-Digital Converter Architectures 2

1.2 Low-Power Low-Voltage Analog-to-Digital Converters 5

1.3 Low-Power CMOS Processes 6

1.4 Floating-Point Analog-to-Digital Converters 8

1.5 Current-Mode vs. Voltage-Mode 8

1.6 Thesis Objective and Outline 9

1.7 References 11

CHAPTER 2

Page

Floating-Point ADC Architecture 16

2.1 Introduction 16

2.2 Floating-Point Analog-to-Digital Conversion Algorithm 17

2.3 Block Diagram of a Floating-Point ADC 19

2.4 Analog-to-Digital Converter Cell 20

2.4.1 Algorithmic Conversion 20

2.4.2 Current-Mode Ratio-Independent Algorithmic ADCs 21

2.4.2.1 Nairn's Design 21

2.4.2.2 Cujec's Design 23

2.4.3 Low-Power Low-Voltage ADC Cell Design 25

2.4.4 Amplifier Design 28

2.5 Current-Mode Programmable Gain Amplifier 32

2.5.1 Basic Structure 32

2.5.2 Current Multiplier Cells 33

2.5.3 Amplifier Design 34

2.6 Encoder Circuit 35

2.7 Control Circuit 36

2.7.1 Generation of Control Signals for the Switches in the ADC Cell 36

2.7.2 Generation of Control Signals for the External Switches 38

Page

2.7.3 Generated Control Signal Waveforms 39
2.8 Layout of the FADC 40
2.9 Simulation Results of the ADC Cell 41
2.10 Simulation Results of the FADC 45
2.11 Experimental Implementation 46
2.12 Summary 46
2.13 References 47

CHAPTER 3

Page

Conclusions 49

APPENDIX A

Page

Analog-to-Digital Converter Testing Procedures 51
A.1 Accuracy Measurements 51
A.2 Conversion Speed Measurements 52
A.3 References 53

LIST OF FIGURES

		Page
Fig. 1.1	Digital Signal Processing	2
Fig. 1.2	The Effect of Vto Scaling on Leakage Current	7
Fig. 2.1	I/O Response of (a) Conventional ADC and (b) Floating-Point ADC	16
Fig. 2.2	(a) Flowchart of Floating-Point Conversion and (b) Multiplication Factors	18
Fig. 2.3	Block Diagram of 12-bit Dynamic Range FADC Employing an 8-bit ADC Cell	20
Fig. 2.4	Flow Chart of the Algorithmic Conversion Method	21
Fig. 2.5	Nairn's Design	22
Fig. 2.6	Cujec's Design	24
Fig. 2.7	Revised ADC Cell Design	25
Fig. 2.8	Op-Amp Design for ADC Cell	29
Fig. 2.9	(a) Active Current Mirror and (b) Small-Signal Model	30
Fig. 2.10	Current-Mode PGA	32
Fig. 2.11	Current Multiplier Cells	33
Fig. 2.12	Op-Amp Design for Multiplier Cell	35
Fig. 2.13	Encoder Circuit	36
Fig. 2.14	Control Circuit 1	37
Fig. 2.15	Generation of Control Signals for Switches S1 ~ S7	37
Fig. 2.16	Control Circuit 2	38
Fig. 2.17	Generated Control Signal Waveforms	39
Fig. 2.18	Layout of the FADC	40
Fig. 2.19	Transient Simulations showing the Currents in ADC Cell	42
Fig. 2.20	Transient Simulations showing the Amplifier Output Voltage	42
Fig. 2.21	Integral Nonlinearity vs. Code	44
Fig. 2.22	Differential Nonlinearity vs. Code	44
Fig. A.1	Setup for Testing the ADCs	52

LIST OF TABLES

		Page
Table 1.1	Recently Reported Low-Power Low-Voltage ADCs	6
Table 1.2	Currently Available Low-Voltage CMOS Processes	8
Table 2.1	Device Sizes for ADC Cell	28
Table 2.2	Device Sizes for Switches in ADC Cell	28
Table 2.3	Device Sizes for Op-Amp	31
Table 2.4	Exponent Output and PGA Gain Settings	32
Table 2.5	Device Sizes for Multiply-by-one Multiplier Cell	33
Table 2.6	Device Sizes for Multiply-by-two Multiplier Cell (odd)	34
Table 2.7	Device Sizes for Multiply-by-two Multiplier Cell (even)	34
Table 2.8	Device Sizes for Switches in PGA	34
Table 2.9	Device Sizes for Op-Amp	35
Table 2.10	Counting Sequence of PRBS Counter	39
Table 2.11	Circuit Area of Each Block	40
Table 2.12	ADC Cell Characteristics	45
Table 2.13	FADC Characteristics	45

CHAPTER 1

Introduction

Traditionally, circuit speed and chip area have been considered the two most critical performance parameters for VLSI designs. Recently, however, power consumption has become increasingly important due to the high demand for portable communication devices. These devices are used to move information to and from people through wireless network supporting a wide range of services [1]. For such devices to gain market acceptance, they must be portable, highly functional and energy efficient. Among these requirements, high energy efficiency deserves special attention [2]. It not only guarantees a long battery life but also results in lower cost, size, weight and increase in reliability of the device by eliminating the need for thermal management hardware.

In digital systems, the most popular way to reduce power dissipation is to lower the supply voltage. Currently, 3 V supply is starting to replace 5 V as the industry standard. It is expected that by the end of this decade, most portable communication devices will operate at around 1 V [2].

On the other hand, in analog systems, reducing the supply voltage does not necessarily result in a lower power dissipation [3]. This is due to the fact that as the supply voltage is scaled, the noise must be scaled correspondingly to maintain the same dynamic range. For this reason, purely analog systems may not follow digital ones in the scaling of the supply. In mixed-signal VLSI circuits used for portable communication devices, however, analog power supplies are likely to be set by digital ones since these devices are usually powered by a single-cell battery.

Signal processing can be accomplished in either the analog or the digital domain. Digital signal processing (DSP) has become increasing popular because of the advances made in the design and fabrication of digital circuits. Since most signals originate in the analog domain, analog-to-digital converters (ADC) are required to convert analog signals into digital signals as shown in Fig. 1.1. Following the DSP block, the processed signals are reconstructed using a digital-to-analog converter (DAC). DSP is common in communication systems, radar and sonar, speech and video coding and enhancement, and biomedical engineering [4].

Fig. 1.1 Digital Signal Processing

1.1 Popular Analog-to-Digital Converter Architectures

There are four major characteristics that define the performance of an ADC. The first characteristic is the resolution used to represent the analog signal. A high resolution is desirable since it ensures reduction of errors inherent to the quantization process. The second characteristic is the sampling rate. A high sampling rate is required if the input signal contains high frequency components. The third characteristic is the power dissipation. Typically, high-resolution or high-speed ADCs tend to consume more power than simpler low-resolution designs. Finally, the last characteristic is the circuit area.

A variety of different architectures exist for implementing ADCs. The five dominant ones include *flash* [5,6], *integrating* [7], *oversampling* [8,9], *successive-approximation* [10,11] and *algorithmic* converters [12,13,14,15]. Each architecture offers specific advantages over the others.

Flash converters are the standard approach for realizing high-speed ADCs. An N-bit flash converter consists of a precision resistor array, (2^N-1) comparators and an encoder. To perform the conversion, separate comparators are used to compare simultaneously the input signal to each of the possible quantization levels. The encoder then takes the output of the comparators and generates the appropriate output code. While Flash ADCs are fast, they consume a significant amount of power and require a large area. In fact, the number of comparators used by the converter doubles with each additional bit of resolution. Recently, a flash converter achieving a resolution of 8 bits and a sampling rate of 500 MHz while occupying an area of 20.8 mm^2 was fabricated using a 10 GHz bipolar process [6].

When higher resolution is required, an integrating converter can be used. First, the input signal, which is usually sampled as a voltage on a capacitor, is discharged using a current sink at a known rate. By measuring the discharge time with a digital counter, the magnitude of the input signal can be determined. The conversion speed of integrating converters is quite slow. In addition, they require a very accurate digital counter and a highly linear current sink. A 14-bit integrating converter with a sampling rate of 50 kHz and an area of 12 mm^2 was fabricated using a 2 μm bipolar process [7].

When high resolution and reduced analog circuit complexity are needed, an oversampling converter is used. This type of converter consists of a modulator and a decimation filter. First, the input signal is sampled at a rate that is much higher than the Nyquist rate. The modulator produces a pulse-density modulated signal whose density over a given time period is equal to the mean value of the input over the same period. The output, however, contains a significant amount of out-of-band quantization noise which is removed by the decimation filter. Although oversampling converters have reduced sensitivity to the analog circuitry, they require additional digital processing. As a result, they typically require a large area. Also, the need for a high oversampling rate makes these converters

slow. Nevertheless, an example of oversampling converter is a fifth order converter with a 18-bit resolution and a 20 kHz sampling rate [9]. It required 32 mm^2 for the modulator and 37.4 mm^2 for the decimation filter.

Successive-approximation converters offer a relatively fast conversion time without the need for excessive post-conversion processing. First, using a DAC and some control circuitry, precisely controlled reference signals are generated. These reference signals are then compared to the input signal. By adjusting the reference signal in a binary search pattern, the converter is able to complete a N-bit conversion in only N comparisons. A successive-approximation converter fabricated in a 6 μm CMOS process achieved a resolution of 15 bits at a sampling rate of 12 kHz while requiring an area of 11.8 mm^2 [11].

By eliminating the need for the DAC used in the successive-approximation converter, an algorithmic converter can be realized. Instead of continuously adjusting the reference current, algorithmic converters use multiplication and subtraction circuits to adjust the input signal until it approximates the reference signal. Since this type of converter requires only simple multiplication and subtraction circuits, it occupies a small area and dissipates very little power. Using a ratio-independent technique, high-resolution converters can be implemented without using precisely matched components. For example, a 10-bit current-mode converter with a sampling rate of 25 kHz occupying only 0.32 mm^2 in a 3 μm CMOS process has been reported [14]. By incorporating a pipeline technique, conversion speed can be significantly improved. This method produced a 10-bit current-mode converter with a 83 kHz sampling rate [15].

Each of the five converters mentioned above presents a performance trade-off. The designer must choose the appropriate architecture based upon the target specifications. In general, flash converters are used when very high speed is required. Integrating, oversampling and successive-approximation converters are used when high accuracy is needed. Algorithmic converters are suited for portable, low-power applications.

1.2 Low-Power Low-Voltage Analog-to-Digital Converters

To be useful in portable communication devices, ADCs must meet very stringent requirements. First and foremost, the power dissipation of the converter must be kept to a minimum to ensure a long battery life. Furthermore, cost, size and performance constraints will require the converter to be powered by a single-cell battery that is compact. The sampling rate depends on the application of the ADC. If the input signal is assumed to lie within the voice band, sampling rates in the range of 8 kHz to 20 kHz are required to satisfy the Nyquist criterion. It is usually very difficult to reduce power dissipation and still maintain a reasonable circuit speed. For instance, an amplifier's bandwidth is proportional to its transconductance which in turn is proportional to the square root of its bias current. Since lower power dissipation usually implies lower bias current, it becomes increasing challenging to maximize circuit speed as the supply voltage is reduced. The resolution of the converter is also application dependent. For example, an ADC used for a digital hearing aid with a SNR of 80 dB requires at least 14 bits of resolution to maintain the quantization noise below this level. Reduced dynamic range in a low-voltage environment requires that the ADC incorporate innovative circuit techniques to achieve a high resolution. Finally, portable communication devices should be lightweight and compact. Therefore, the ADC must occupy as small an area as possible.

A number of low-power low-voltage ADCs have been reported as listed in Table 1.1. In the reported ADCs, high-speed ones with sampling rates in the MHz range consumed more power than other designs because they used the flash architecture. In addition, to retain wide signal swings at low supply voltages, most designs did not employ popular circuit configurations such as cascodes. The gate voltage of many switches had to be bootstrapped so that the switches can be fully turned on or off. To reduce the effects of these problems, some circuits took advantage of a low-voltage CMOS process with a reduced threshold voltage which is discussed in the next section.

At present, there are very few ADCs operating from a power supply lower than 1 V. One was constructed using a 0.5 μm CMOS process that has both normal and low threshold voltage transistors [22]. The other design used voltage doublers to increase the supply voltage internally [32].

Table 1.1 Recently Reported Low-Power Low-Voltage ADCs

Reference	Resolution (bit)	Input Bandwidth (Hz)	Power Dissipation (mW)	Supply Voltage (V)	Circuit Area (mm^2)	Technology (μm CMOS)	Low/ Multi V_{th}
[16]	10	10 M	30	2.5	6.5	0.8	No
[17]	10	20 M	85	2.7	4.0	0.8	Yes
[18]	12	0.5 M	1	3	4.1	0.8	No
[19]	12	0.5 M	60	2	22.4	1.2	No
[20]	4	2.25 M	0.5	2.5	0.02	1.2	No
[21]	8	10 M	10	1.5	N/A	0.5	Yes
[22]	10	192 k	1.56	1	2.5	0.5	Yes
[23]	12	5 k	2	1.5	N/A	0.8	No
[24]	16	14~27 k	40	2.7	N/A	0.8	Yes
[25]	10	1.5 M	10.8	2.7	1.5	0.8	No
[26]	10	10 M	20	2	12.16	0.5	Yes
[27]	15	25 k	5.4	1.8	2.9	1.2	No
[28]	15	3.5 k	2	1.8	0.44	0.6	No
[29]	13	3.4 k	0.2	2.2	0.5	0.5	No
[30]	12	2.5 M	33	2.5	17.2	1.2	No
[31]	8	7.5 M	8	1.5	3.7	0.5	No
[32]	13	8 k	N/A	0.9	N/A	0.8	Yes

1.3 Low-Power CMOS Processes

CMOS is considered to be a convenient technology in low-power designs because it offers very low standby currents. As mentioned previously, decreasing the supply voltage is one of the most efficient ways of reducing the power dissipation in digital systems. However, the threshold voltage should also be scaled down to ensure that the performance remains as high as possible at the reduced power supply. Based on energy-delay product considerations, the threshold voltage should be approximately three times the supply volt-

age to achieve the optimum operating point between energy efficiency and circuit speed [33].

When reducing the threshold voltage from V_{to} to V_{to}', the off-state leakage current increases from I_{off} to I_{off}' due to subthreshold leakage as shown in Fig. 1.2 [34]. Therefore, the subthreshold swing S must be reduced (from s1 to s2) in order to ensure that the device can be turned off efficiently without undesirable leakage currents.

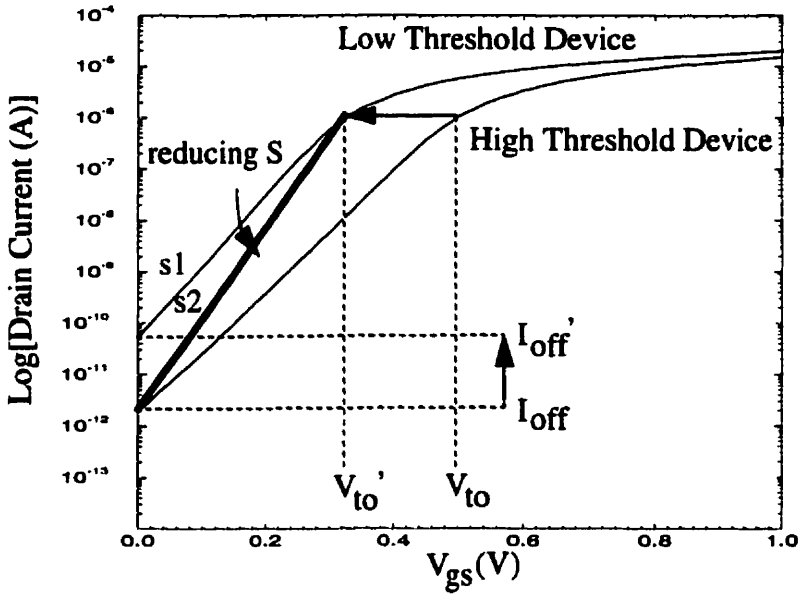


Fig. 1.2 The Effect of V_{to} Scaling on Leakage Current

Table 1.2 shows a list of presently available low-voltage CMOS processes [34]. The IMEC process was used for this thesis because of its inherent 300 mV threshold voltage and its low subthreshold slope.

Table 1.2 Currently Available Low-Voltage CMOS Processes

Company/ University	Supply Voltage (V)	V_T (V)	L(μm)	X_o (Å)	S (mV/dec)
TI	3.3	0.8	0.5	120	80
IBM	2.5	0.4	0.25	70	80
AT&T	1	0.2	0.25	90	80
IMEC	1	0.3	0.5	70	70
STANFORD	1	0.1	0.25	49	80
MIT	1	0.25	0.25	50	70

1.4 Floating-Point Analog-to-Digital Converters [35]

Floating-point analog-to-digital conversion is a technique to improve the signal-to-quantization noise ratio and to reduce redundancy of digital data by providing a non-uniform quantization of the analog input [35]. By performing a variable amplification of the input signal, a wide dynamic range can be obtained without using high-resolution components.

A number of floating-point ADCs (FADC) have been reported. A 20-bit dynamic range FADC with a 320 kHz sampling rate was implemented using a 4-bit flash ADC and a 12-bit two-step ADC [36]. Also, using a 10-bit capacitive DAC, a 16-bit dynamic range FADC was designed [37]. Finally, a 20-bit dynamic range FADC was realized using a 4-bit flash ADC and a 12-bit sampling ADC [38].

1.5 Current-Mode vs. Voltage-Mode

An ADC can be realized using either voltage or current as the active signal. The voltage-mode technique has dominated so far [39] because MOS transistors have the unique ability to transfer and store voltages. The current-mode technique offers many advantages over the more traditional voltage-mode technique. First, due to the non-linear

I-V characteristics of MOS transistors, small changes in the gate voltage result in large changes in the drain current. As a result, current-mode circuits can achieve large signal swings even with a reduced power supply voltage. Second, current-mode circuits are typically faster than their voltage-mode counterparts because their required low-impedance nodes result in smaller time constants. Third, current-mode circuits usually occupy a smaller area and consume less power because they use current mirrors as the major processing block instead of operational amplifiers. Finally, addition and subtraction of signals in current-mode circuits are easily accomplished by simply connecting two or more nodes together. Current-mode techniques have been used in a wide range of applications including filters, data converters and amplifiers [39].

1.6 Thesis Objective and Outline

The main objective of this thesis is to design a 1 V low-power FADC for portable communication devices. The converter must have a resolution of 12 ~ 16 bits and an input bandwidth of 6 ~ 8 kHz while dissipating power in the 300 ~ 500 μW range. The floating-point technique is used to achieve the desired resolution using only an 8-bit ADC cell. In addition, the current-mode technique is employed because it features good signal swings, a high speed and a small circuit area.

The low-voltage 0.5 μm, 1 V CMOS process from Inter-University MicroElectronics Centre (IMEC)[1] is used to design and fabricate the design. This process provides a threshold voltage of 320 mV and a subthreshold slope of 70 mV/dec which are required to achieve optimum energy-delay product at a supply voltage of 1 V.

Chapter 2 discusses the algorithm, structure and advantages of the floating-point technique. It investigates the major building blocks necessary to implement the FADC.

1. Leuven, Belgium.

Simulation results are also presented [40]. Finally, Chapter 3 provides conclusions and suggestions for future work.

1.7 References

[1] R. W. Brodersen, A. Chandrakasan and S. Sheng, "Technologies for Personal Communications," *IEEE Symposium of VLSI Circuits*, pp. 5-9, 1991.

[2] S. Malhi and P. Chatterjee, "1-V Microsystems - Scaling on Schedule for Personal Communications," *IEEE Circuit & Devices*, vol. 10, pp. 13-17, 1994.

[3] R. Castello, "Analog Supply Scaling. Will it Follow Digital?" *International Solid-State Circuits Conference*, pp. 106-107, 1996.

[4] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, Prentice Hall Inc., New Jersey 1989.

[5] T. Kumamoto, M. Nakaya, H. Honda, S. Asai, Y. Akasaka and Y. Horiba, "An 8-bit High-Speed CMOS A/D Converter", *IEEE Journal of Solid-State Circuits*, vol. 21, pp. 976-981, 1986.

[6] Y. Gendai, Y. Komatsu, S. Hirase and M. Kawata, "An 8b 500 MHz ADC," *IEEE International Solid-State Circuits Conference*, pp. 172-173, 1991.

[7] T. Sugawara, M. Ishibe, H. Yamada, S. Majima, T. Tanji and S. Komatsu, "A Monolithic 14 Bit/20 μs Dual Channel A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 18, pp. 723-728, 1983.

[8] S. R. Norsworthy, I. G. Post and H. S. Fetterman, "A 14-bit 80-kHz Sigma-Delta A/D Converter: Modeling, Design and Performance Evaluation," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 256-266, 1989.

[9] R. W. Adams, P. F. Ferguson, Jr., A. Ganesan, S. Vincelette, A. Volpe and R. Libert, "Theory and Practical Implementation of a Fifth-Order Sigma-Delta A/D Converter," *Journal of the Audio Engineering Society*, vol. 39, pp. 515-528, 1991.

[10] R. J. Van De Plassche and H. J. Schouwenaars, "A Monolithic 14 Bit A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 17, pp. 1112-1117, 1982.

[11] H. S. Lee, D. A. Hodges and P. R. Gray, "A Self-Calibrating 15 bit CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 813-819, 1984.

[12] P. W. Li, M. J. Chin, P. R. Gray and R. Castello, "A Ratio-Independent Algorithmic Analog-to-Digital Conversion Technique," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 828-836, 1984.

[13] H. Onodera, T. Tateishi and K. Tamarur, "A Cyclic A/D Converter That Does Not Require Ratio-Matched Components," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 152-158, 1988.

[14] D. G. Nairn, "Current-Mode Algorithmic Analog-to-Digital Converters," *Ph.D. Thesis*, EE Dept., University of Toronto, 1989.

[15] A. M. Cujec, "An Optimized Bit Cell Design For A Pipelined Current-Mode Algorithmic A/D Converter," *M.A.Sc. Thesis*, EE Dept., University of Toronto, 1991.

[16] K. Kusumoto, A. Matsuzawa and K. Murata, "A 10-b 20-MHz 30-mW pipelined interpolating CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 1200-1206, 1993.

[17] K. Nakamura, M. Hotta, R. Carley and D. Allstot, "A 85-mW, 10-bit 40-Ms/s ADC with Decimated Parallel Architecture," *IEEE Custom Integrated Circuits Conference*, pp. 495-498, 1994.

[18] K. Satou, K. Tsuji, M. Sahoda and H. Otsuka, "12 bit 1 MHz ADC with 1 mW power consumption," *IEEE Custom Integrated Circuits Conference*, pp. 515-518, 1994.

[19] Z. Liqang, T. Sculley and T. Fiez, "A 12 bit, 2 V current-mode pipelined A/D converter using a digital CMOS process," *IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 369-372, 1994.

[20] K. L. Fong and C. A. T. Salama, "Low-power current-mode algorithmic ADC," *IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 473-476, 1994.

[21] H. Hasegawa, M. Yotsuyanagi, M. Yamaguchi and K. Sone, "A 1.5 V video-speed current-mode current-tree A/D converter," *IEEE Symposium on VLSI Circuits*, pp. 17-18, 1994.

[22] Y. Matsuya and J. Yamada, "1 V power supply, low-power consumption A/D conversion," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 1524-1530, 1994.

[23] C. C. Chen, C. Y. Wu and J. J. Cho, "A 1.5 V CMOS current-mode cyclic analog-to-digital converter with digital error correction," *IEEE Symposium on Circuits and Systems*, vol. 1, pp. 537-540, 1995.

[24] P. van Gog, B. Kup and R. van Osch, "A Two-Channel 16/18b Audio AD/DA Including Filter Function with 60/40 mW Power Consumption at 2.7 V," *IEEE International Solid-State Circuits Conference*, pp. 208-209, 1995.

[25] A. Kitagawa, T. Kokubo, T. Tsukada, T. Matsuura, M. Hotta, K. Maio, E. Yamamoto and E. Imaizumi, "A 10 b 3 Msamples/s CMOS Cyclic ADC," *IEEE International Solid-State Circuits Conference*, pp. 280-281, 1995.

[26] M. Yotsuyanagi, H. Hasegawa, M. Yamaguchi, M. Ishida and K. Sone, "A 2 V 10 b 20 Msamples/s Mixed-Mode Subranging CMOS A/D Converter," *IEEE International Solid-State Circuits Conference*, pp. 282-283, 1995.

[27] S. Rabii and R. Wooley, "A 1.8 V, 5.4 mW, Digital-Audio ΣΔ Modulator in 1.2 μm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 228-229, 1996.

[28] J. Grilo, E. MacRobbie, R. Halim and G. Temes, "A 1.8 V 94 dB Dynamic Range ΔΣ Modulator for Voice Applications," *IEEE International Solid-State Circuits Conference*, pp. 230-231, 1996.

[29] E. van der Zwan and E. Dijkmans, "A 0.2mW CMOS ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range," *IEEE International Solid-State Circuits Conference*, pp. 232-233, 1996.

[30] P. C. Yu and H. S. Lee, "A 2.5 V 12 b 5Msamples/s Pipelined CMOS ADC," *IEEE International Solid-State Circuits Conference*, pp. 314-315, 1996.

[31] H. Hasegawa, M. Yotsuyanagi, M. Satoh, S. Kishi, M. Ishida and M. Yamaguchi, "A 1.5 V 8 b 8 mW BiCMOS Video A/D Converter," *IEEE International Solid-State Circuits Conference*, pp. 322-323, 1996.

[32] H. Neuteboom, M. Janssens, J. Leenen, B. Kup, E. Dijkmans, B. de Koning, V. Frowijn, R. De Bleecker, E. van der Zwan, S. Note, Z. Wu and M. Masschelein, "A Single Battery, 0.9 V-Operated Digital Sound Processing IC Including AD/DA and IR Receiver with 2mW Power Consumption," *IEEE International Solid-State Circuits Conference*, pp. 98-99, 1997.

[33] M. Horowitz, T. Indermaur and R. Gonzalez, "Low-Power Digital Design," *IEEE Symposium on Low Power Electronics*, pp. 8-11, 1994.

[34] L. Di Pede, "A 1V Low-Power CMOS Process," *M.A.Sc. Thesis*, EE Dept., University of Toronto, 1998.

[35] K. Tsukamoto, T. Watahiki and T. Miyata, "A Floating-Point A/D Converter Using Switched-Capacitor Array," *Electronics and Communications in Japan*, vol. 69, pp. 68-75, 1986.

[36] R. Burrier, R. Mangiapane, J. Rhodes, R. Duris and C. Sabolis, "Floating-Point Converter Uses Hardware to Get a 20-bit Dynamic Range," *Electronic Design*, vol. 32, pp. 175-186, 1984.

[37] F. Goodenough, "Floating-Point CMOS ADC Takes 16-bit Dynamic-Range Inputs," *Electronic Design*, vol. 35, pp. 47-50, 1987.

[38] F. Chen and C. S. Chen, "A 20-b Dynamic-Range Floating-Point Data Acquisition System," *IEEE Transactions on Industrial Electronics*, vol. 38, pp. 10-14, 1991.

[39] C. Toumazou, J. Lidgey and D. Haigh, *Analogue IC Design: the current-mode approach*, Peter Peregrinus Ltd., London 1990.

[40] Takayuki Hayashi and C. A. T. Salama, "A 1 V Floating-Point ADC for Portable Communication Devices," *IEEE International Symposium on Circuits and Systems, accepted for publication*, 1998.

CHAPTER 2

Floating-Point ADC Architecture

2.1 Introduction

In a conventional ADC, the quantizing steps remain constant throughout the entire range as shown in Fig. 2.1 (a), leading to a deteriorating signal-to-quantizing error ratio with decreasing input signal amplitude [1]. An attempt to increase the number of bits or resolution to improve this ratio results in the redundancy of digital data at higher input signals. This problem can be overcome by employing a floating-point ADC (FADC) which has non-uniform quantizing steps. As shown in Fig. 2.1 (b), the quantizing step size in a FADC decreases as the input signal amplitude is reduced, leading to a relatively constant signal-to-quantization error ratio throughout the entire range. It is important to note that although the quantizing steps are non-uniform, there is still a linear relationship between the analog input and the digital output. Therefore, a conventional DAC is all that is required to recover the analog signal.

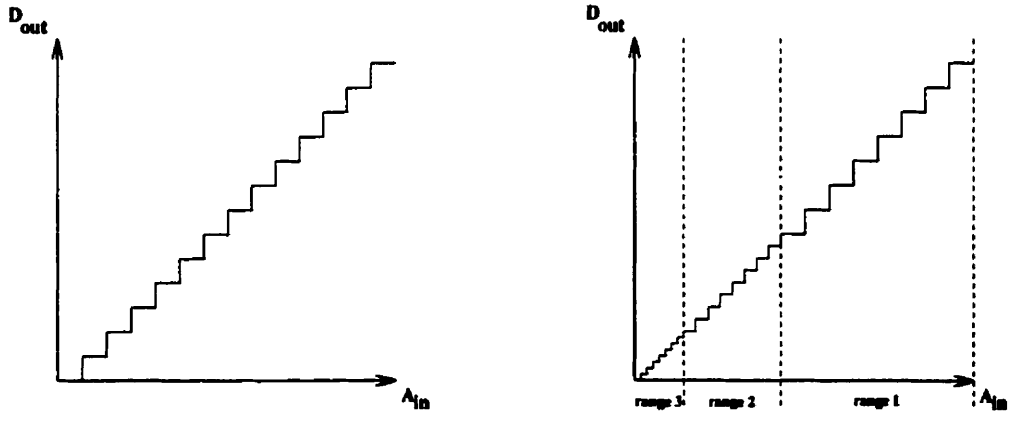


Fig. 2.1 I/O Response of (a) Conventional ADC and (b) Floating-Point ADC

2.2 Floating-Point Analog-to-Digital Conversion Algorithm

The floating-point conversion is performed using the algorithm shown in Fig. 2.2 (a) [2]. The process requires two separate A/D conversions: exponent and mantissa. The full-scale input range of the FADC, shown in Fig. 2.2 (b), is divided into different gain ranges. The top half of the scale is called gain range 1, the next quarter section is called gain range 2 and the size of every succeeding gain range decreases by a factor of a half. For simplicity, the FADC in this example has only six gain ranges.

The first step in the conversion process is to determine the gain range of the input. For example, if the input lies somewhere between 1/2 and 1/4 of the full-scale input, its gain range is 2. Similarly, the input is considered to be in gain range 6 if it is less than 1/32 of the full-scale input. To find the correct gain range, the exponent A/D conversion is used. This does not require a high resolution. It only needs enough precision to resolve the smallest gain range.

The next step is to amplify the input according to the gain range number. For example, if the result of the exponent A/D conversion reveals that the input lies somewhere in gain range 3, the input must be amplified by four which is the largest factor it can be multiplied by without exceeding the full-scale input range of the FADC.

The final step is to perform the mantissa A/D conversion of the amplified input. This conversion is used to determine the exact value of the input within the gain range found by the exponent A/D conversion. The two outputs, the exponent and mantissa, represent the output code in a floating-point representation. By bit shifting the mantissa part by the exponent part, fixed-point representation of the output can be obtained.

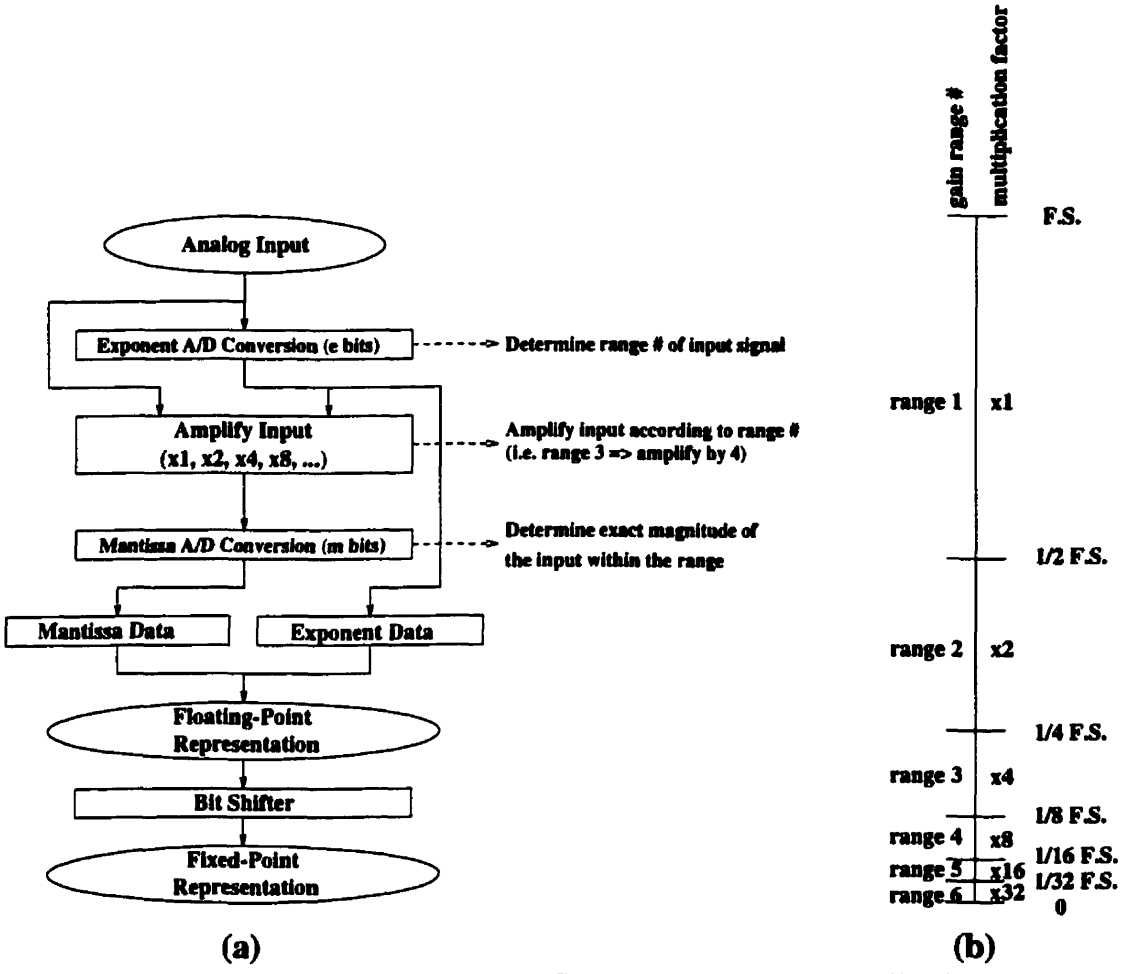


Fig. 2.2 (a) Flowchart of Floating-Point Conversion and (b) Multiplication Factors

The dynamic range, which is defined as the ratio of the full-scale input range to the smallest signal the ADC can detect, is expressed as

$$\text{Dynamic Range} = \text{number of gain ranges} + \text{mantissa resolution} - 1 \qquad (2.1)$$

Therefore, one can build a wide dynamic range ADC using only low-resolution components. For example, a 16-bit dynamic range ADC can be built using a 6-bit ADC for the exponent A/D conversion which provides seven gain ranges and a 10-bit ADC for the mantissa A/D conversion. This ADC does not have a 16-bit accuracy; it only has the ability to resolve signals as small as 2^{-16} of the full-scale input.

2.3 Block Diagram of a Floating-Point ADC

The block diagram of a current-mode FADC is shown in Fig. 2.3. With five gain ranges and an 8-bit resolution for the mantissa, this FADC has a dynamic range of 12 bits.

Several building blocks are necessary to implement an integrated FADC. In most designs, the exponent and the mantissa A/D conversion are accomplished using two separate ADCs. Usually, a fast low/medium-resolution flash ADC is used for the exponent A/D conversion and a high-resolution ADC is employed for the mantissa A/D conversion [3,4,5]. For the design in this thesis, a current-mode algorithmic 8-bit ADC cell is used for both the exponent and the mantissa conversion to conserve circuit area and power. This is the primary block of the FADC since the accuracy and the speed of the ADC cell directly influence the overall performance. A shift register is required at the output of the ADC cell since the cell performs the conversion serially as discussed in Section 2.4.2.2. The other major block is the current-mode Programmable Gain Amplifier (PGA) which has a total of five gain ranges. The gain selection of the PGA is governed by the encoder circuit. The 5-bit register is used to store the output from the exponent A/D conversion during the mantissa A/D conversion. The 12x5 Barrel shifter is required to convert the output from floating-point representation into fixed-point representation. Finally, a control circuit (not shown in the figure) is necessary to control the external switches S9 (closed during the exponent A/D conversion) and S10 (closed during the mantissa A/D conversion) and the internal switches in the ADC cell. The design of each building block is discussed in the following sections.

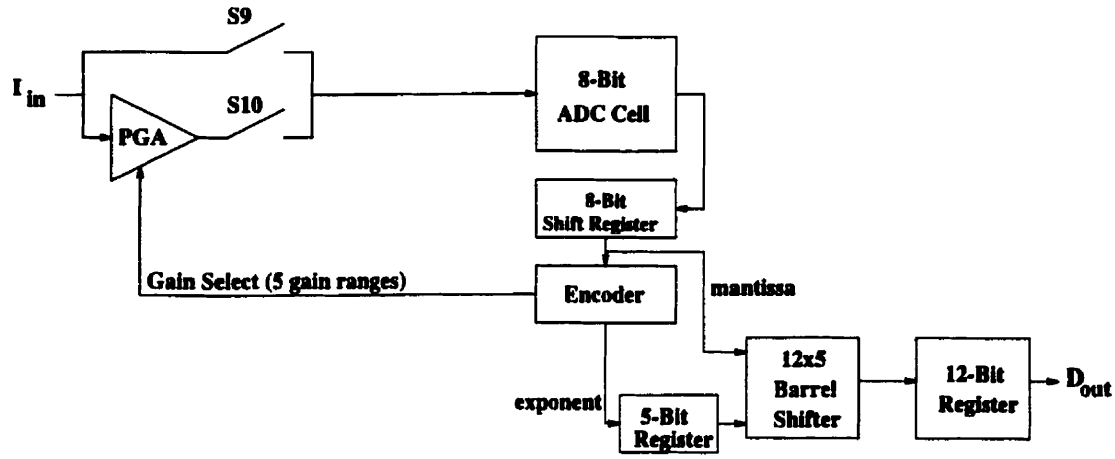


Fig. 2.3 Block Diagram of 12-bit Dynamic Range FADC Employing an 8-bit ADC Cell

2.4 Analog-to-Digital Converter Cell

The ADC cell is the most crucial part of the FADC since it largely determines the overall performance of the system. Although any of the architectures discussed in Chapter 1 can be used to implement the cell, the algorithmic approach is chosen here because of its low power consumption, medium resolution, moderate speed and small circuit area.

2.4.1 Algorithmic Conversion

The operation of an algorithmic converter is shown in Fig. 2.4. The first step in the conversion process is to compare the input signal Y_k to the reference signal Y_{REF}. If the input signal is greater than the reference signal, the digital output D_k is set to "1" and the difference between Y_k and Y_{REF} is doubled before becoming the new input signal Y_{k+1}. If the input signal is less than the reference signal, on the other hand, D_k is set to "0" and $2\cdot(Y_k)$ becomes Y_{k+1}. The first digital output represents the MSB and the conversion process must be repeated in order to determine the remaining bits from MSB-1 to LSB.

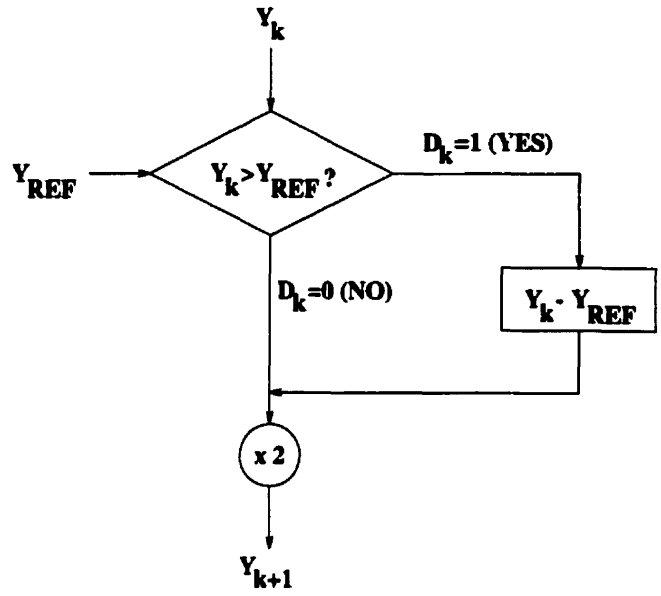


Fig. 2.4 Flow Chart of the Algorithmic Conversion Method

The operation can be summarized using the following equations

$$D_k = \begin{pmatrix} 0, Y_k < Y_{REF} \\ 1, Y_k > Y_{REF} \end{pmatrix} \tag{2.2}$$

$$Y_{k+1} = 2(Y_k - Y_{REF} \times D_k) \tag{2.3}$$

2.4.2 Current-Mode Ratio-Independent Algorithmic ADCs

The ADC cell in this thesis is based on the algorithmic ADCs designed by D. G. Nairn [6] and A. M. Cujec [7]. Both designs incorporate current-mode and ratio-independent techniques.

2.4.2.1 Nairn's Design [6]

The current-mode ADC designed by Nairn is shown in Fig. 2.5 [6]. The ADC takes four clock cycles to complete a bit conversion. During the first cycle, the input current I_{in} is sampled using transistor N1 and capacitor C1 by closing switches S1, S2 and S3. Similarly, during the second cycle, the same input current is sampled using transistor N2

and capacitor C2 by closing switches S1, S4 and S5. Transistor P1 then samples the current stored in N1 and N2 by closing switches S2, S4, S6 and S7 to effectively double the input current. During the final cycle, with switches S6 and S8 closed, the current in P1 and the reference current I_{ref} are compared using the current comparator to determine the digital output D_{out}. If the reference current is greater, D_{out} is set to "0", otherwise D_{out} is set to "1". If D_{out} is "0", the current in P1 is used as the input for the next conversion cycle. On the other hand, if D_{out} is "1", the difference between the current in P1 and the reference current is used as the new input by closing switch S8. The clocking scheme for the switches is shown at the bottom of Fig. 2.5. The algorithm used in this ADC is slightly different from the approach explained in Fig. 2.4. Here, the input signal is multiplied by two before the comparison to the reference signal. As a result, the maximum input signal is equal to the reference signal instead of twice the reference signal.

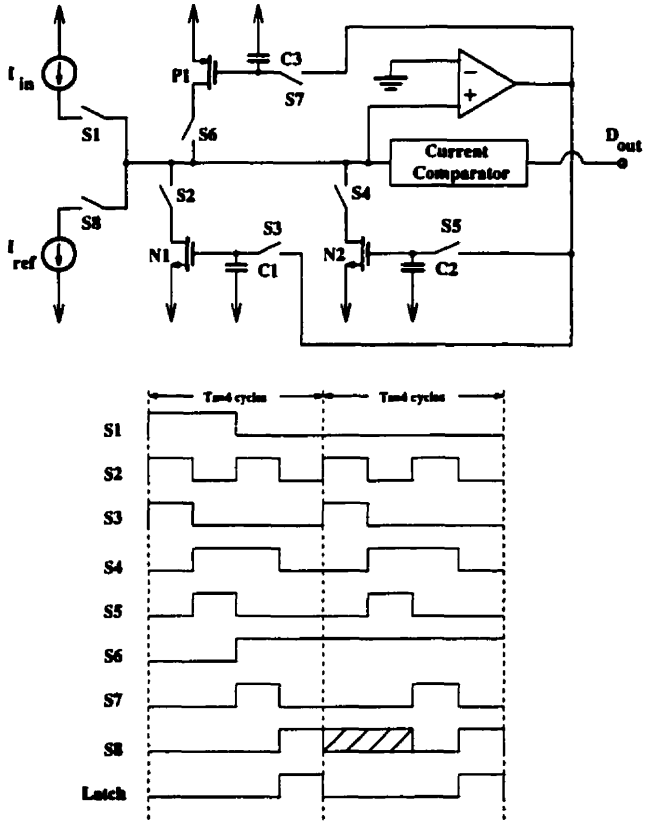


Fig. 2.5 Nairn's Design [6]

This ADC possesses two characteristics that improve the accuracy of the cell. First, active current mirrors are employed to enhance the current matching by reducing the mirror's input resistance [6]. Second, the current mirrors in the ADC are insensitive to device mismatches since the same transistor is used as both the input and the output transistor. During the sampling cycle, the feedback path from the op-amp to the gate of the transistor is closed and the appropriate voltage is stored on the capacitor at the gate. During the sourcing cycle, with the feedback loop opened and the gate voltage unchanged, the transistor acts as a constant current source.

The circuit implemented by Nairn used a 3 μm CMOS process [6]. It achieved a sampling rate of 25 kHz and a resolution of 10 bits while dissipating 3.5 mW. It occupied an area of 0.18 mm^2 and 0.14 mm^2 for the main circuit and the control logic respectively.

2.4.2.2 Cujec's Design [7]

Cujec implemented on an improved algorithmic ADC, shown in Fig. 2.6, using a pipelined architecture [7]. This ADC also takes four cycles to complete a bit conversion using the clocking scheme shown at the bottom of Fig. 2.6. During the first cycle, I_{bias1} - I_{in} is sampled using transistor N1 and capacitor C1 by closing switch S4. The second cycle is used to compare the input current to the reference current I_{ref} by opening switch S4 and closing switch S3. If the input is greater than the reference, D_{out} is set to "1", otherwise D_{out} is set to "0". During the third cycle, I_{in} + I_{bias2} is sampled by transistor N2 and capacitor C2 by closing switches S1 and S5. If D_{out} was high in the previous cycle, the reference must be subtracted from I_{in} by closing switch S3. For the final cycle, switches S2 and S6 are closed to sample I_{in} + I_{bias2} in transistor N3 and capacitor C3. When the two S7 switches are closed at the beginning of a new cycle, $2 \cdot (I_{in})$ is passed on to the following bit cell, successfully completing the multiply-by-two function. During the first, third and fourth cycle, erroneous voltages can be stored on the capacitors if switches S1, S2, S3 and

S7 are opened before gate switches S4, S5 and S6 are closed. Therefore, it is critical to ensure that gate switches are closed slightly before the end of the cycle.

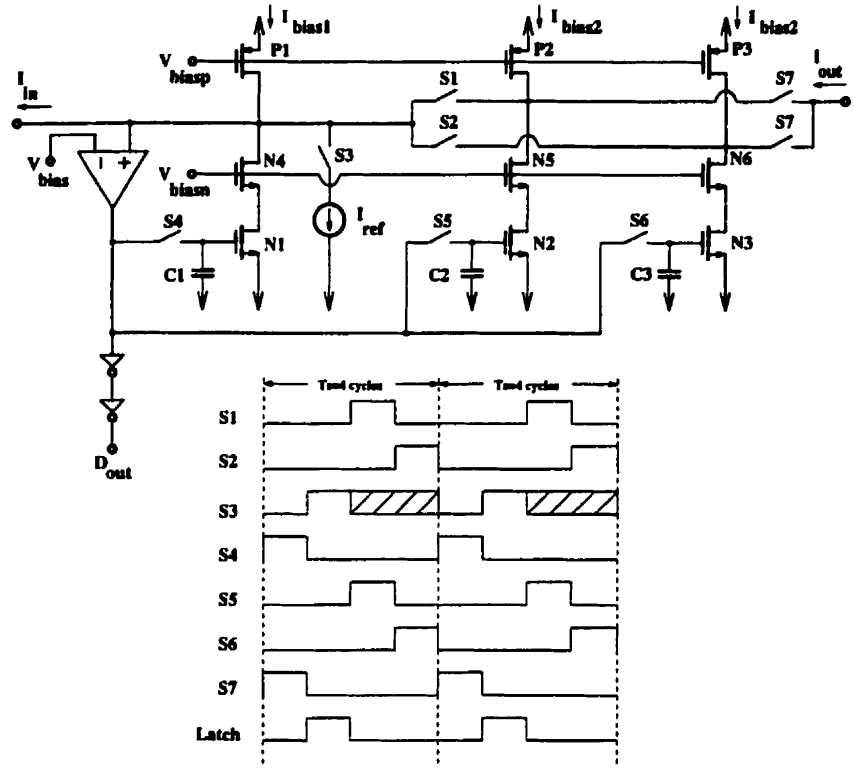


Fig. 2.6 Cujec's Design [7]

This design has a number of advantages over the Nairn's design. First, bias transistors P1, P2 and P3 are used to bias the three active current mirrors so that even if the input current is very small, the speed of the circuit is not compromised. Second, cascode transistors N4, N5 and N6 ensure that voltage swings at the input and the output node are not partially transmitted to the gate of transistors N1, N2 and N3, causing incorrect voltages to be stored on the gate capacitors. Finally, both the bias and the cascode transistors help maintain a constant output impedance. The output impedance can be approximated to be the output impedance r_o of the bias transistor since the impedance of the N-cascode branch is so much greater. Therefore, regardless of the current in the N-cascode branch, the output impedance remains relatively constant. On the other hand, in the simple transistor case, the output impedance is inversely proportional to the current that it is sourcing.

Using this ADC cell, a 10-bit pipelined current-mode algorithmic ADC was implemented in a 1.2 μm CMOS process [7]. The ADC cell occupied an area of 0.066 mm^2 each while the total area of the complete pipelined ADC was 6.5 mm^2. Overall, it achieved a sampling rate of 83 kHz and a power dissipation of 24.5 mW.

2.4.3 Low-Power Low-Voltage ADC Cell Design

A modified version of Cujec's design, shown in Fig. 2.7, is employed for the ADC cell in this work. A connection is added between the input and the output of the cell to effectively convert it from a pipeline bit cell to a stand-alone cell. In addition, cascode transistors N4, N5 and N6 in Fig. 2.6 are removed to allow greater signal swings. Finally, the amplifier in the cell is completely redesigned as discussed in Section 2.4.4.

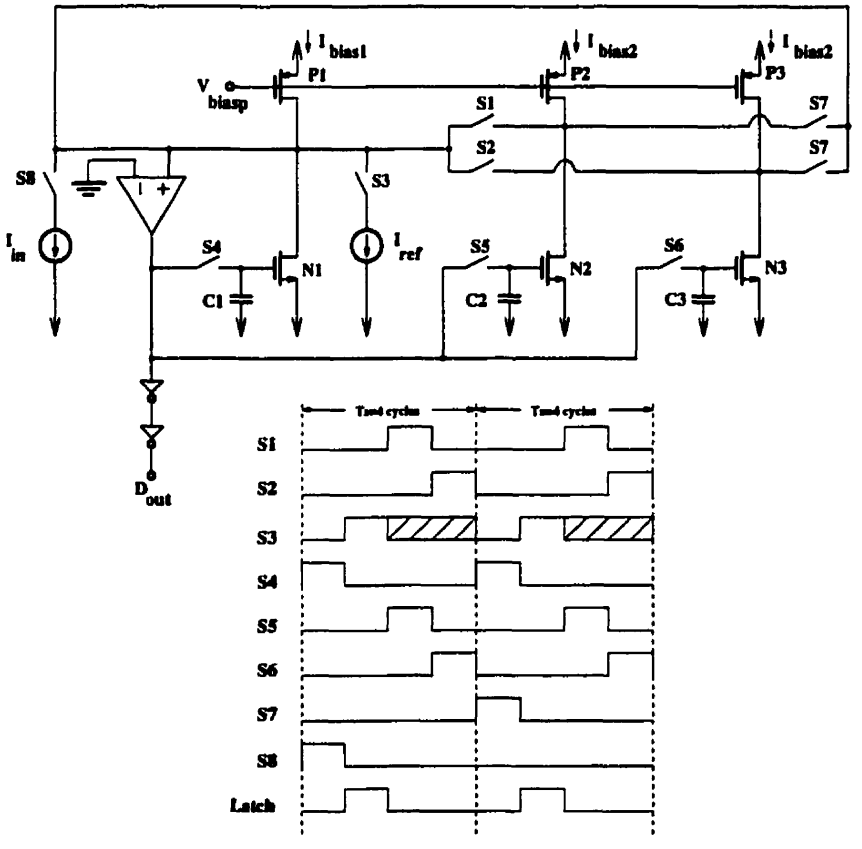


Fig. 2.7 Revised ADC Cell Design

The low-power CMOS process used in the fabrication of this design has a higher leakage current than a standard 5 V process as discussed in Chapter 1. As a result, there is some leakage through the switches when they are suppose to be turned off, leading to a degradation of accuracy. Therefore, although the design is very similar to the one by Cujec, the resolution of this cell is limited to approximately 8 bits.

To ensure that the ADC cell achieves the required resolution of 8 bits, charge-injection errors must be minimized [8,9]. This can be accomplished in one of two ways. The first approach is to increase the size of the gate capacitors C1, C2 and C3, which leads to slower settling times [6]. The other approach is to use a charge-injection cancellation scheme such as dummy transistors or capacitor dividers [7]. The first method is chosen since charge-injection errors can be easily controlled by using moderately sized capacitors. The minimum capacitor size is chosen so that the charge-injection errors are kept below the level of 1 LSB [10]. With a reference current of 25 μA, the maximum input current is 50 μA and the minimum current (1 LSB) is

$$I_{min} = \frac{I_{max}}{2^8} = \frac{50 \times 10^{-6}}{2^8} = 1.95 \times 10^{-7} A \tag{2.4}$$

Next, assuming that the largest error occurs when the input is zero, the maximum error voltage ΔV caused by I_{min} is given by

$$I_{min} = 1.95 \times 10^{-7} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (\Delta V)^2 = \frac{1.87 \times 10^{-4}}{2} \frac{60 \times 10^{-6}}{2 \times 10^{-6}} (\Delta V)^2 \tag{2.5}$$

where μ_n=380 $cm^2/(V \cdot s)$ and C_{ox}= 4.93x10^{-3} F/m^2. The size of the transistor in the current mirror is assumed to be W=60 μm and L=2 μm. Solving Equation (2.5) for ΔV gives 8.34 mV. The oxide capacitance can be found by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-12}}{7 \times 10^{-9}} = 4.93 \times 10^{-3} \frac{F}{m^2} \quad (2.6)$$

$$C_{ox} W_s L_s = 4.93 \times 10^{-3} \times 5 \times 10^{-6} \times 0.5 \times 10^{-6} = 1.23 \times 10^{-14} F \quad (2.7)$$

where T_{ox}=7x10^{-9} m and the size of the switch is chosen to be W_s=5 μm and L_s=0.5 μm. If the control signal waveform of the switch is very fast, the channel charge will flow equally out through both junctions [11]. If transmission gates are used for the switches, the total channel charge is the sum of the charge for P-type and N-type transistor. They are given by

$$Q_n = \frac{(V_{gs} - V_{tn}) C_{ox} W_s L_s}{2} = \frac{(1.0 - 0.32) \times 1.23 \times 10^{-14}}{2} = 4.19 \times 10^{-15} C \quad (2.8)$$

$$Q_p = \frac{(V_{gs} - V_{tp}) C_{ox} W_s L_s}{2} = \frac{(0 - 0.32) \times 1.23 \times 10^{-14}}{2} = -1.97 \times 10^{-15} C \quad (2.9)$$

$$Q_T = Q_n + Q_P = 2.22 \times 10^{-15} C \quad (2.10)$$

where transistor threshold voltage V_{tn} and V_{tp} are assumed to be 0.32 V and -0.32 V respectively and V_{gs} is the gate-to-source voltage of the transistor in the switch. When the switch is closed, V_{gs} is Vdd (1V) for N-type transistor and Vss (0V) for P-type transistor. Note that the use of transmission gates reduces the total channel charge since Q_n and Q_p have a different polarity. Finally, using ΔV from Equation (2.5), the minimum capacitor size can be determined using

$$C_{min} = \frac{Q_T}{\Delta V} = \frac{2.22 \times 10^{-15}}{8.34 \times 10^{-3}} = 0.27 pF \quad (2.11)$$

Therefore, gate capacitors C1, C2 and C3 must be at least 0.27 pF in order to reduce the effects of charge-injection errors. They are chosen to be 3 pF for this design since larger capacitors also reduce the effects of kT/C noise [6].

Table 2.1 lists the transistor sizes for the ADC cell. Device sizes for the transmission gate switches are shown in Table 2.2. All the switches are designed with minimum length transistors for fast switching times. Switches S1, S2, S3 and S7 are made with wide transistors to reduce the voltage drop across them while switches S4, S5 and S6 are kept small to reduce the effects of charge injection.

Table 2.1 Device Sizes for ADC Cell

Device	Type	W (μm)	L (μm)
P1	P	160	2
P2	P	50	2
P3	P	50	2
N1	N	60	2
N2	N	60	2
N3	N	60	2

Table 2.2 Device Sizes for Switches in ADC Cell

Switch	Type	W (μm)	L (μm)
S1, S2	P	20	0.5
S3, S7	N	20	0.5
S4, S5	P	5	0.5
S6	N	5	0.5

2.4.4 Amplifier Design

The ADC cell uses active current mirrors to improve the cell's accuracy. The most crucial part of the active current mirror is the op-amp since the accuracy of the mirror is dependent on the open-loop gain of the amplifier. In addition, the settling behaviour of the amplifier determines the speed of the active current mirror.

The required open-loop gain of the op-amp can be determined using the current transfer function [6]

$$\frac{\Delta I}{I_{IN}} = \frac{1}{gm_n r_o A_V} \tag{2.12}$$

where $\Delta I = I_{in} - I_{out}$, gm_n and r_o are the transconductance and the output impedance of the transistor in the current mirror respectively and A_v is the open-loop gain of the op-amp. Assuming $gm_n \approx 200\ \mu A/V$ and $r_o \approx 250\ k\Omega$, a gain of only 14 dB is required to achieve an accuracy of 0.4% or a resolution of 8 bits. Note that a simple current mirror (A = 1) can only achieve a 0.2% accuracy or a 6-bit resolution.

Since the required gain is relatively small, a simple differential-pair amplifier shown in Fig. 2.8 is chosen. The simplicity in the design also allows wide signal swings which are essential in low-voltage designs.

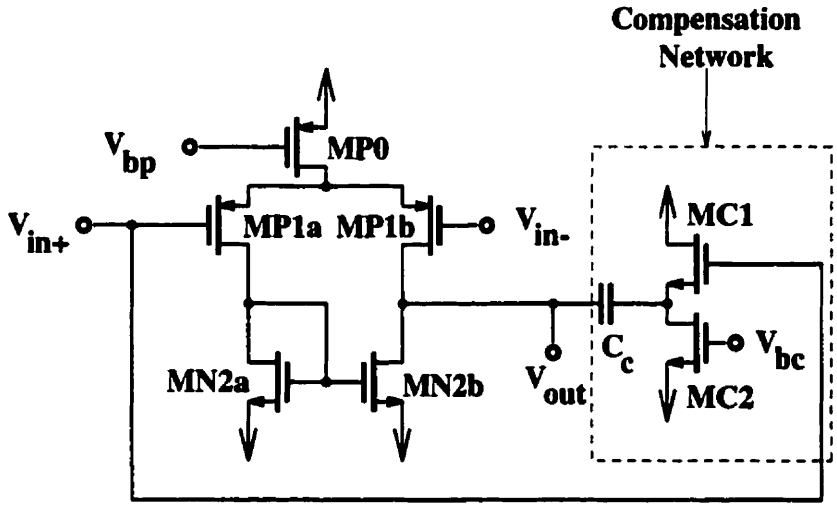
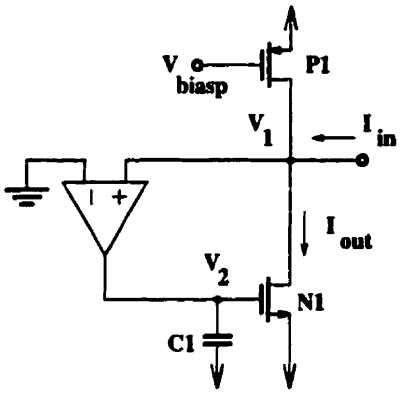


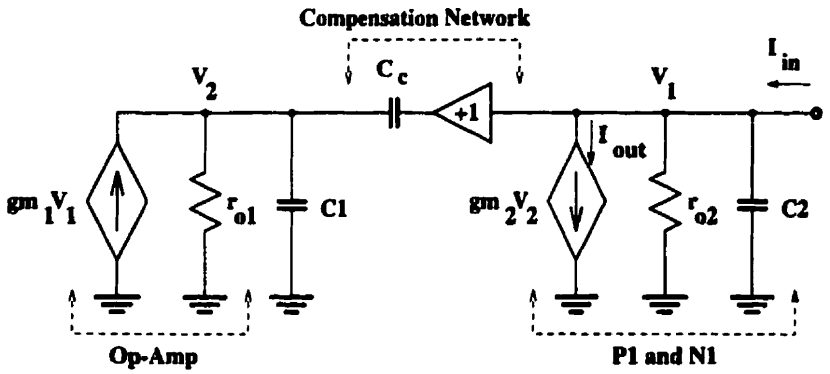
Fig. 2.8 Op-Amp Design for ADC Cell

Although the op-amp only has single gain stage, compensation is necessary because the current mirror at the output of the op-amp behaves like a second gain stage as shown in Fig. 2.9 (a). The conventional R-C compensation network is not suitable for this application because of the large variation in the current flowing through transistor N1,

making it difficult to match R to the inverse of the transconductance of N1. A compensation network consisting of a capacitor and a source follower is employed instead, eliminating the need for a signal dependent network [12].



(a)



(b)

Fig. 2.9 (a) Active Current Mirror and (b) Small-Signal Model

The compensation capacitor C_c can be determined from the small-signal model of the active current mirror shown in Fig. 2.9 (b). The op-amp stage on the left is represented by transconductance gm_1 and output impedance r_{o1}. The current mirror stage on the right contains gm_2 which represents the transconductance of transistor N1 and r_{o2} which is the output impedance at node V_1. The transfer function derived from the small-signal model is [7]

$$\frac{I_{out}}{I_{in}} = \frac{\frac{gm_2(gm_1 + sC_c)}{C_2(C_c + C_L)}}{s^2 + s\frac{gm_2C_c}{C_2(C_c + C_L)} + \frac{gm_1gm_2r_{o1}r_{o2} + 1}{r_{o1}r_{o2}C_2(C_c + C_L)}} \tag{2.13}$$

Assuming that the second pole is much larger than the first pole, the two poles can be estimated from Equation (2.13) as

$$\omega_{p1} = -\frac{gm_1gm_2r_{o1}r_{o2} + 1}{gm_2r_{o1}r_{o2}C_c} \tag{2.14}$$

$$\omega_{p2} = -\frac{gm_2C_c}{C_2(C_c + C_L)} \tag{2.15}$$

For $gm_1gm_2r_{o1}r_{o2} >> 1$, $\omega_{p1} \approx -gm_1/C_c$. There is also a zero at

$$\omega_z = -\frac{gm_1}{C_c} \tag{2.16}$$

Therefore, the effect of the first pole is somewhat cancelled by the zero. The value of C_c can be determined by ensuring that ω_{p2} is much larger than ω_{p1}.

The device sizes for the transistors in the op-amp are listed in Table 2.3 while the size of C_c is chosen as 5 pF. Bias voltages V_{bp} and V_{bc} are supplied through external pins so that they can be adjusted after fabrication.

Table 2.3 Device Sizes for Op-Amp

Device	Type	W (μm)	L (μm)
MP0	P	50	1
MP1	P	50	1
MN2	N	50	1
MC1	N	100	15
MC2	N	10	1

2.5 Current-Mode Programmable Gain Amplifier

2.5.1 Basic Structure

The PGA is used to amplify the input signal according to the exponent results as shown in Table 2.4. The current-mode PGA consists of a group of cascaded current multiplier cells. As shown in Fig. 2.10, the PGA has five possible gain factors (x1, x2, x4, x8 and x16) that can be easily selected by closing the appropriate switches. For example, if a gain of four is required, switches S25, S35 and S3 must be closed so that the input current can flow through the two multiply-by-two cells. Since the multiplier cells are composed of active current mirrors as discussed in Section 2.5.2., the direction of the current is reversed between every other multiplier cells. Therefore, two different types of multiply-by-two cells, "odd" and "even", as well as multiply-by-one cells are needed to accommodate the change in the direction of the current.

Table 2.4 Exponent Output and PGA Gain Settings

Input Signal Amplitude (F.S. = Full Scale)	Exponent Output (before Encoder)	PGA Gain Setting
1/2 F. S. ~ F. S.	From 10000 To 11111	x 1
1/4 F. S. ~ 1/2 F. S.	From 01000 To 01111	x 2
1/8 F. S. ~ 1/4 F. S.	From 00100 To 00111	x 4
1/16 F. S.~ 1/8 F. S.	From 00010 To 00011	x 8
0 ~ 1/16 F. S.	From 00000 To 00001	x 16

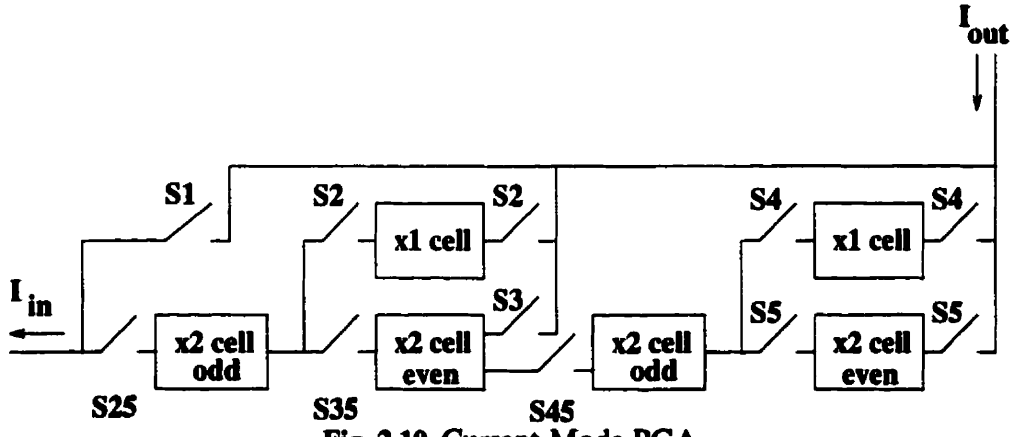


Fig. 2.10 Current-Mode PGA

2.5.2 Current Multiplier Cells

Current multiplier cells consist of active current mirrors as shown in Fig. 2.11. Active-negative feedback approach is used to reduce the current mismatch caused by transistor's finite output impedance [6]. Ratio-independent techniques are not used to mirror currents because of speed considerations. Instead, these cells rely on device matching to produce matched currents and they therefore cannot be expected to achieve an accuracy better than 8 bits [6]. This, however, would not be a problem since the PGA is followed by the ADC cell which has an 8-bit resolution. All the transistor sizes are presented in Table 2.5, Table 2.6 and Table 2.7 and the switch sizes are shown in Table 2.8. The design of the amplifier in the multiplier cells is discussed in Section 2.5.3.

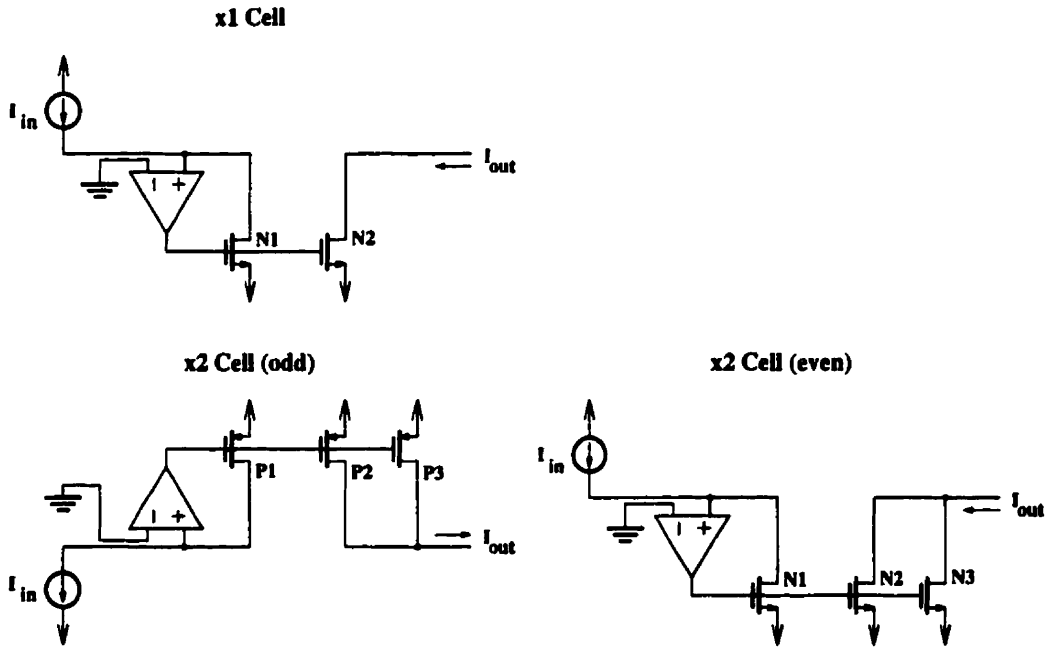


Fig. 2.11 Current Multiplier Cells

Table 2.5 Device Sizes for Multiply-by-one Multiplier Cell

Device	Type	W (μm)	L (μm)
N1, N2	N	25	2

Table 2.6 Device Sizes for Multiply-by-two Multiplier Cell (odd)

Device	Type	W (μm)	L (μm)
P1, P2, P3	P	15	2

Table 2.7 Device Sizes for Multiply-by-two Multiplier Cell (even)

Device	Size	W (μm)	L (μm)
N1, N2, N3	N	3	2

Table 2.8 Device Sizes for Switches in PGA

Switch	Type	W (μm)	L (μm)
All switches	P	20	0.5
	N	20	0.5

2.5.3 Amplifier Design

The amplifier used in the multiplier cells is basically identical to the one used in the ADC cell as shown in Fig. 2.12. The compensation network, however, needs to be redesigned since there are no gate capacitors (C1, C2 and C3 in Fig. 2.7) in the multiplier cells, resulting in a different capacitive loading at the output of the op-amp. Also note that this op-amp and the compensation network can be turned off using switches SB and SC respectively to minimize power dissipation when the PGA is in idle. The device sizes are listed in Table 2.3. The size of C_c is 1 pF.

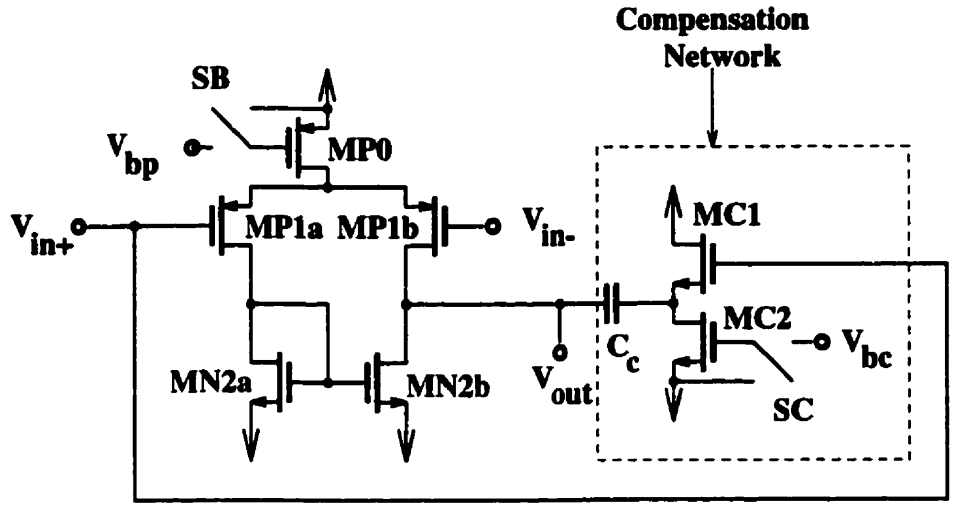


Fig. 2.12 Op-Amp Design for Multiplier Cell

Table 2.9 Device Sizes for Op-Amp

Device	Type	W (μm)	L (μm)
MP0	P	50	1
MP1	P	100	1
MN2	N	5	1
MC1	N	100	1
MC2	N	10	1

2.6 Encoder Circuit

The purpose of the encoder circuit, shown in Fig. 2.13, is to set the gain of the PGA using the exponent results from the ADC cell.

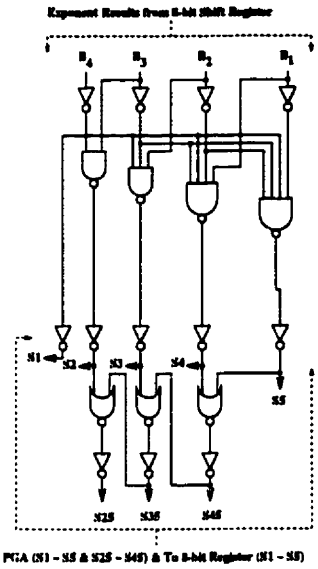


Fig. 2.13 Encoder Circuit

2.7 Control Circuit

The control circuit is divided into two parts: Control Circuit 1 is responsible for generating control signals for the switches in the ADC cell and Control Circuit 2 governs the operation of the external switches. Both control circuits operate from a main clock with a frequency of 8 MHz.

2.7.1 Generation of Control Signals for the Switches in the ADC Cell

Control Circuit 1, shown in Fig. 2.14, generates the control signals for switches S1 ~ S7 in the ADC cell. These signals are generated using a 6-bit synchronous counter and some combinational logic. The signals at different parts of the counter are shown in Fig. 2.15. As discussed in Section 2.4.2.2, it is important for switches S4, S5 and S6 to close slightly before switches S1, S2, S3 and S7 open to ensure that the correct voltages are stored on the gate capacitors. Finally, note that the control signal for switch S3 is dependent on the value of the current digital output D_{out} since switch S3 controls the flow of the reference current in the ADC cell.

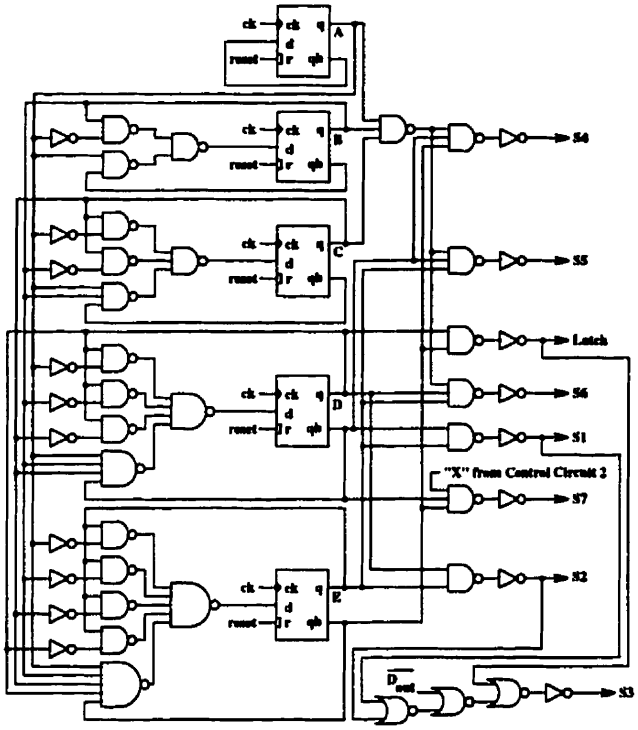


Fig. 2.14 Control Circuit 1

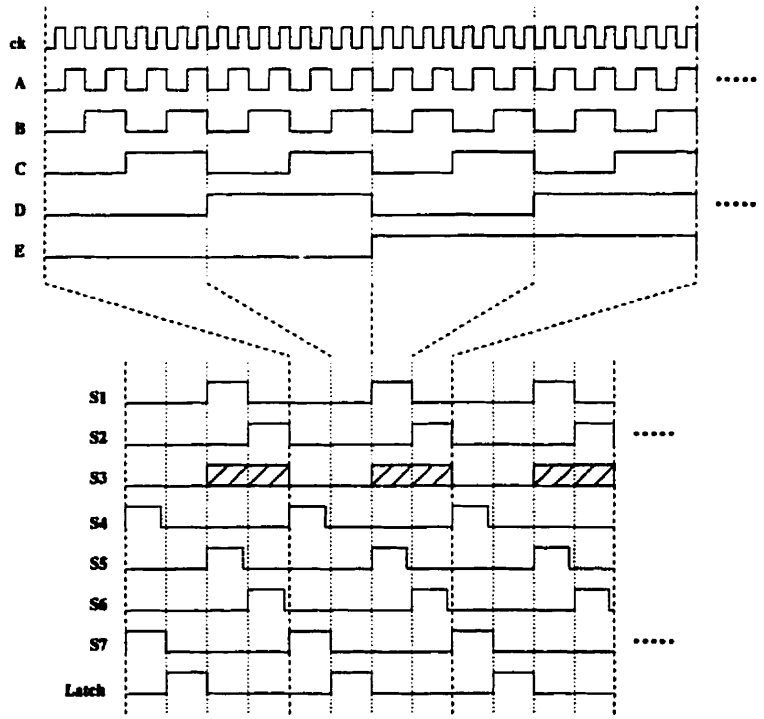


Fig. 2.15 Generation of Control Signals for Switches S1 ~ S7

2.7.2 Generation of Control Signals for the External Switches

Control Circuit 2, shown in Fig. 2.16, is used to generate the control signals for external switches S9 and S10 which remain closed at the beginning of the exponent and the mantissa conversion respectively. The heart of the design is a Pseudo Random Binary Sequence (PRBS) counter [13] which counts up in a non-binary sequence fashion as the name suggests. The output from the counter must be decoded to obtain any meaningful data. When the input is being sampled at the beginning of the exponent stage and amplified at the beginning of the mantissa stage, the "stall" signal is used to hold the operation of Control Circuit 1 by using it as the reset signal for all the flip-flops in the circuit. Table 2.10 shows the counting sequence of the PRBS counter used in this thesis. The counter operates from a 1 MHz clock that is derived from the main 8 MHz clock using some frequency dividers.

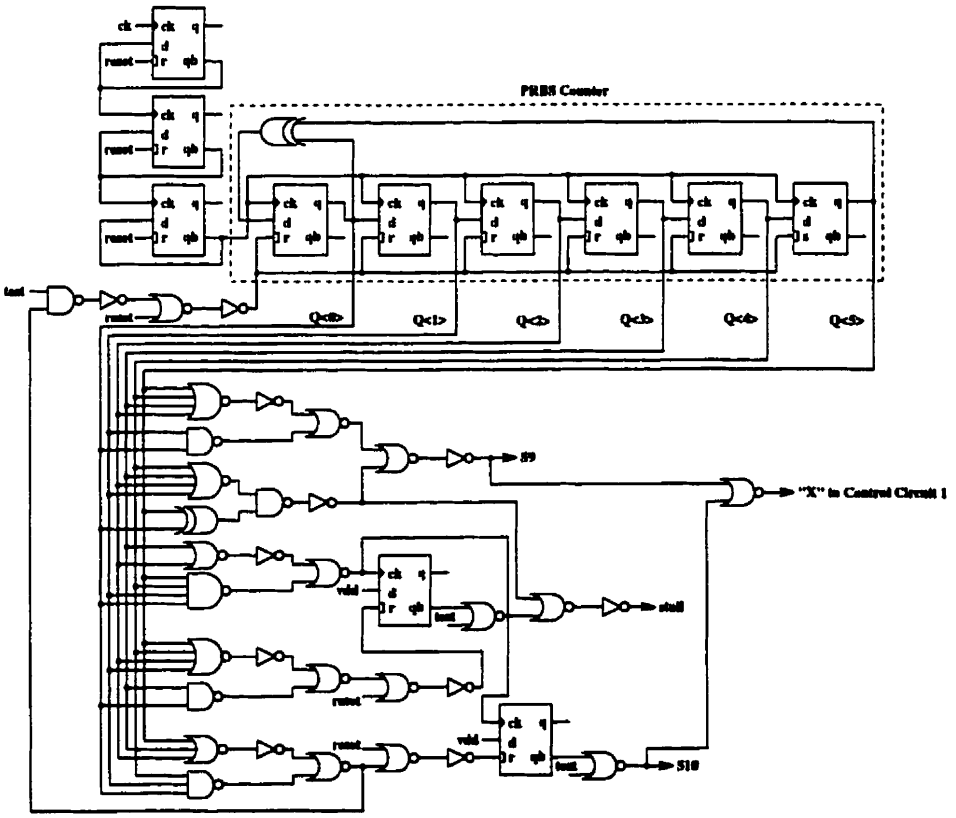


Fig. 2.16 Control Circuit 2

Table 2.10 Counting Sequence of PRBS Counter

Q<5:0>	Comment	Q<5:0>	Comment	Q<5:0>	Comment
100000	Exponent Start				
000001		010110			
000011		101100			
		011001	Exponent Finish		
		110011	PGA Setup		
			&		
		100100	Amplify		
		001001	Mantissa Start		
		010011		000100	
		100111		001000	
				010000	Mantissa Finish

2.7.3 Generated Control Signal Waveforms

The control signals generated from Control Circuit 1 and 2 are shown in Fig. 2.17. The exponent conversion takes 17 µs, followed by the PGA setup and amplification step that takes 15 µs, and finally the mantissa conversion which takes another 31 µs. The total conversion time of 63 µs translates to a sampling rate of 16 kHz.

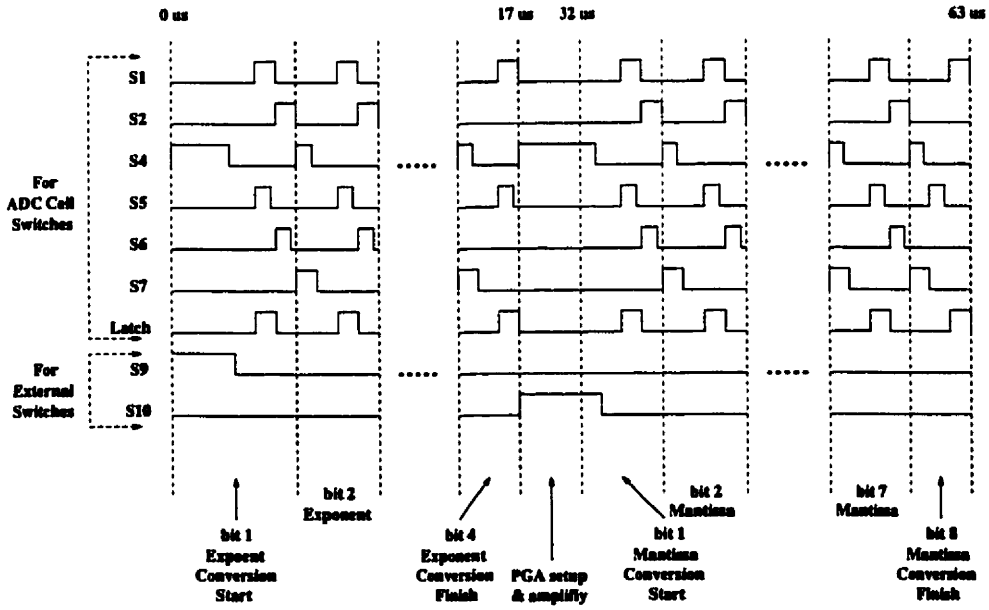


Fig. 2.17 Generated Control Signal Waveforms

2.8 Layout of the FADC

The layout of the complete FADC is shown in Fig. 2.18. The ADC cell is located in the upper left while the lower left shows the PGA. The right hand side contains the control circuit and the encoder. These digital blocks are laid out using standard cells provided by IMEC. The circuit area for each block and the total circuit area are shown in Table 2.11.

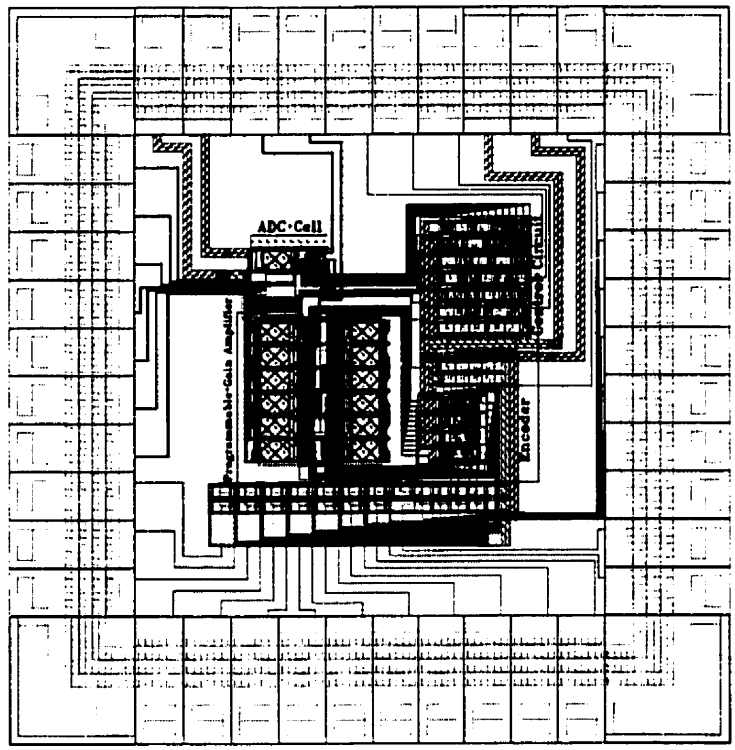


Fig. 2.18 Layout of the FADC

Table 2.11 Circuit Area of Each Block

Component	Circuit Area
ADC Cell	240 µm x 110 µm = 0.03 mm^2
PGA	470 µm x 530 µm = 0.25 mm^2
Encoder	220 µm x 230 µm = 0.05 mm^2
Control Circuit	360 µm x 380 µm = 0.14 mm^2
Total Core Area	1.0 mm x 1.0 mm = 1.0 mm^2
Total Area with 40 I/O Pads	2.3 mm x 2.3 mm = 5.3 mm^2

To minimize the effects of digital noise coupling, some protective layout techniques are employed [14]. First, separate analog and digital pads are used for power and ground to make sure that the analog supply lines are not affected by the noise on the digital supply lines. Second, the analog circuitry and the digital circuitry are laid out as far as possible with guard rings separating them. The rings consist of substrate-bias contacts which provide a low impedance path for noise currents present in the substrate. Finally, an N-well layer is placed under capacitors' bottom plates. The well behaves like a shield against substrate noise when it is connected to a clean power supply.

2.9 Simulation Results of the ADC Cell

The ADC cell was analyzed using ELDO transient simulations. Plots of the current in transistors N1, N2 and N3 (see Fig. 2.7) are shown in Fig. 2.19 and the amplifier output voltage is shown in Fig. 2.20. For both cases, an input current of 20 μA and a reference current of 25 μA are chosen. From 0 μs to 1 μs, the input is sampled by transistor N1. From 1 μs to 2 μs, this input is compared with the reference current. Since the input is smaller than the reference in this case, the amplifier output swings to 0 V indicating a bit "0". From 2 μs to 3 μs and from 3 μs to 4 μs, the difference between the current through transistors P1 and N1 is sampled in transistors N2 and N3 respectively. Finally, from 4 μs to 5 μs, the current in transistors N2 and N3 are combined and the sum is sampled by transistor N1, completing the multiply-by-two function. From the plot, it is observed that each cycle needs at least 1 μs for all the currents to settle down. Since one bit conversion takes four cycles as discussed in Section 2.4.2.2, an 8-bit conversion requires 32 μs or a sampling rate of 30 kHz. For sampling rates above this value, the resolution is limited by the settling time of the amplifier.

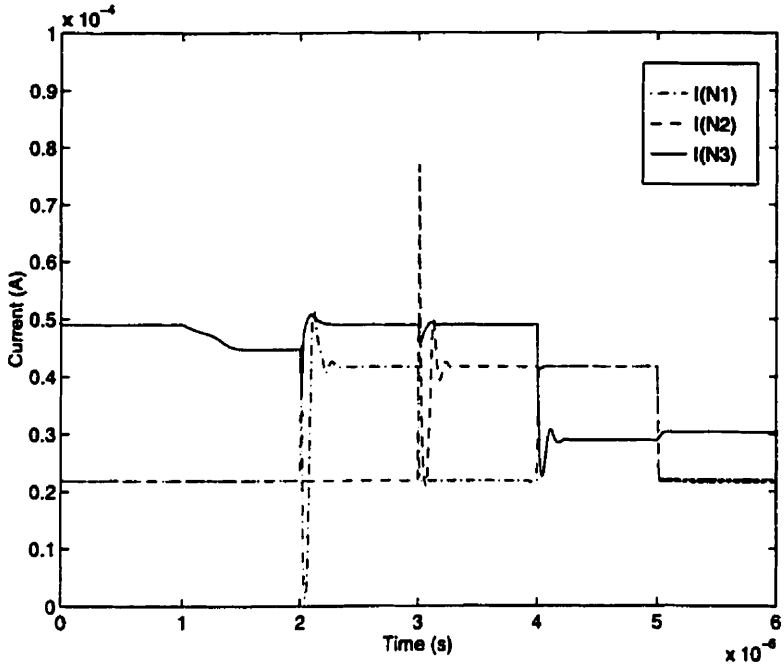


Fig. 2.19 Transient Simulations showing the Currents in ADC Cell

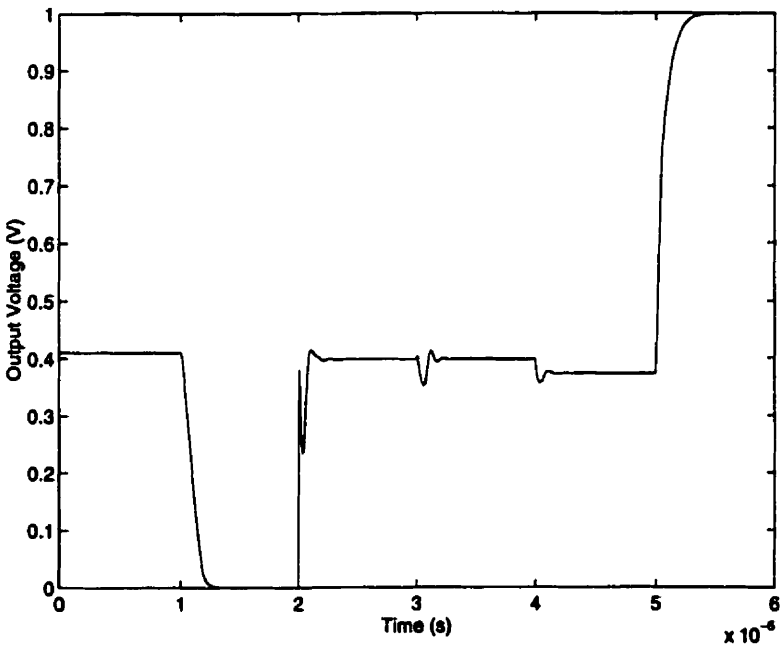


Fig. 2.20 Transient Simulations showing the Amplifier Output Voltage

The resolution is determined by the cell's ability to resolve small currents. The maximum current error should be limited to half the least significant bit or LSB and is defined by [7]

$$\text{Error}_{max} = \Delta I = \frac{I_{FS}}{2^{(N+1)}} \tag{2.17}$$

where ΔI is the current error, I_{FS} is the full scale input (50 μA) and N is the resolution. Rearranging Equation (2.17) and solving for N gives

$$N = \frac{\ln(\frac{I_{FS}}{\Delta I})}{\ln 2} - 1 \tag{2.18}$$

It is found through simulation that the cell can resolve currents within 70 nA, indicating an 8-bit resolution. A plot of the ADC cell's integral nonlinearity and differential nonlinearity are shown in Figs. 2.21 and 2.22 respectively. The worst case nonlinearity for both cases is less than 1 LSB indicating a true 8-bit performance. Due to simulation time constraints, these nonlinearity simulations do not include parasitics.

The power dissipation of the ADC cell is only 170 μW and its characteristics are presented in Table 2.12.

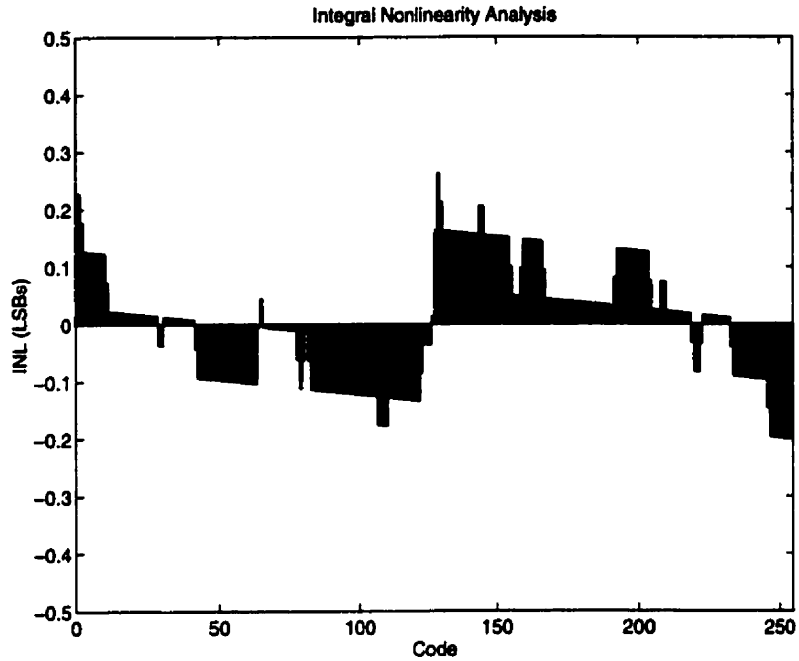


Fig. 2.21 Integral Nonlinearity vs. Code

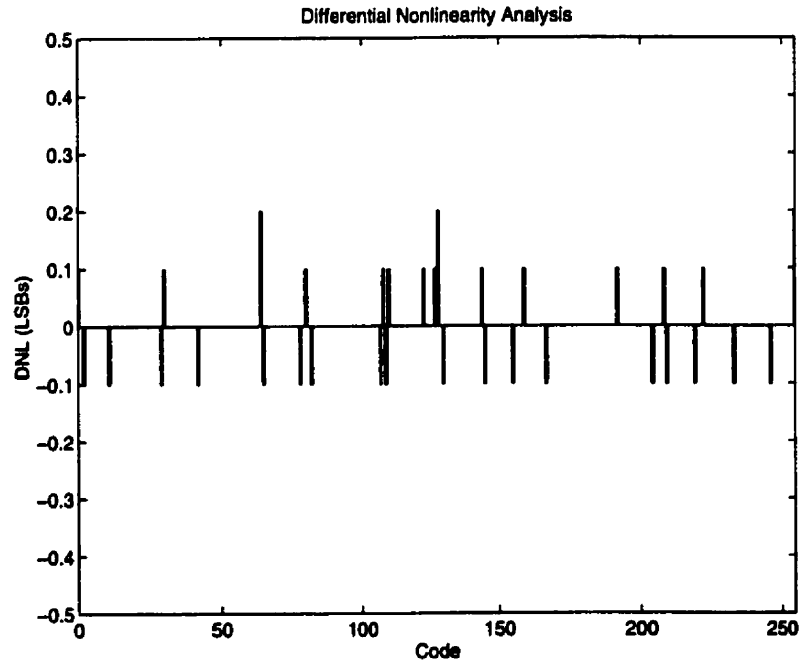


Fig. 2.22 Differential Nonlinearity vs. Code

Table 2.12 ADC Cell Characteristics

Parameter	Simulation Results
Technology	0.5 μm low-power CMOS
Power Supply	1 V
Reference Current	25 μA
Power Dissipation	170 μW
Resolution	8 bit
Conversion Time	32 μs
Gain Error @ full scale	-0.13 LSB
Offset Error	-0.13 LSB
Integral Nonlinearity	
Maximum INL	0.26 LSB
Minimum INL	-0.2 LSB
Differential Nonlinearity	
Maximum DNL	0.20 LSB
Minimum DNL	-0.1 LSB
Missing Codes	0

2.10 Simulation Results of the FADC

Based on the simulation results of the ADC cell, the FADC is expected to achieve a dynamic range of 12 bits while dissipating 470 μW. The conversion time of 63 μs translates to a sampling rate of 16 kHz. The expected characteristics are listed in Table 2.13.

Table 2.13 FADC Characteristics

Parameter	Simulation Results
Technology	0.5 μm low-power CMOS
Power Supply	1 V
Reference Current	25 μA
Power Dissipation	450 μW
Dynamic Range	12 bit
Resolution	8 bit
Conversion Time	63 μs

2.11 Experimental Implementation

The designs were sent to IMEC in December 1996. Unfortunately, IMEC has been unable to date to meet the analog specifications defined for their 0.5 μm, 1 V CMOS process. Therefore, due to time constraints imposed on the completion of the M.A.Sc. degree, it was decided to present the thesis at this point in time without experimental verification of the designs.

2.12 Summary

The architecture and design of the FADC were investigated. The major advantage of using the floating-point technique is the wide dynamic range that can be obtained without requiring any high-resolution components. This is achieved through two separate A/D conversions and an amplification step.

A ratio-independent current-mode algorithmic ADC was chosen for the ADC cell which is the core part of the architecture. Issues such as charge-injection and op-amp design for the ADC cell were considered. Amplification was performed using a current-mode PGA consisting of series of active current mirrors. Also, a control circuit capable of generating non-overlapping signals was proposed

The complete FADC occupies an area of 1 mm^2 without I/O pads. Simulation results revealed that the ADC cell has a resolution of 8 bits, a conversion time of 32 μs and a power dissipation of 170 μW. Extension of the cell's simulation results suggest that the FADC would achieve a dynamic range of 12 bits, a conversion time of 63 μs and a total power dissipation of 450 μW.

2.13 References

[1] S. K. Sharma, G. Otomo, K. Tsukamoto and T. Miyata, "A floating-point A/D converter uses low resolution DAC to get wide dynamic range," *International Journal of Electronics*, vol. 64, pp. 787-794, 1988.

[2] K. Tsukamoto, T. Watahiki and T. Miyata, "A Floating-Point A/D Converter Using Switched-Capacitor Array," *Electronics and Communications in Japan*, vol. 69, pp. 68-75, 1986.

[3] R. Burrier, R. Mangiapane, J. Rhodes, R. Duris and C. Sabolis, "Floating-Point Converter Uses Hardware to Get a 20-bit Dynamic Range," *Electronic Design*, vol. 32, pp. 175-186, 1984.

[4] F. Chen and C. S. Chen, "A 20-b Dynamic-Range Floating-Point Data Acquisition System," *IEEE Transactions on Industrial Electronics*, vol. 38, pp. 10-14, 1991.

[5] D. H. K. Hoe and D. B. Ribner, "An Auto-Ranging Photodiode Preamplifier with 114 dB Dynamic Range," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 187-194, 1996.

[6] D. G. Nairn, "Current-Mode Algorithmic Analog-to-Digital Converters," *Ph.D. Thesis*, EE Dept., University of Toronto, 1989.

[7] A. M. Cujec, "An Optimized Bit Cell Design For A Pipelined Current-Mode Algorithmic A/D Converter," *M.A.Sc. Thesis*, EE Dept., University of Toronto, 1991.

[8] C. Eichenberger, *Charge Injection in MOS Integrated Sample-and-hold and Switched-Capacitor Circuits*, Hartung-Gorre, Konstanz 1989.

[9] M. Chen, Y. Gu and T. Wu, "Weak inversion charge injection in analog MOS switches," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 604-606, 1995.

[10] J. W. Gates, *Research Report*, University of Toronto, 1995.

[11] J. Shieh, M. Patil and B. L. Sheu, "Measurement and Analysis of Charge Injection in MOS Analog Switches," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 277-281, 1987.

[12] Y. P. Tsividis and P. R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation," *IEEE Journal of Solid-State Circuits*, vol. 11, pp. 748-753, 1976.

[13] Flemming Hansen, "Gigabit per second VLSI for Broadband ISDN," *Ph.D. Thesis*, Dept. of Electromagnetic Systems, Technical University of Denmark, 1996.

[14] F. Maloberti, "Layout of Analog and Mixed Analog-Digital Circuits," in *Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing*, Prentice Hall Inc., 1994.

CHAPTER 3

Conclusions

This thesis investigated the design and implementation of a low power low voltage analog-to-digital converter that can be utilized in portable communication devices. The converter was designed to meet some stringent specifications which include low power dissipation, audio signal bandwidth, wide dynamic range and small area. In order to meet these requirements, floating-point and current-mode techniques were employed to achieve the required performance of the converter in a low voltage environment.

By quantizing the input in a non-uniform fashion, the FADC can achieve a wide dynamic range without using high-resolution components. The floating-point architecture consists of two main blocks: the ADC cell and the programmable gain amplifier. A ratio-independent algorithmic ADC was chosen for the ADC cell because it features small area, low power dissipation and insensitivity to device mismatches. From simulation results, the ADC cell had a resolution of 8 bits with a conversion time of 32 μs and a 170 μW power dissipation. The programmable gain amplifier was realized by cascading a series of active current mirrors. Based on extension of the ADC cell's results, it is estimated that the complete FADC would have a dynamic range of 12 bits while dissipating only 450 μW. The total conversion time is expected to be 63 μs which corresponds to a sampling frequency of 16 kHz. The total core area is 1 mm^2.

The FADC designed in this thesis has an input bandwidth that lies in the audio band. Several options are available to improve the speed of the converter. The first approach is to employ a charge-injection cancellation scheme so that the capacitors in the

ADC cell can be made smaller. This will lead to a quicker settling time at the output of the op-amp and as a result, it will shorten the overall conversion time. Examples of charge-injection cancellation scheme include dummy transistors and capacitor dividers.

The second method is to simply replace the ratio-independent algorithmic ADC cell with a faster converter such as flash. If power consumption is a major concern, one can choose a fast, but power hungry, flash ADC for the exponent conversion and use a more power efficient, but slow, converter for the mantissa conversion.

APPENDIX A

Analog-to-Digital Converter Testing Procedures

A.1 Accuracy Measurements

To determine the accuracy of the ADC cell and the complete FADC, the following parameters must be measured [1,2]:

1. Offset Error:	the consistent deviation from the ideal transfer function and appears as a shift in the transfer function
2. Gain Error:	the deviation in the slope of the transfer function from its ideal slope.
3. Integral Nonlinearity:	the deviation of the transfer function from the ideal straight line.
4. Differential Nonlinearity:	the difference between an ideal LSB code width and the actual code width.
5. Resolution:	the number of bits for which both the differential and integral nonlinearities are less than one LSB.

The setup shown in Fig. A.1 must be used to determine these parameters. Hewlett Packard 4155A Semiconductor Parameter Analyzer provides the analog input and the reference current for the ADC under test. A slow ramp signal is selected as the input signal so that it can sweep over the entire input range of the ADC. The clock signal is controlled by Hewlett Packard 33120A Function/Arbitrary Waveform Generator. Finally, the digital output is captured using Audio Precision System Two Dual Domain S2-2322A[1] and then processed using MATLAB to determine the ADC's offset error, gain error, integral nonlinearity and differential nonlinearity.

1. Comprehensive high-performance audio testing system

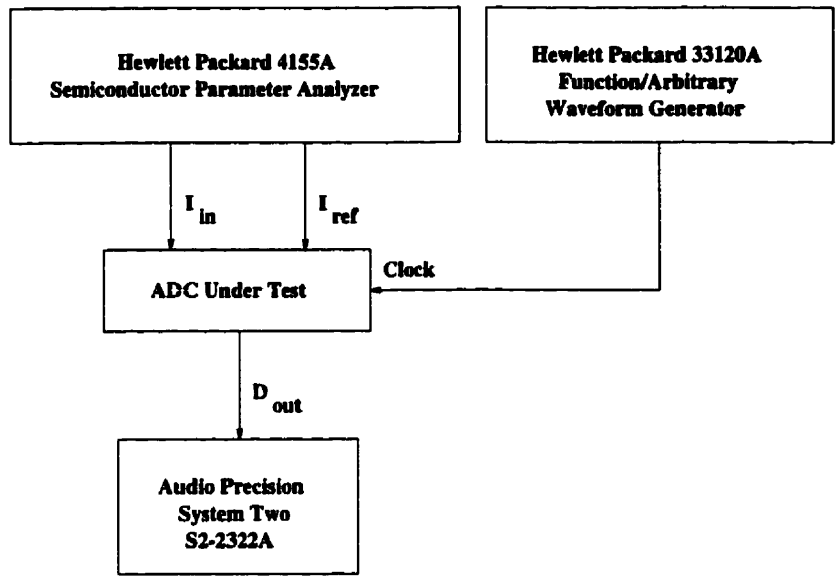


Fig. A.1 Setup for Testing the ADCs

A.2 Conversion Speed Measurements

The setup shown in Fig. A.1 can also be used to measure the conversion speed of the ADC. Different clock rates from Hewlett Packard 33120A are applied to the converter and the maximum rate at which the converter still displays its full resolution is measured.

A.3 References

[1] D. G. Nairn, "Current-Mode Algorithmic Analog-to-Digital Converters," *Ph.D. Thesis*, EE Dept., University of Toronto, 1989.

[2] G. Waterfall and B. C. Baker, "Digital-servo and linear-regression methods test high-resolution ADCs," *EDN*, vol. 40, pp.113-122, 1995.